

# **HGTD Module Assembly and Loading**

**Yunpeng Lu**

**2019.6.10**



# Proposed HGTD minimal results for TDR

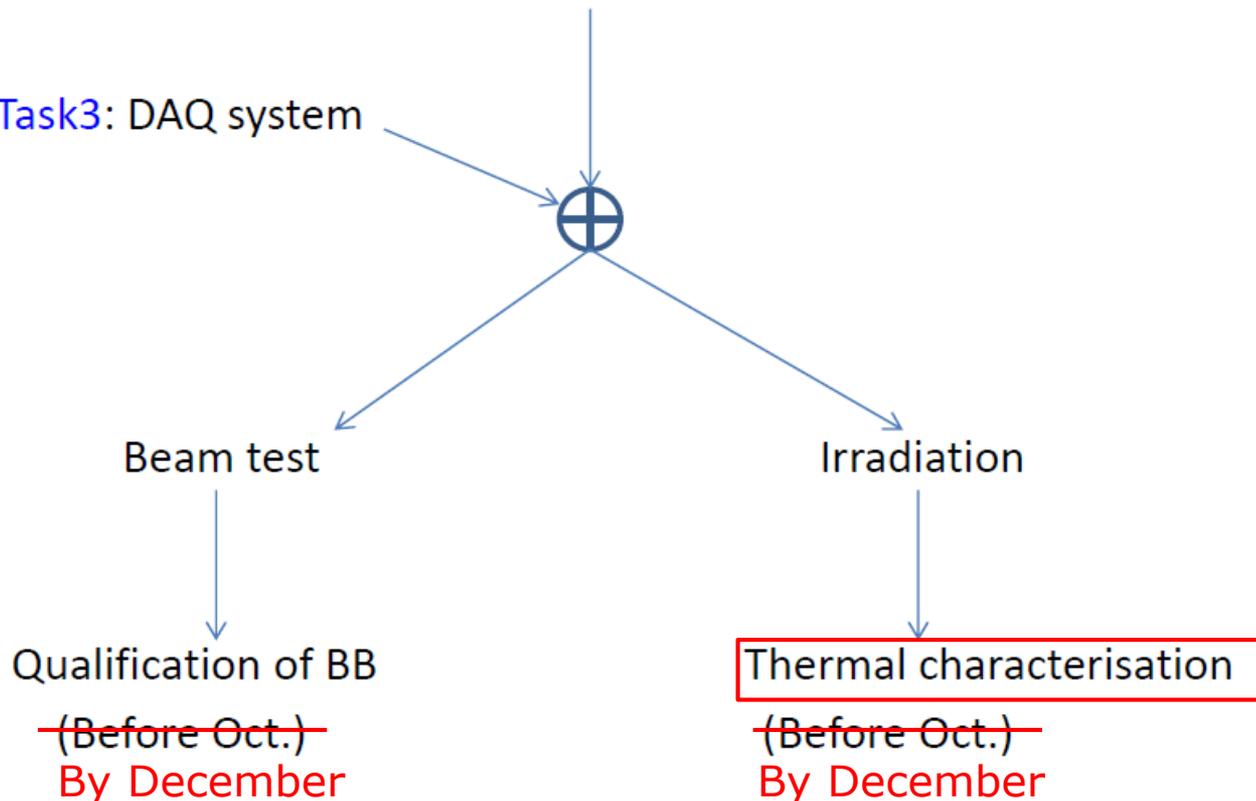
A. Henriques, L. Serin

- Introduction
  - Sensor : Irradiation program
    - Thermal runaway analysis
    - Other studies (\*)
  - ASIC : Lab characterisation
    - TID results
    - Final design (\*)
  - Mini-module (5x5 channels) : bare module assembly
    - bare module test beam performance
    - bare module irradiated : lab measurements
  - HGTD layout : Updated design with max fluence of  $3.e15$  n/cm<sup>2</sup>
  - Performance : Updated performance with rel20.20
  - Other activities update (\*)
  - Timeline
- (\*) Potential additional results

# List of Critical Module Tasks

- **Task1:** Detailed production plan for ~10K modules
  - Assemble and test time
  - Manpower required
- Bump-bonding
  - **Task2:** ALTIROC1 “mini-modules” made with 5\*5 sensors (**Urgent!**)

- **Task3:** DAQ system



# More to contribute

<https://indico.cern.ch/event/823044/>

## HGTD Module Assembly and Loading

Wednesday, 29 May 2019 - 10:00



: Sessions / : Talks : Breaks

29 May 2019	
AM	
10:00	Introduction - Lucia Masetti (Johannes Gutenberg Universitaet Mainz (DE)) Didier Lacour (LPNHE-Paris CNRS/IN2P3) Sebastian Grinstein (IFAE - Barcelona (ES)) () <a href="#">possible staves rearrangement.pdf</a>
10:10	Intermediate Plates Design - Didier Lacour (LPNHE-Paris CNRS/IN2P3) Didier Laporte (Centre National de la Recherche Scientifique (FR)) () <a href="#">2019_05_29_update LPNHE HGTD.pdf</a>
10:30	Status of dummy bare module and bump-bonding at SINAO - Yanwen Liu (University of Science and Technology of China (CN)) () <a href="#">Dummy and Bump Bonding at SINANO.pdf</a> <a href="#">Dummy and Bump Bonding at SINANO.pptx</a>
10:50	Bare module studies at IHEP - Zhijun Liang (Chinese Academy of Sciences (CN)) () <a href="#">IHEP_bump_bond_update_may29_v3.pdf</a> <a href="#">IHEP_bump_bond_update_may29_v3.pdf</a> <a href="#">IHEP_bump_bond_update_may29_v3.pptx</a>
11:00	Status of Hybridization and assembly at IFAE - Sebastian Grinstein (IFAE - Barcelona (ES)) () <a href="#">sgrinstein_hgtd_assembly_29May2019.pdf</a>
11:20	Flex status and splitted design (flex module and flex tail) - Maria Robles Manzano (Johannes Gutenberg Universitaet Mainz (DE)) () <a href="#">HGTD_assemblymeeting_29May2019_FLEX_Robles_v1.pdf</a>
11:40	A.O.B: what are the needs for the final assembly and commissioning at CERN and synergies with mod. assembly QA ?(space, clean room, cooling, tools...)? - Ana Maria Henriques Correia (CERN) () <a href="#">space and commissioning needs.pdf</a> <a href="#">space and commissioning needs.pptx</a>



# Current schedule on TDR

<https://indico.cern.ch/event/779123/contributions/3280950/subcontributions/271383/attachments/1783601/2903161/go>

<b>8.4-Module assembly+loading in staves</b> 8.4.1- Bump-bonding	Specifications doc.+SPR PDR FDR Pre-production PRR Production (0-50%) Production (51-100%)	<b>1 Jan 21</b> Q4 21 Q4 22 1 Oct 22 Q3 23 1 Sep 23 1 Aug 24	30 Sep 21 Q4 21 Q4 22 30 Jan 23 Q3 23 30 Jul 24 30 Jun 25
8.4.2-Flex cables	Specifications doc.+SPR PDR FDR Pre-production PRR Production (0-50%) Production (51-100%)	<b>1 April 21</b> Q4 21 Q2 22 1 Sep 22 Q2 23 1 Sep 23 1 Nov 24	30 Sep 21 Q4 21 Q2 22 30 Mar 23 Q2 23 30 Oct 24 30 Sep 25
8.4.3-Modules assembly	Specifications doc.+SPR PDR FDR Pre-production PRR Production (0-50%) Production (51-100%)	<b>1 Apr 21</b> Q4 21 Q3 22 1 Jan 23 Q4 23 1 Jan 24 1 Apr 25	30 Sep 21 Q4 21 Q3 22 30 Aug 23 Q4 23 15 Mar 25 1 Sep 26

# Current schedule on TDR

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8.4.4-Modules loading on staves	Specifications doc.+SPR PDR FDR Pre-production PRR Production (0-50%) Production (51-100%)	<b>1 April 21</b> Q4 21 Q4 22 1 April 23 Q1 24 1 Mar 24 1 May 25	30 Oct 21 Q4 21 Q4 22 30 Dec 23 Q1 24 30 April 25 30 Sep 26
<b>8.7 Installation and commissioning</b> 8.7.1 and 8.7.3 (Services,p. panels,cool.,mod.) 8.7.2 Back-end electronics inst. in USA15 <b>8.7.4 HGTD-A (w/ 1 layer)</b> <b>8.7.4 HGTD-C (w/ 1 layer)</b> 8.7.5 Commissioning in LS3 (w/ IL/EC) <b>8.7.6 HGTD-A (w/ layer 2) in YETS27</b> <b>8.7.6 HGTD-C (w/ layer 2) in YETS27</b> 8.7.7 Commissioning in YETS27 (w/ 2L/EC)	Installation+QA (0-100%) Installation+QA (0-100%) <b>Installation</b> <b>Installation</b> Commissioning <b>Install in situ layer 2</b> <b>Install in situ layer 2</b> Commissioning	30 Jan 24 1 Jul 24 <b>2 Jun 25</b> <b>3 Jul 25</b> 3 Jul 25 <b>1 Jan 27</b> <b>1 Feb 2027</b> 1 Mar 27	30 Apr 25 30 Jun 25 <b>2 Jul 25</b> <b>1 Aug 25</b> 10 Mar 26 <b>30 Jan 27</b> <b>2 Mar 27</b> <b>30 May 27</b>



## Bare mini-modules (5x5 channels)

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Bare module assembly :

- Bare module already assembled at IFAE and IHEP with ALTIROC1-V1 but cannot be used for any ASIC measurement (need to access to a debugging pad & probe to cure gate leakage current problem for discriminator)

→ currently (this week) trying to assemble one sensor shifted by one column to V1

- Bare module with ALTIROC1-V2 :

→ Expect first assembly in July (IFAE/IHEP) for lab measurements, testbeam and irradiation

DESY testbeam : 19-25 Aug (debugging) & 4-17 Nov (non irradiated module performance)

Irradiated module in testbeam in Nov ?

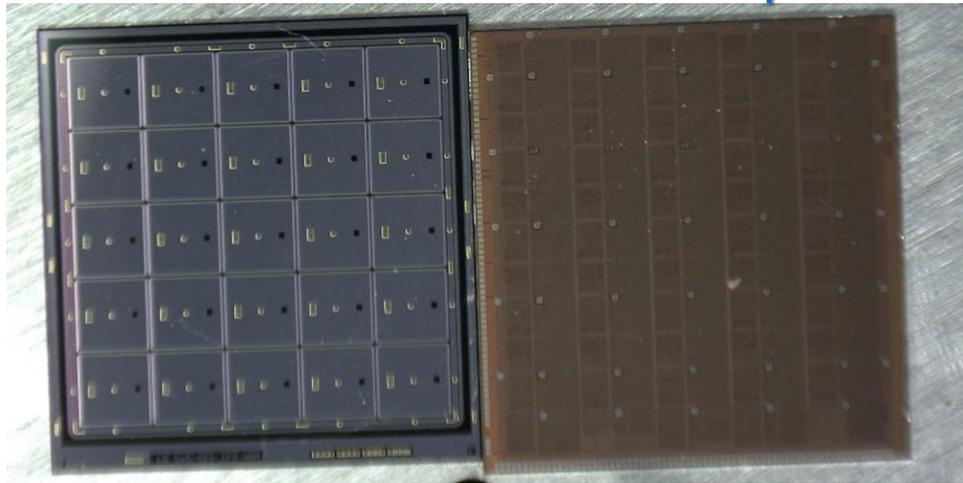
Module irradiation : can not assemble sensor already irradiated (annealing)

Assemble module → neutron irradiation → lab measurement (Q vsV) → TID  
→ lab measurements

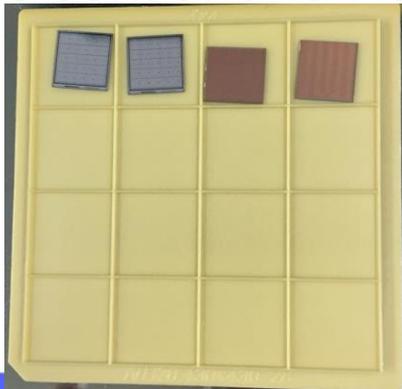
- Module assembly in German & Chinese companies
-

# Bump bonding study

- Identify two company identified (both are top 10 packaging company)
    - The National Center for Advanced Packaging (NCAP, 华进)
      - <http://www.ncap-cn.com/en/index.aspx>
- HPK 5x5 Sensors and Altirco1 chip in IHEP



5x5 sensor and ASIC

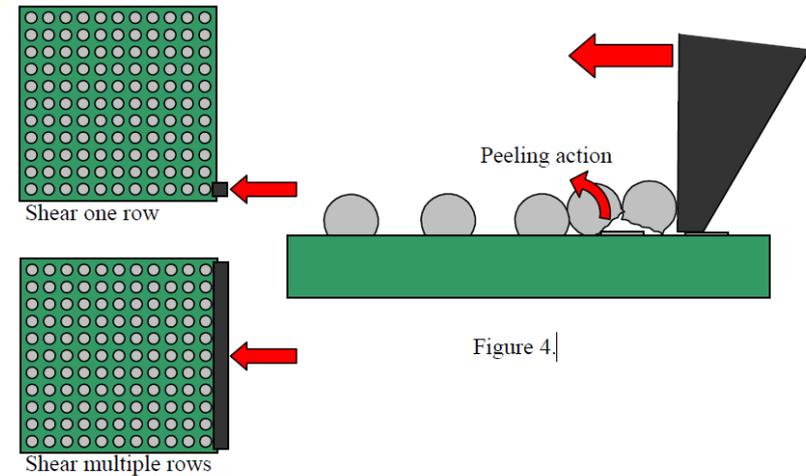


Bare module



# Bond Test

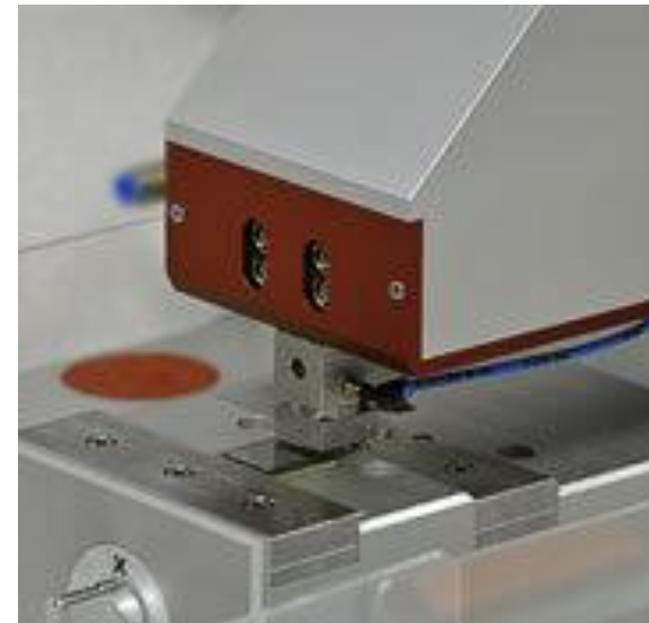
- Proper tools needed
  - DIE SHEAR
  - FLIP CHIP PULL
- Operator



## Dage 4000 | Standards

The Dage 4000 conforms to and in some cases exceeds the following industry standards:

CBP/HBP	JEITA EIAJ ET-7407
BGA BUMP SHEAR	JEDEC JESD22-B117
AU BALL SHEAR	JEDEC JESD22-B116
BALL BOND SHEAR	ASTM F1269
WIRE PULL DT/NDT	MIL STD 883
DIE SHEAR	MIL STD 883
STUD PULL	MIL STD 883
FLIP CHIP PULL	JEDEC JESD22-B109



# Setting up the FPGA Board

- Yunyun and Shuo are working on the FPGA board

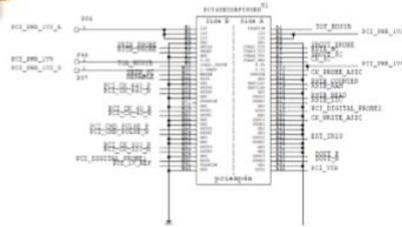
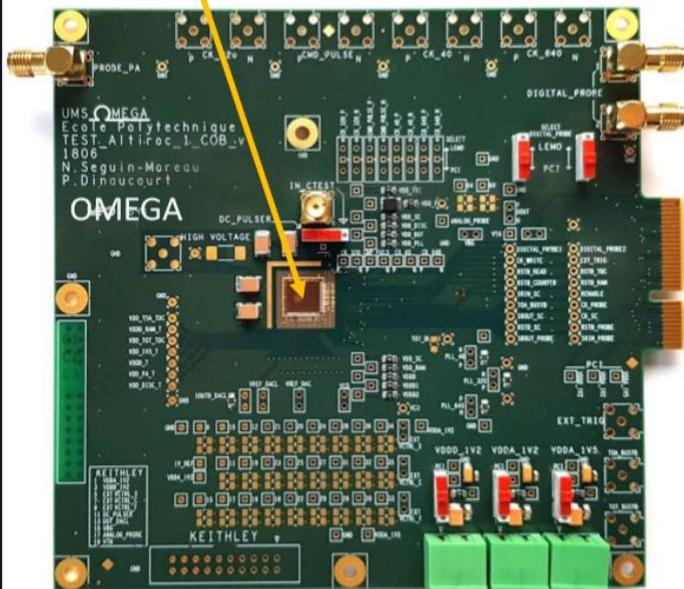
## SETUP for ALTIROC1 measurements

- One setup @ OMEGA + one setup @ SLAC, debug tests started at the end of November



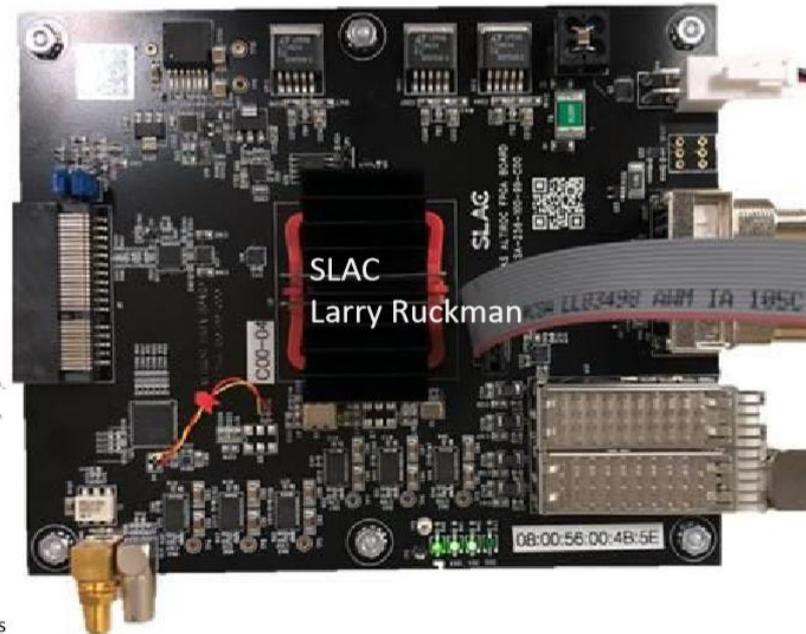
Altiroc1 die

Wire bonding @ IFAE



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ALTIROC2 - Initial Design Review - Analog part measurements



SLAC  
Larry Ruckman

# What we can do now

- Possibility of sharing of resources with ITK
- Bump bonding test
  - Very “hardware”
- ALTIROC1 readout board

