HGTD DAQ AND ELECTRONICS

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HGTD IHEP Workshop
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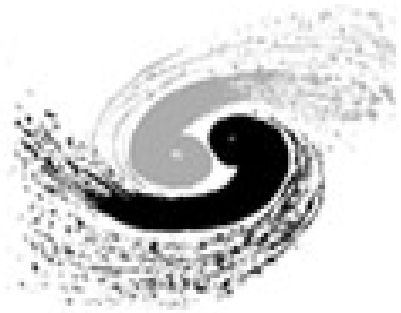
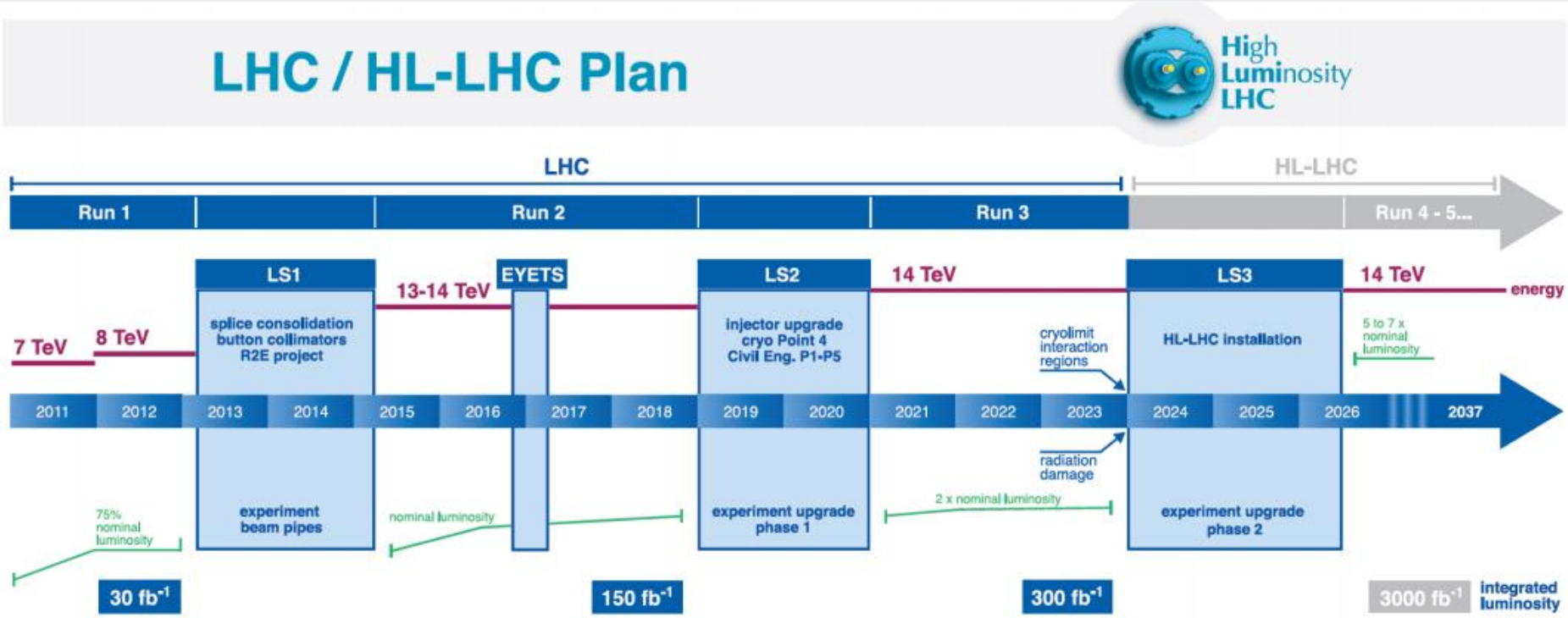


Institute of High Energy Physics
Chinese Academy of Sciences

OUTLOOK

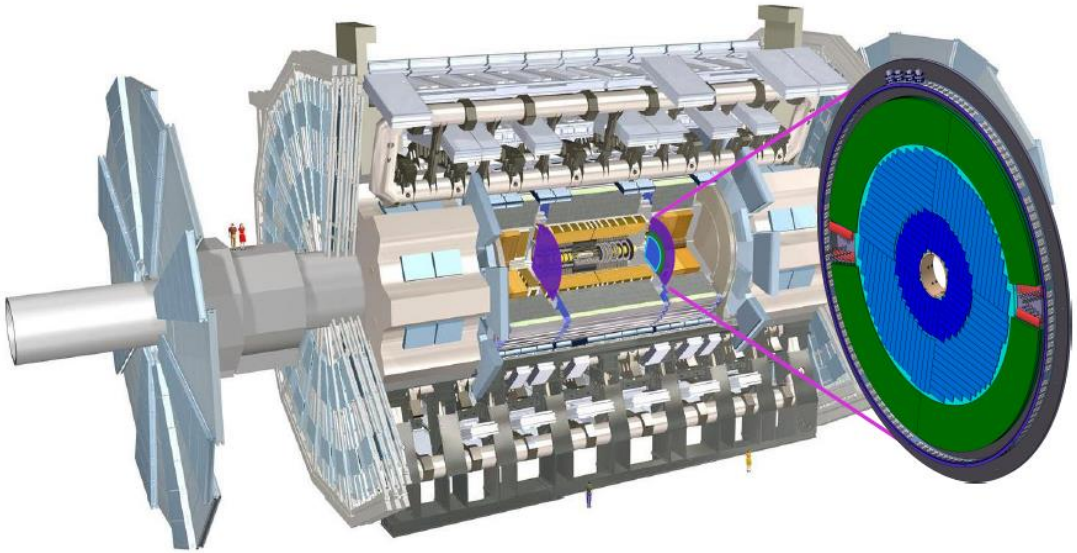
- HGTD requirements
- HGTD readout system
  - On detector electronics
  - Off detector electronics
- DAQ and Luminosity
- HGTD demonstrator
- TO-DO list

HGTD REQUIREMENTS



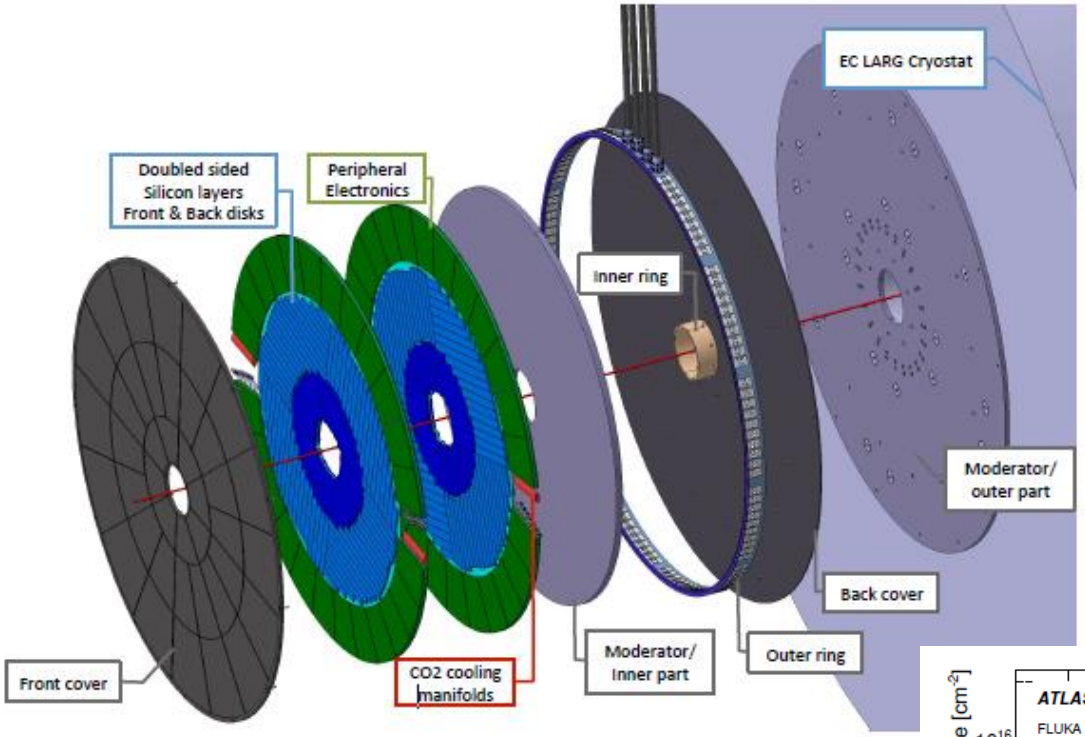
$L = 7.5 \times 10^{34}\ cm^{-2}\ s^{-1}$
Pile-up of $\mu \approx 200$

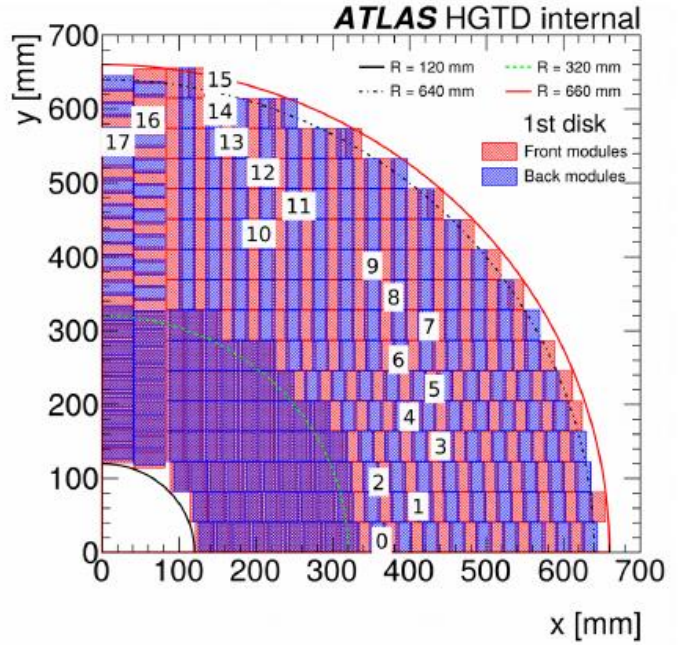
High Granularity Timing Detector will provide time resolution at a high pile-up

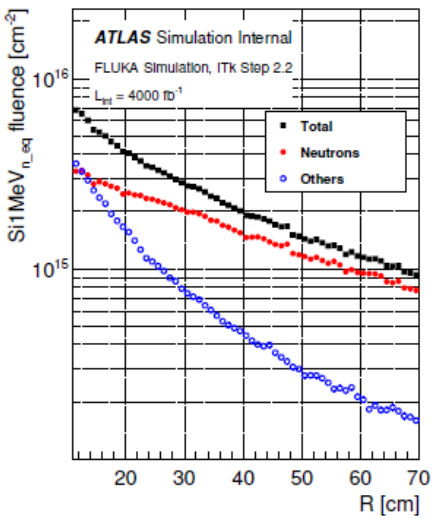


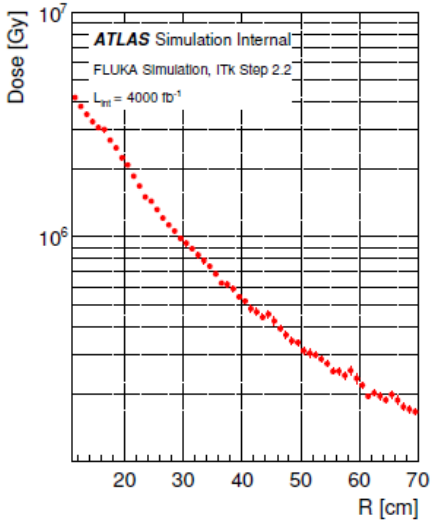
HGTD REQUIREMENTS

Detector layout and radiation hardness:









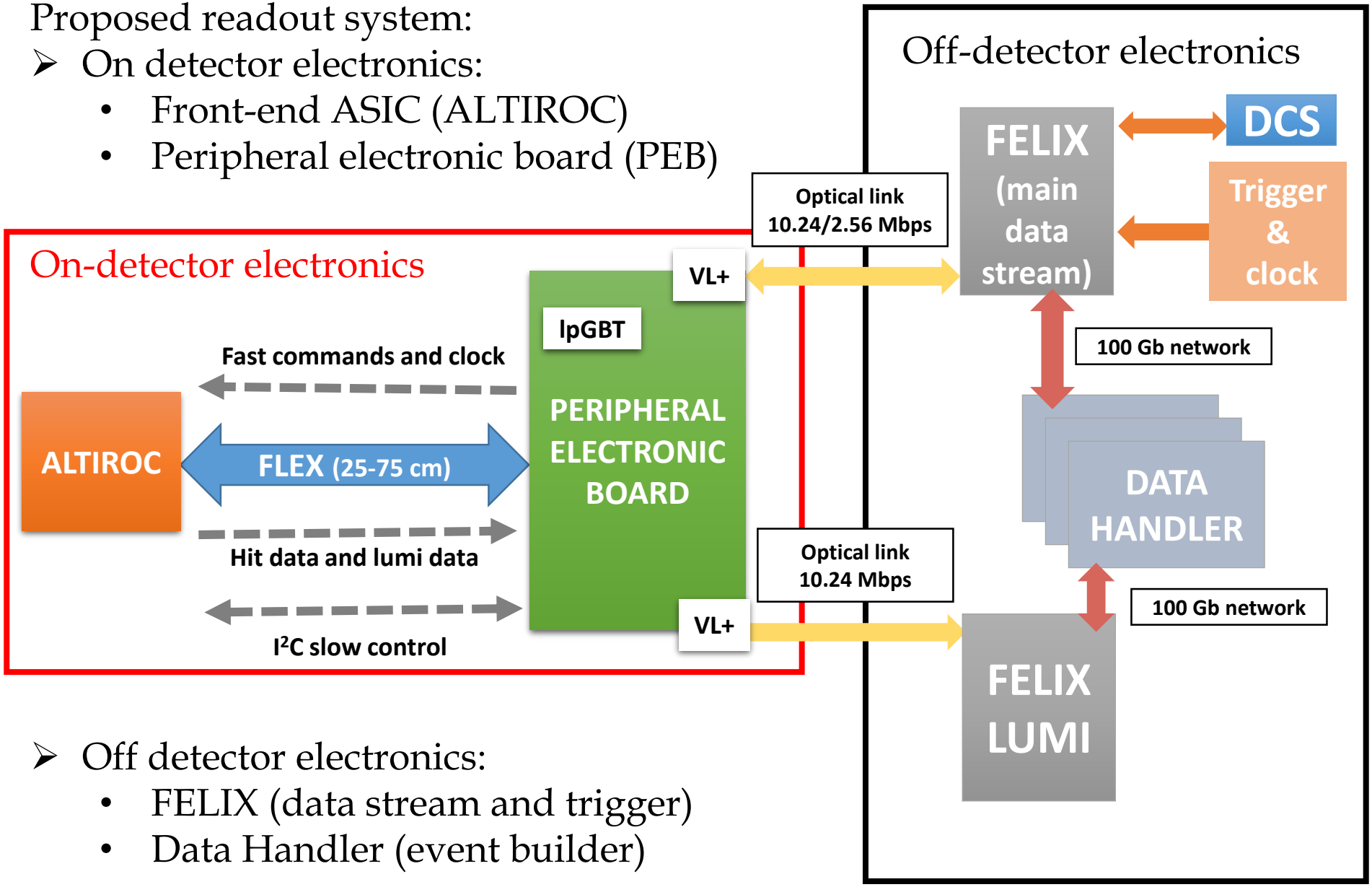
Radiation hardness is required for all the components:

- Sensor
- On-detector electronics

HGTD READOUT SYSTEM

Proposed readout system:

- On detector electronics:
  - Front-end ASIC (ALTIROC)
  - Peripheral electronic board (PEB)

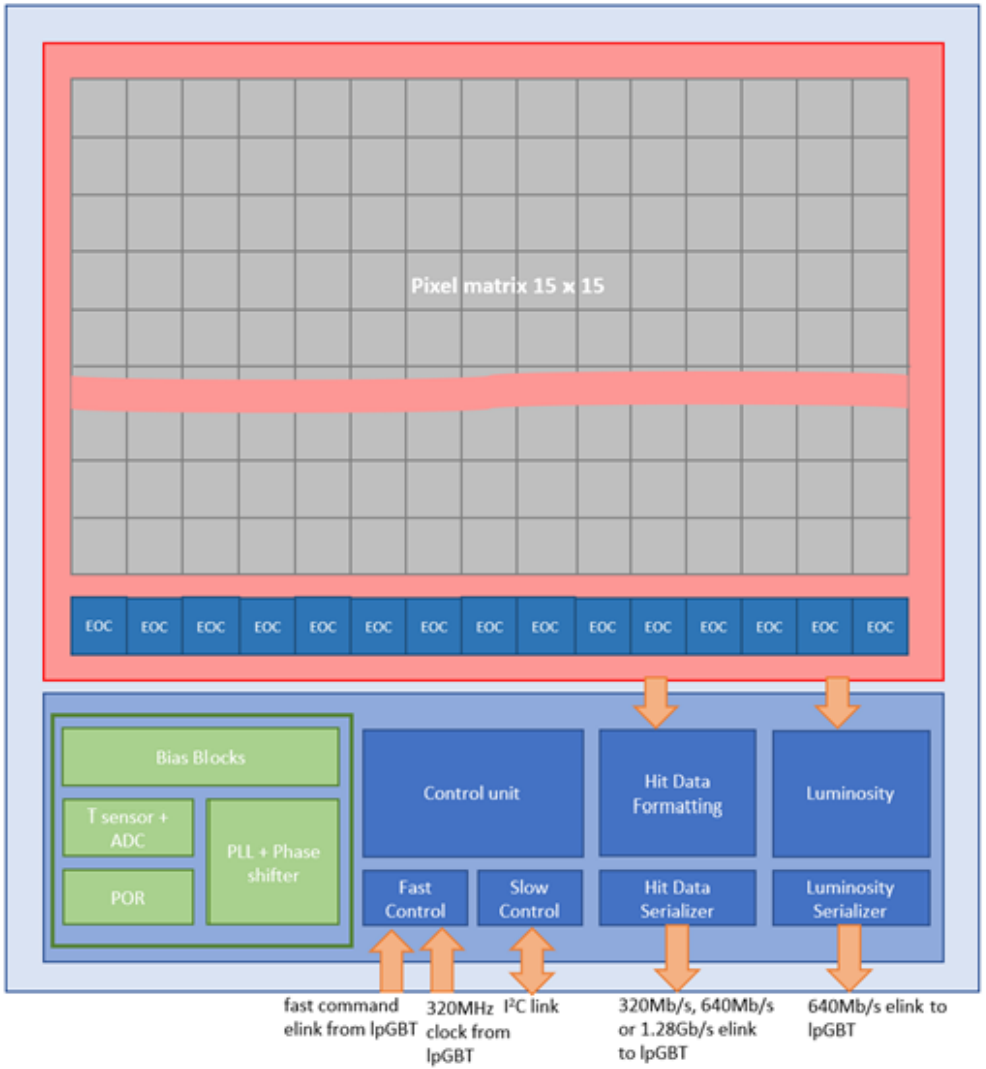


- Off detector electronics:
  - FELIX (data stream and trigger)
  - Data Handler (event builder)

ON DETECTOR ELECTRONICS

Front-end ASIC (ALTIROC) readout architecture:

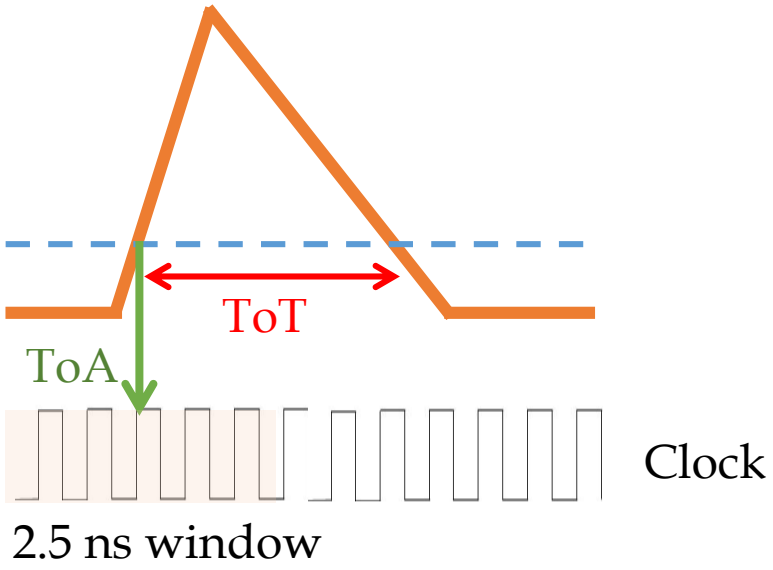
- 130 nm CMOS technology
- Analog and digital architecture
- End of column (EOC) logic
- 225 channels (pixels)/ ASIC
- I^2C link for slow control
- PLL and phase shifter
- DAQ stream 320, 640 and 1280 Mbps
- Luminosity stream 640 Mbps



ON DETECTOR ELECTRONICS

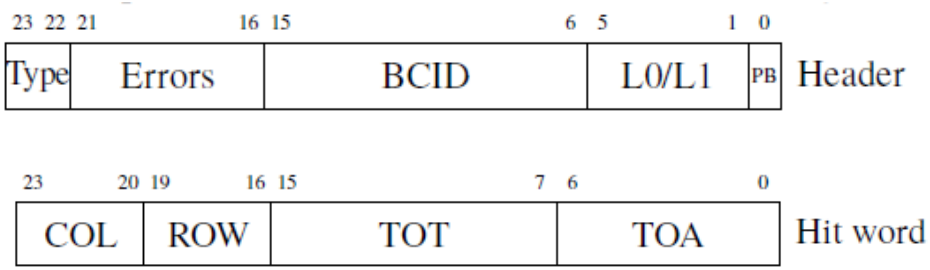
ALTIROC requirements:

- Radiation hardness ~5 MGy
- Clock jitter <25 ps
- Time over threshold (ToT) and Time of Arrival (ToA) information
- Latency up to 35 µs @ 40 MHz
- Low power dissipation



Hit data format:

- 8b10b encoding
- Header: (BCID,L0, parity bit,...)
- Hit word:
  - Row, col
  - ToT (9 bits)
  - ToA (7bits)

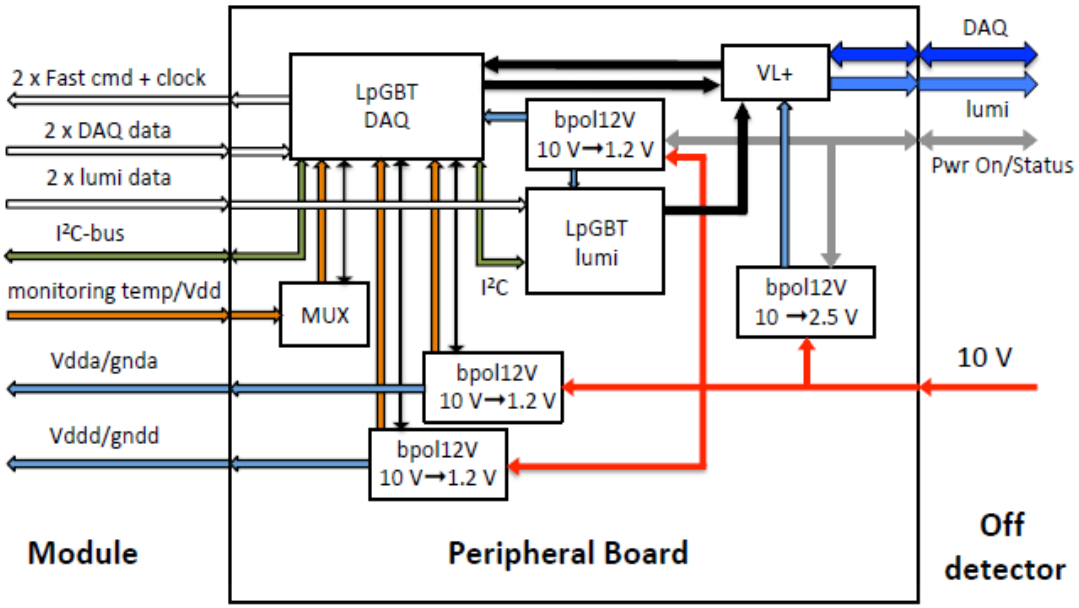


See Jie Zhang talk about the data format

ON DETECTOR ELECTRONICS

Peripheral electronic board:

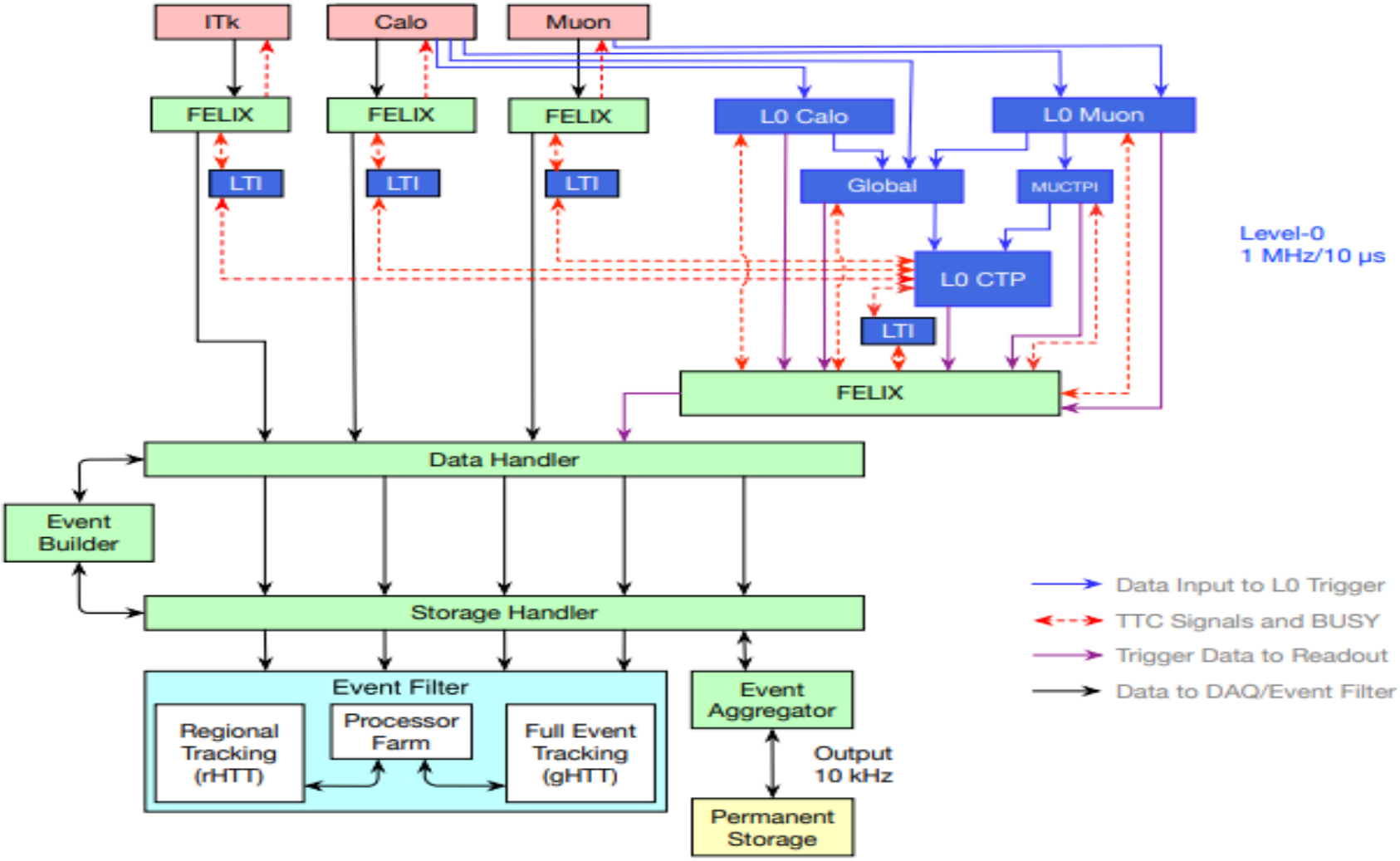
- 10 V to 1.2 V DC-DC converter
- High voltages
- Versatile link Plus: 2.56 and 10.24 Gbps (up/down-link)
- Low power GigaBit Transciver (lpGBT)
  - Radiation hard
  - Low power dissipation
  - Clock jitter <2 ps
  - I²C bus
  - E-link data stream 320, 640 and 1280 Mbps
  - E-link data up 80, 160 and 320 Mbps



Need to identify a person for the PCB design and construction!!

OFF DETECTOR ELECTRONICS

ATLAS phase II readout architecture:



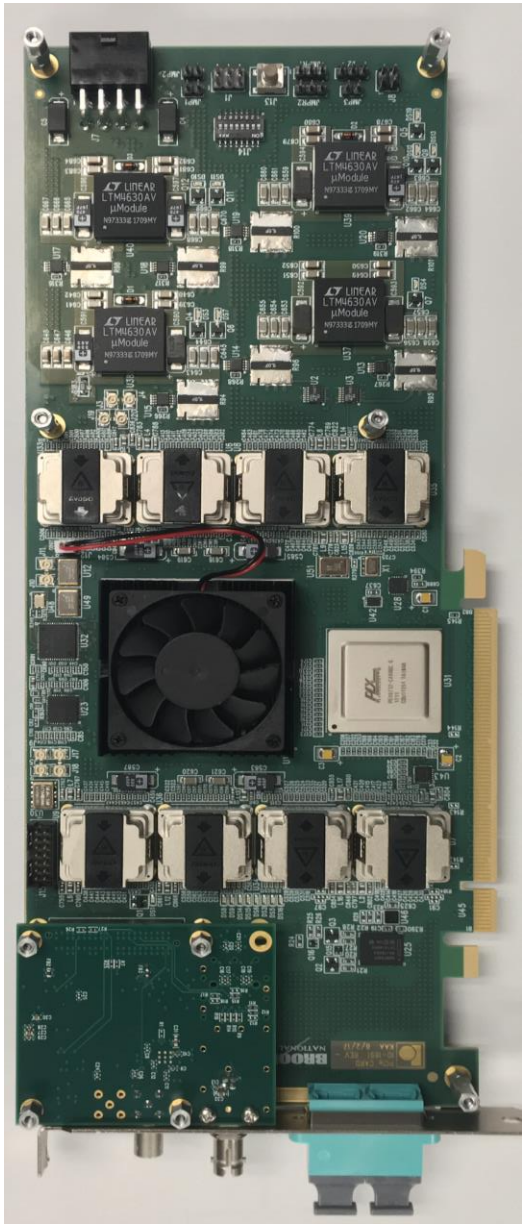
OFF DETECTOR ELECTRONICS

The FELIX (Front End LInk Exchange) board:

- Detector independent (common to all ATLAS detectors).
- Support standard GBT protocol.
- Distribute TTC (Timing, Trigger and Control) signals via fixed latency.
- Support control, calibration and monitoring of sub-detectors.

FELIX will interface with most of the ATLAS systems:

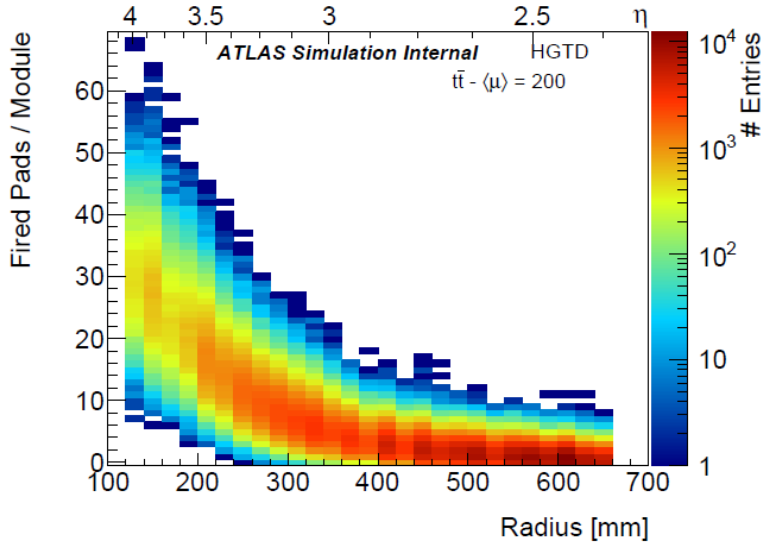
- Data handler → Event builder
- Detector Control System (DCS): LV current, temperature,...
- On-line monitoring
- Control and configuration of the FE ASIC



DAQ AND LUMINOSITY

High uncertainty in the occupancy:

- Average vs maximum
- ITK Pixel layout/services
- Trigger effect: We typically trigger in fill (high occ) bunches
  → Underestimated?



Readout layout:

- r < 200 mm

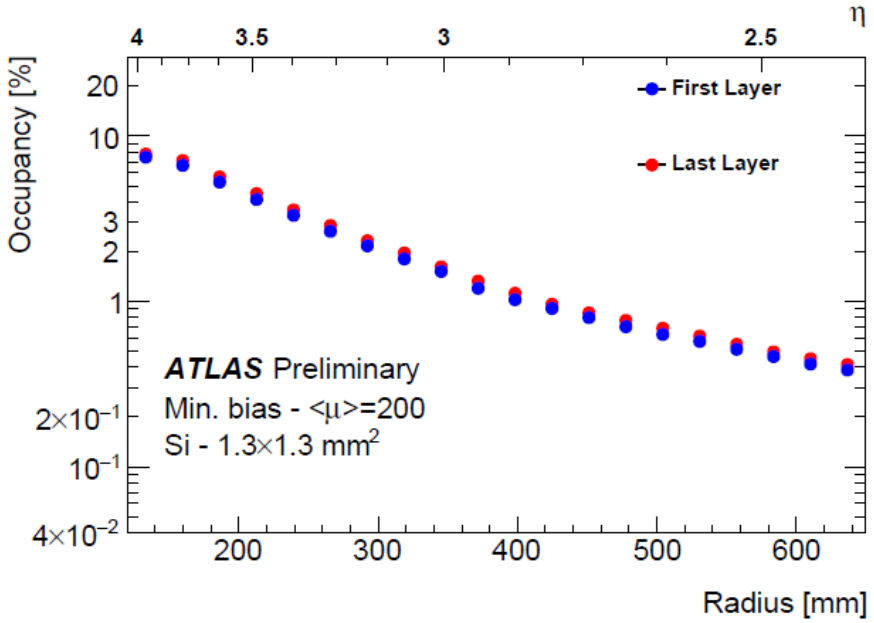
→ readout speed = 1280 Mbps

- 200 < r < 320 mm:

→ readout speed = 640 Mbps

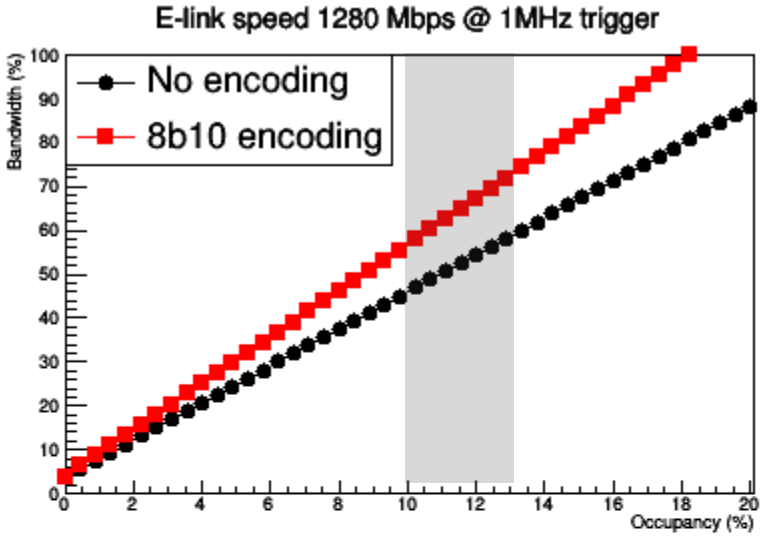
- r > 320 mm:

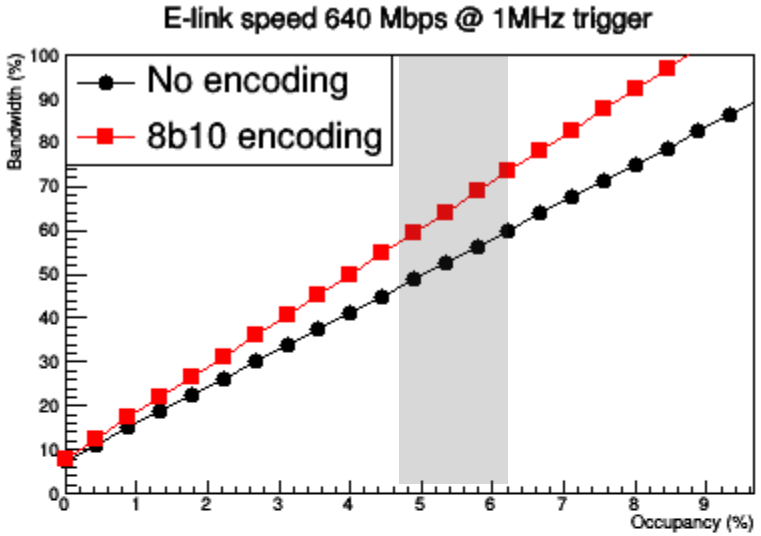
→ readout speed = 320 Mbps

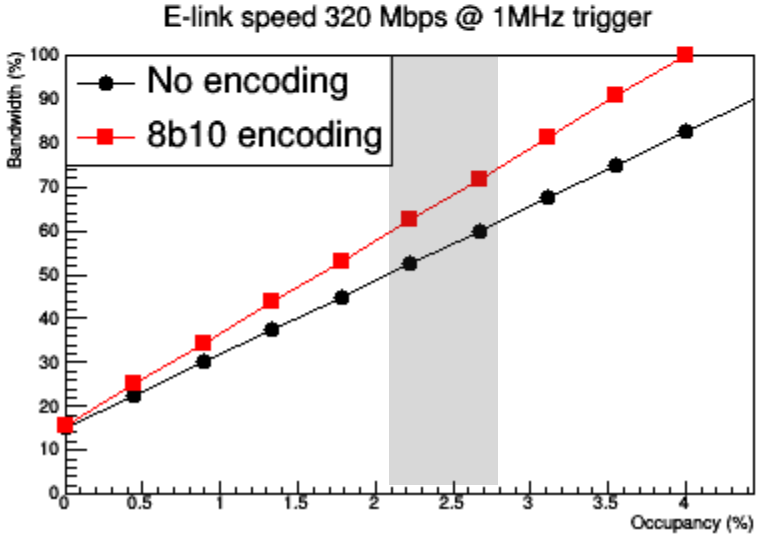


DAQ AND LUMINOSITY

Expected link usage at different link speeds:





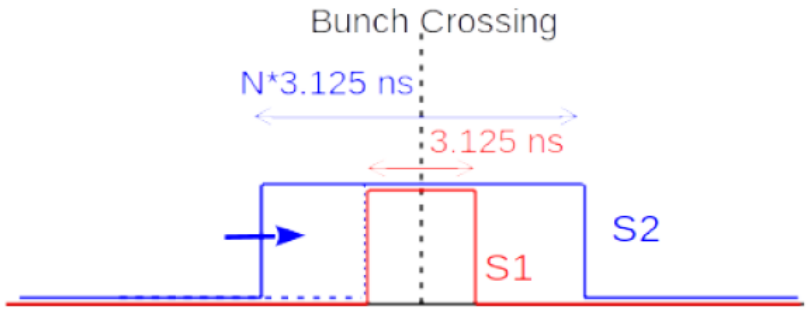


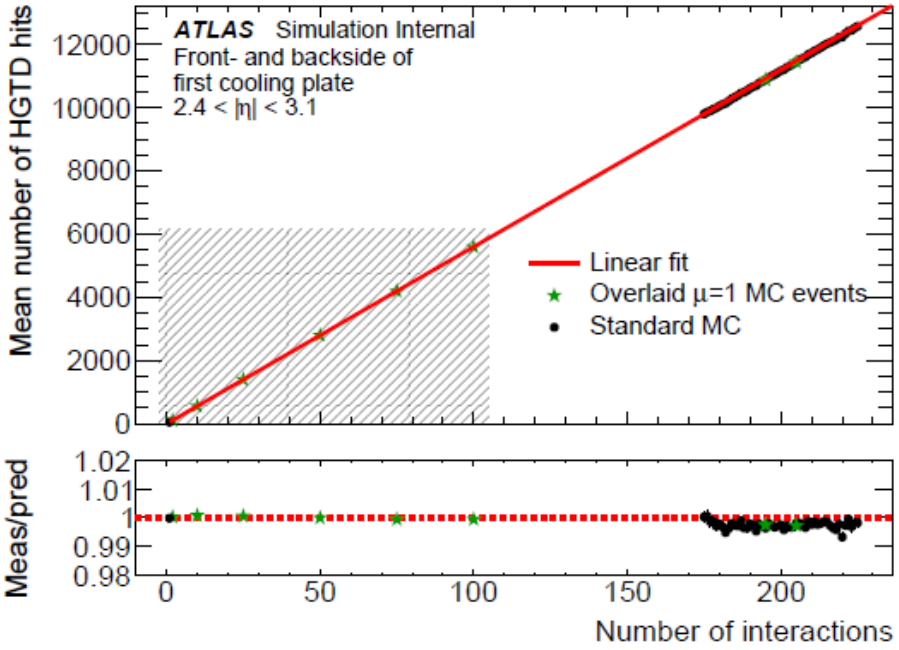
Upper limit on the number of hits/ASIC driven by the bandwidth
→ This is linked with the ALTIROC data format

DAQ AND LUMINOSITY

HGTD as luminometer:

- Bunch by bunch information at 40 MHz
- Sum of the hits between two different time Windows (S1 and S2)
- Dedicated luminosity stream at 640 Mbps.
- Only a sub-sample of modules will be used for luminosity measurements 200 < r < 320 mm
- Off detector readout: Dedicated FELIX lumi boards.

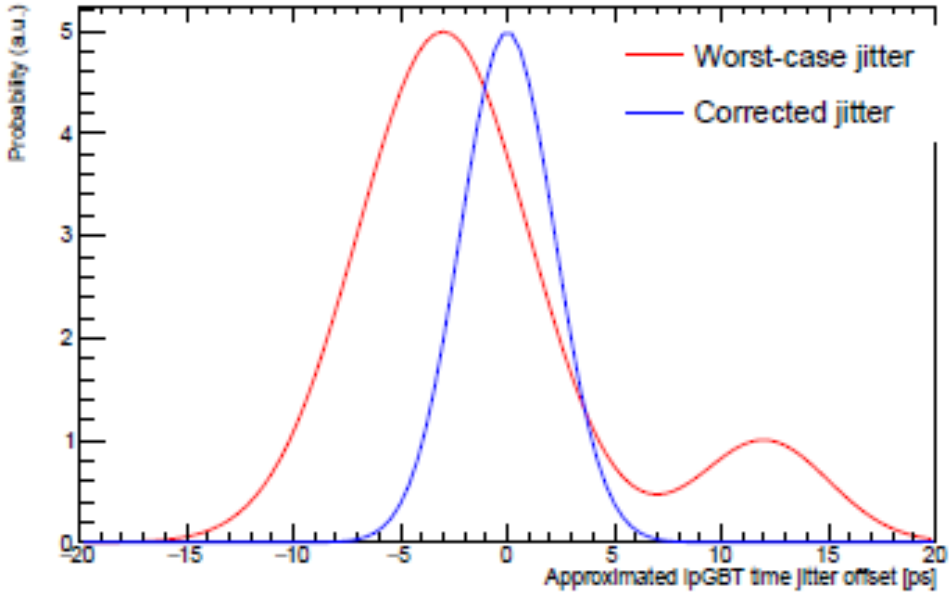




DAQ AND LUMINOSITY

T0 calibration:

- Particularly challenging:
  - Bunch by bunch inhomogeneities in t0
  - Different sources of clock jitter: LHC, FELIX, lpGBT, ALTIROC,...
  - Dynamic contributions: Noise from the flex, day/night temperature changes,...
- A t0 calibration procedure is under study



See Ludovica's talk on the t0 calibration

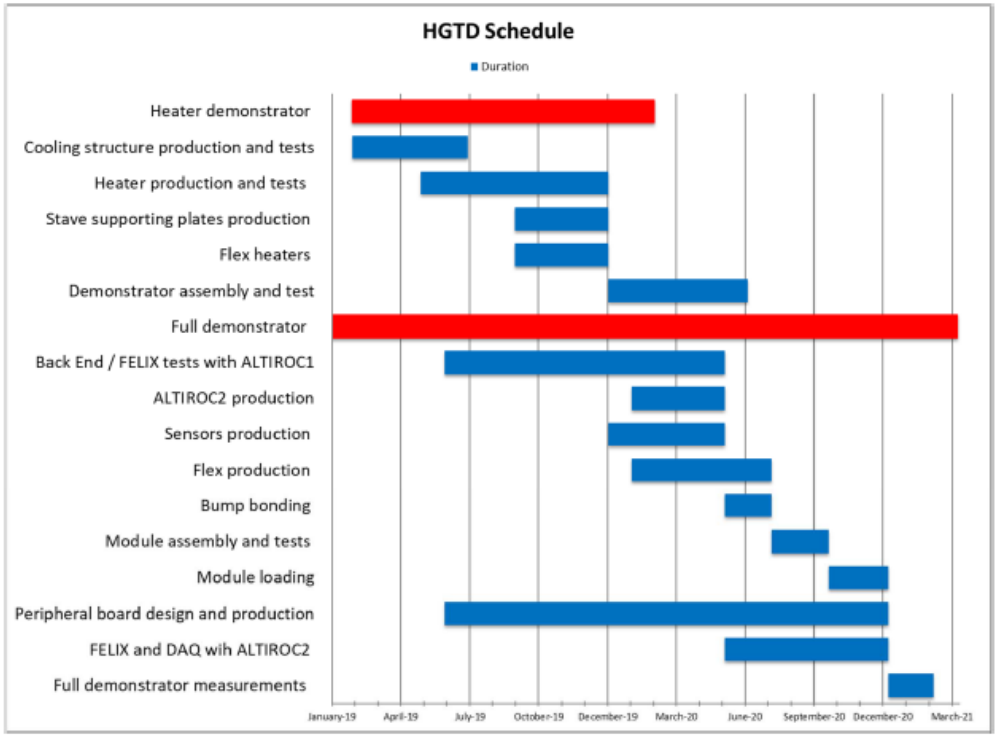
HGTD DEMONSTRATOR

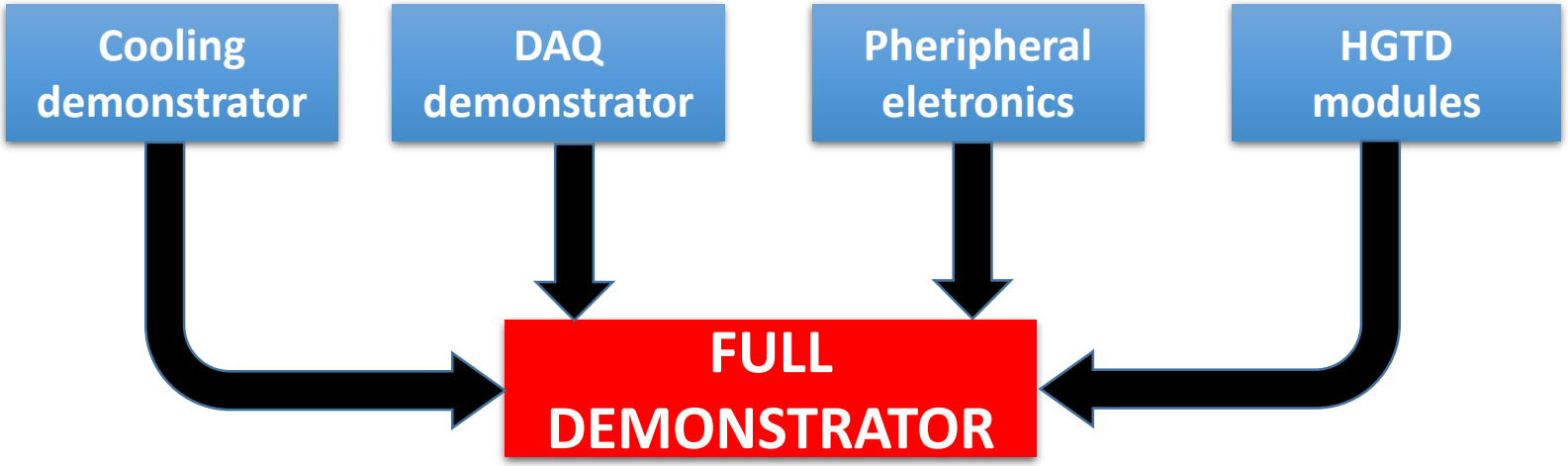
An space has been identified for HGTD demonstrator at CERN

HGTD DEMONSTRATOR

Proof of concept:

- Cooling demonstrator with heaters → Validate termal model and loading procedure
- Mechanical structure and services
- HGTD modules
- DAQ/Luminosity demonstrator (FELIX+GBT)
- Peripheral electronics





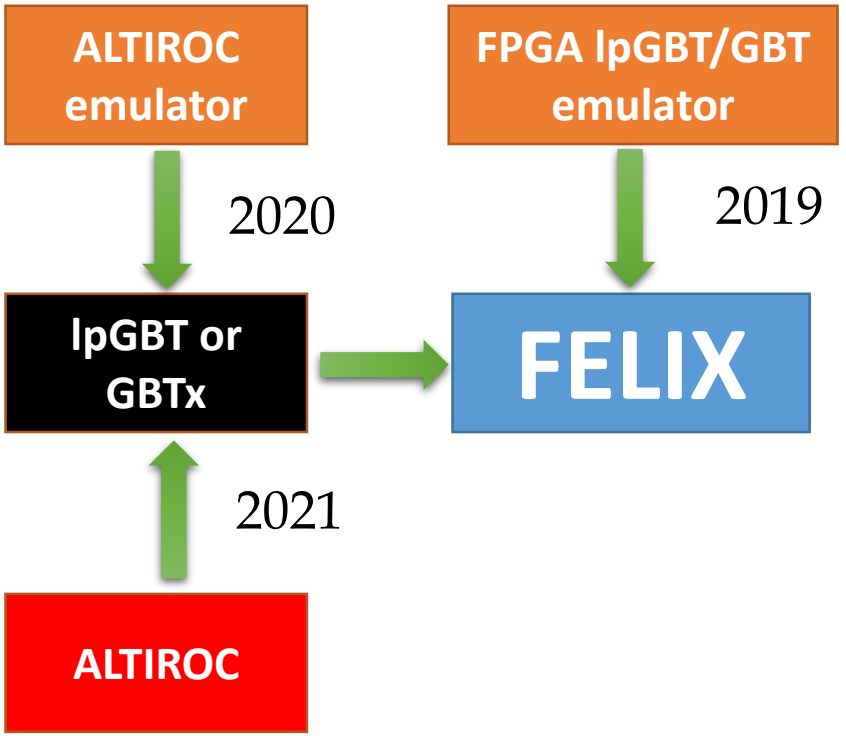
HGTD DEMONSTRATOR

DAQ demonstrator roadmap:

- 2019: Validation of FELIX readout with FPGA emulator
- 2020: Validation of lpGBT + ALTIROC emulator
- 2021: First test with ALTIROC modules

Further test:

- Measurement of clock jitter: FELIX+lpGBT+FLEX+ALTIROC
- Validate services (LV,HV,...)
- Develop a calibration procedure: FELIX + YARR (Yet Another Rapid Readout): Generic PCI SW and FW meant for calibrations.



FELIX board just arrive for first test

TO-DO LIST

- Front-end ATLIROC
  - Data format (Jie Zhang)
  - Command decoder
- Peripheral electronics:
  - PCB design and construction
  - Integration of lpGBT and Versatile link
- T0 calibration (Ludovica)
  - Study of bunch by bunch t0 drift
  - Measurement of the jitter performance after the FLEX
- DAQ demonstrator (myself):
  - FPGA lpGBT/GBT emulator
  - ALTIROC emulator
  - Interface with FELIX
  - Proof of concept of peripheral boards
  - Calibration procedure


Thank You

BACKUP

Useful links:

- TDAQ requirements phase II: https://edms.cern.ch/ui/file/1563801/1/RequirementsPhaseII_v1.1.0.pdf
- lpGBT: https://espace.cern.ch/GBT-Project/LpGBT/default.aspx
- FELIX: https://atlas-project-felix.web.cern.ch/atlas-project-felix/
- HGTD: https://cds.cern.ch/record/2623663/files/LHCC-P-012.pdf
- YARR: https://yarr.readthedocs.io/en/latest/