

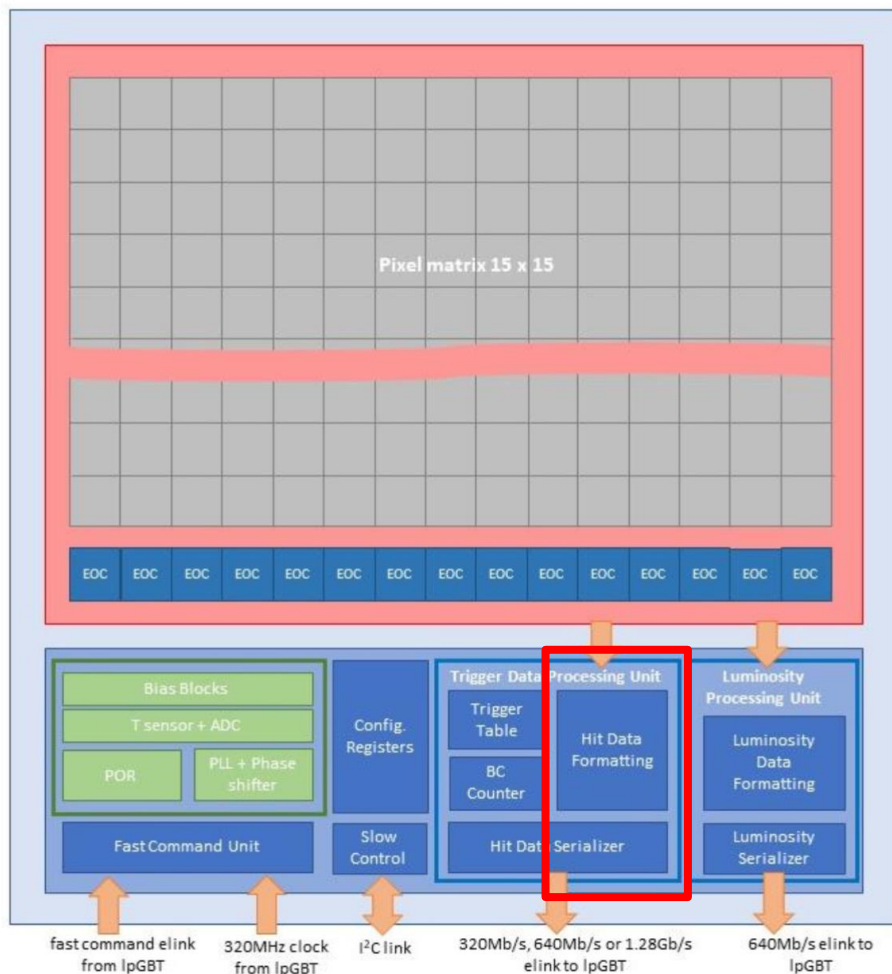


DATA FORMATTING AND TRANSMISSION OF ALTIROC2

Jie Zhang, Raimon Casanova Mohr

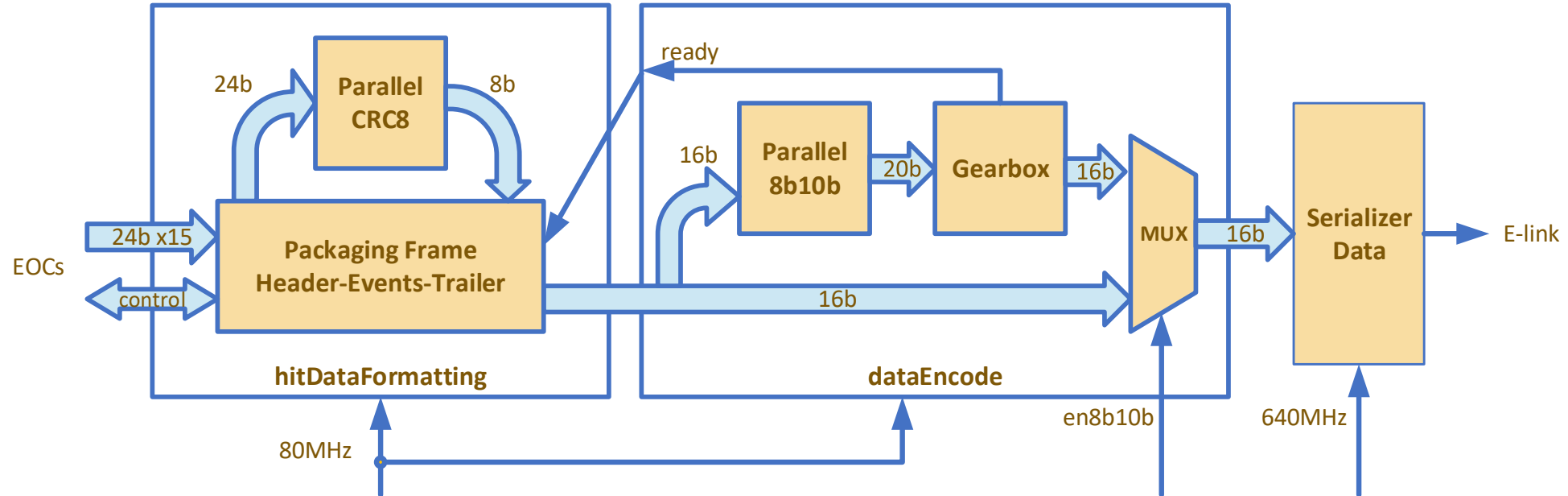
zhj@ihep.ac.cn

REQUIREMENT



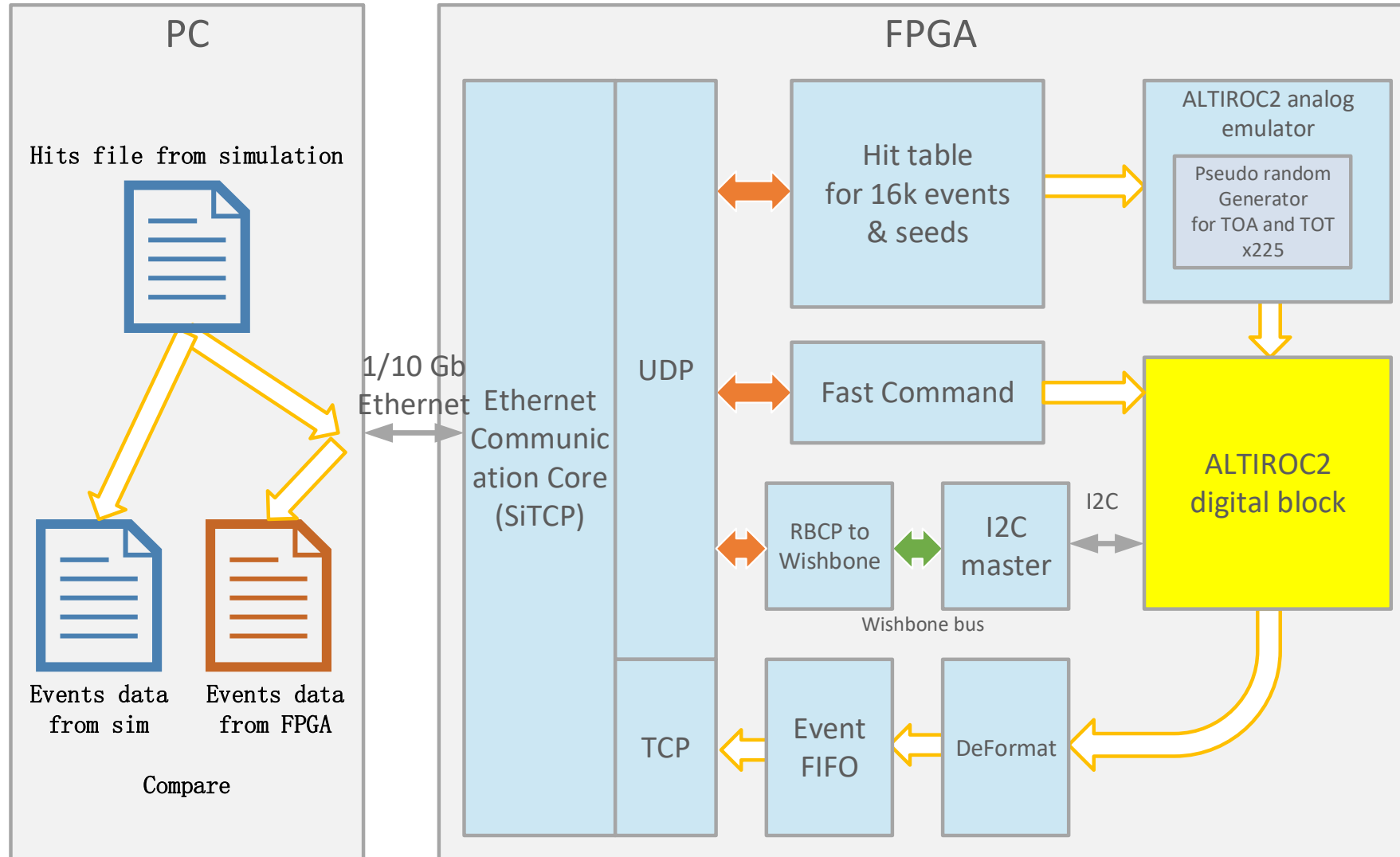
- Upon receiving the trigger signal, the control unit requests the EOCs to retrieve and store the data from the pixels.
- Pack the data in frames, serialize and transmit them to the peripheral on-detector electronics through e-links.
- Frame protocol
 - 8b10b encoding mode
 - Raw data mode
 - Configurable through I2C, [Details](#)
- Transmission speed
 - 320 Mb/s, 640 Mb/s or 1.28 Gb/s
 - Configurable through I2C

IMPLEMENTATION



- To full fill the bandwidth at 1.28Gbps, we replace the 40MHz clock to 80MHz to fetch more data from EOCs
 - $24b \times 40 = 960b$
- Calculate the CRC8 with 24-bit in parallel
- The FSM need to handle two bytes in parallel
 - $16b \times 80 = 1280b$
- Calculate the 8b10b with 16-bit in parallel
- Only 640MHz clock is used for serializing with double data rate (DDR)

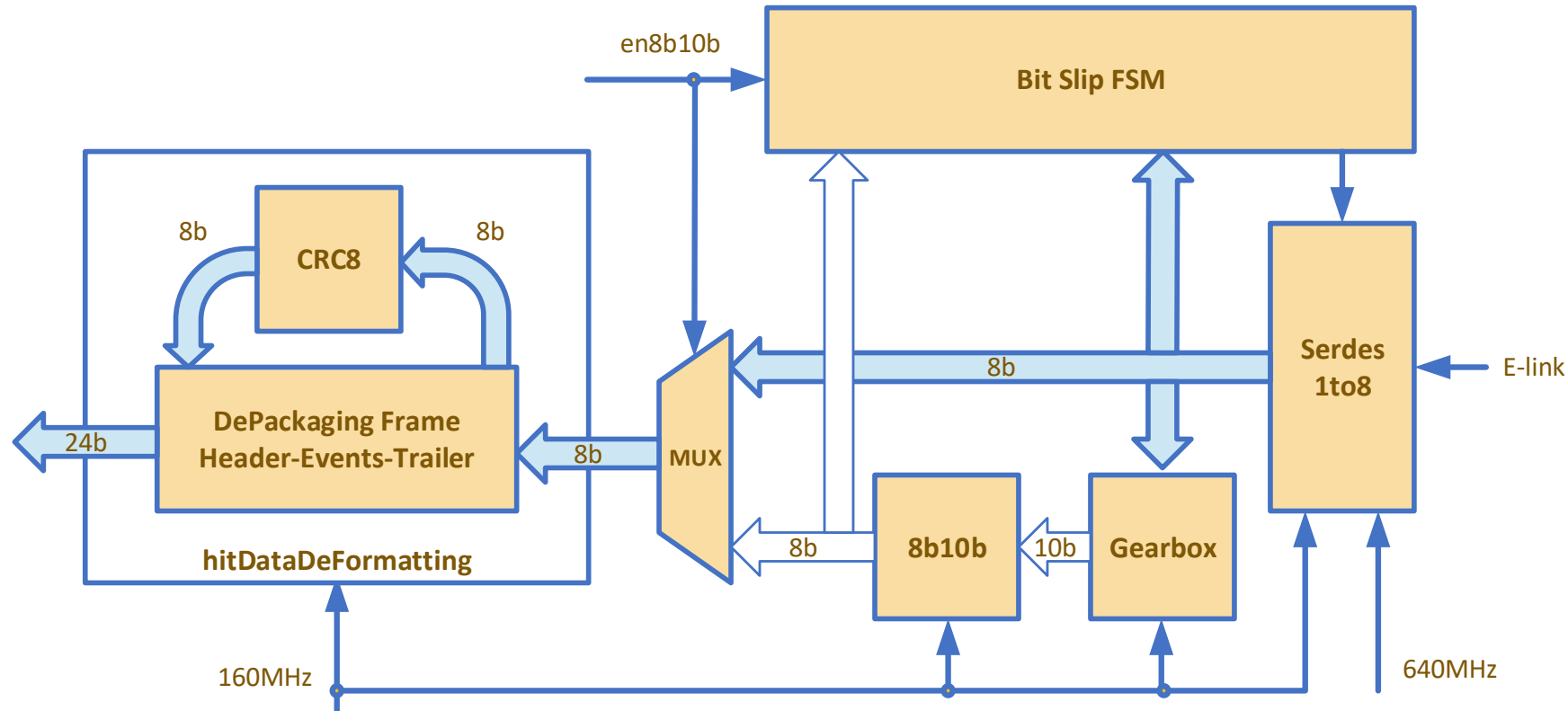
TESTING PROCESS



1. Get the hits file from simulation.
2. Send it to the emulator via Ethernet.
3. Generate pseudo random numbers as TOT and TOA.

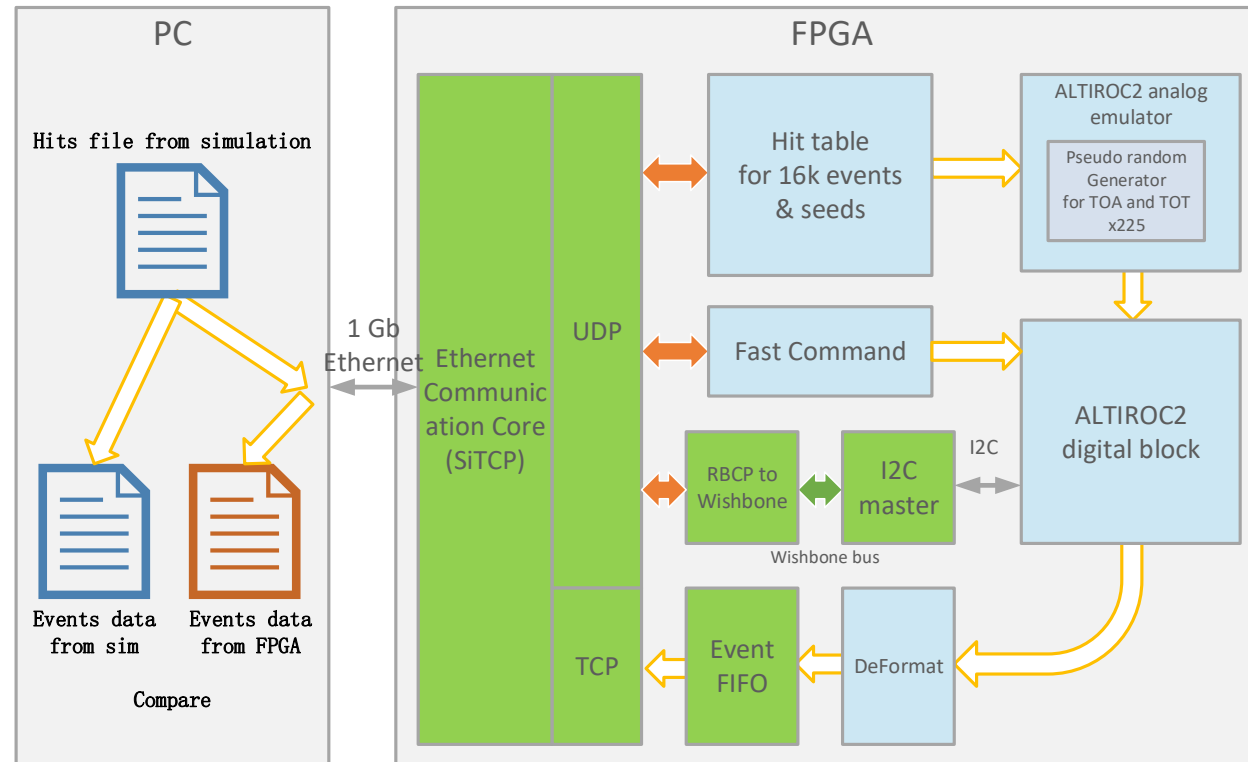
Generate the triggers to start the data acquisition.
4. Readout the events from FPGA
5. Compare the events with the one from simulation

DE FORMATTING IN FPGA



- The main clock is 160Mhz
 - Easy to handle the data in byte mode, for 8b10b and CRC8

PROGRESS



- The green blocks are ready, the blue blocks are under development
- The HDL codes are uploaded to Gitlab,
https://gitlab.cern.ch/jiezh/altiroc2_emulator
- The scripts for DAQ/slow control at PC are written by Python
- The register map and descriptions are uploaded to Wiki
https://gitlab.cern.ch/jiezh/altiroc2_emulator/wikis/home.



THANKS TO YOUR ATTENTION

SIMPLIFIED MODEL

Network Layer

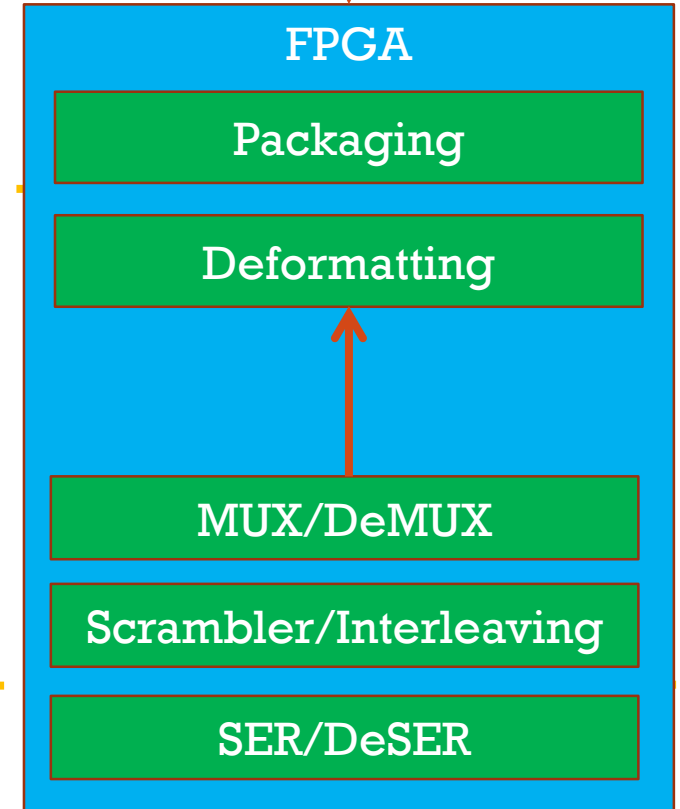
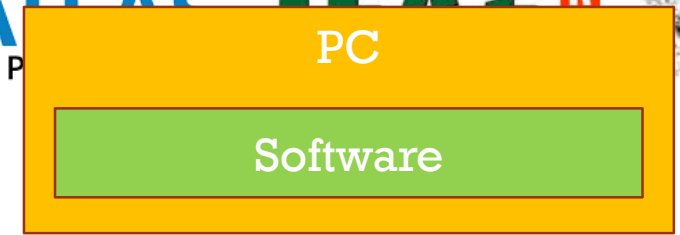
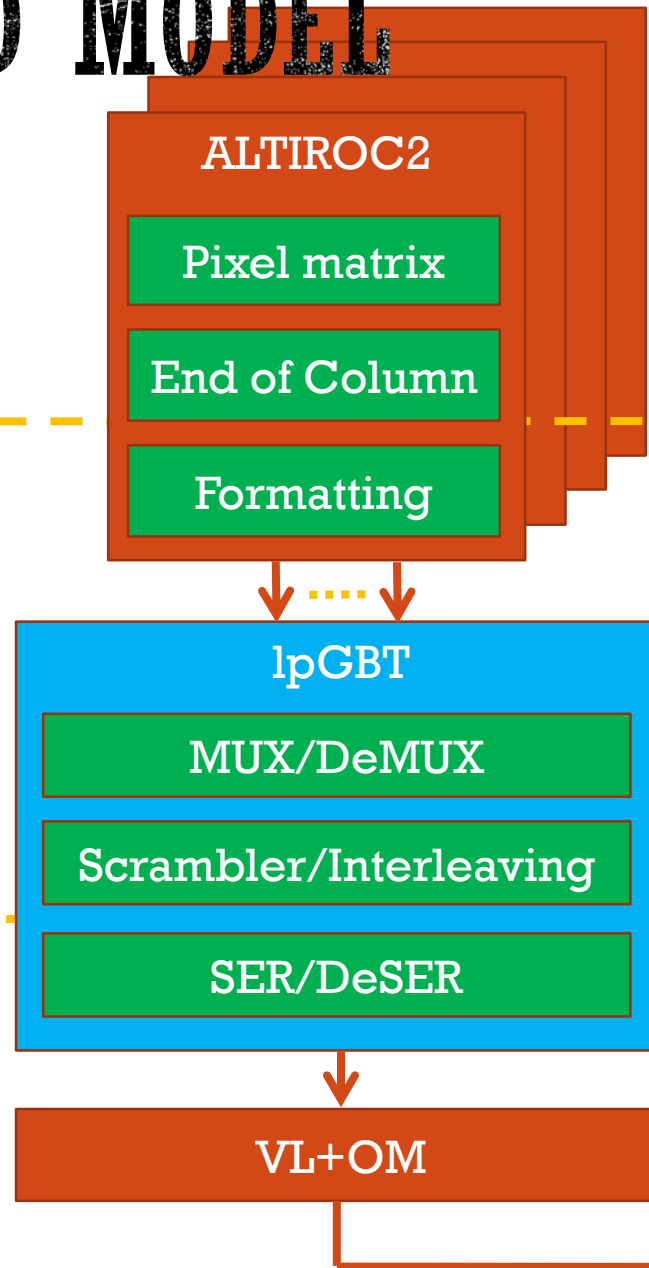
Packet

Data link Layer

Frame

Physical layer

Symbol

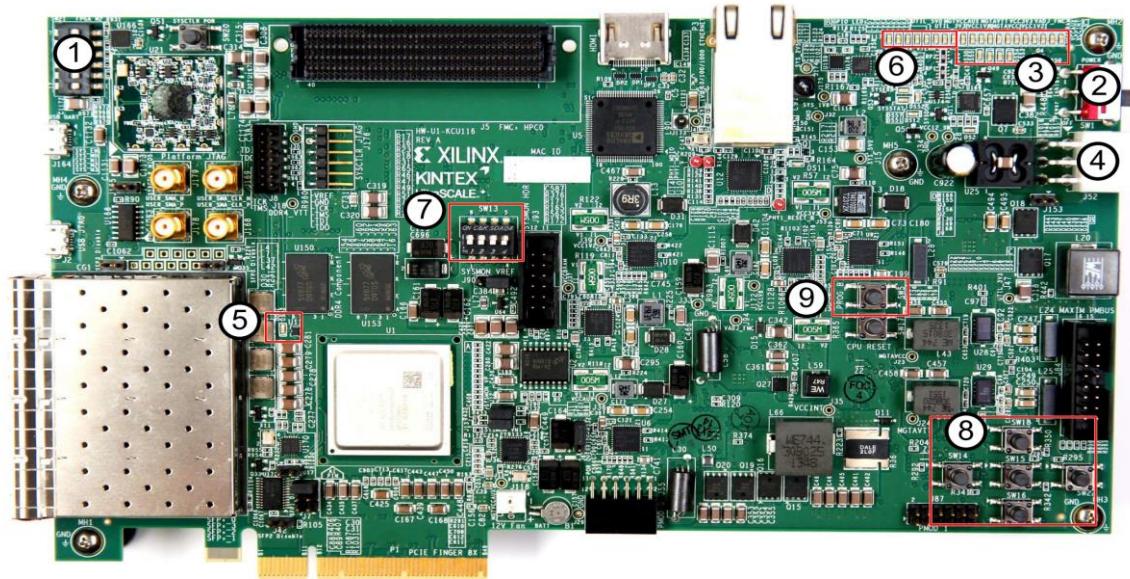


FELIX

DEMONSTRATOR



- The FPGA board with Kintex/Virtex Ultrascale or Kintex/Virtex Ultrascale plus
 - The IO block should support 1.28 Gbps
- Example:



KCUI16

PROBLEMS NEED TO BE SOLVED



- Develop the RAM (random access memory) emulation model based on FPGA BlockRAM
- Replace the tristate logic (high-Z) to the multiplexer at the EOC (end of column)