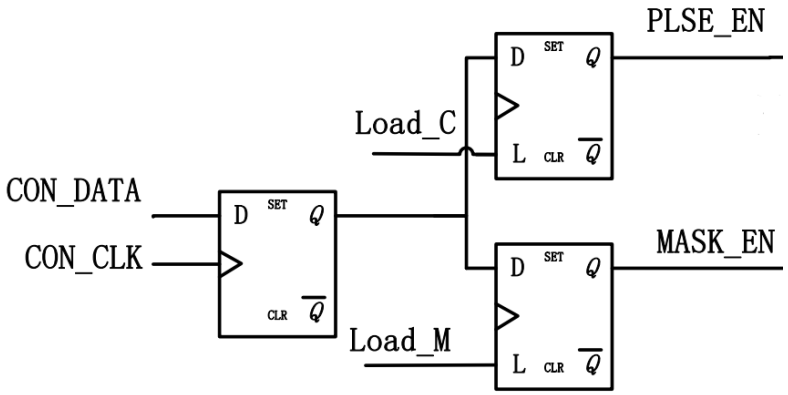
中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

# MPW1 UserManual

Ying ZHANG

# Configuration of Load_C and Load_M

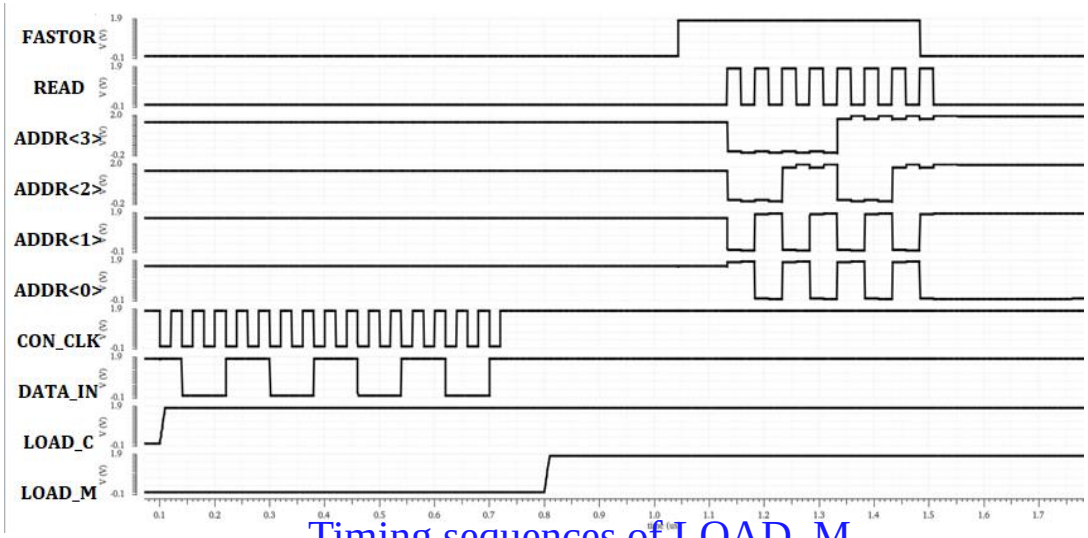
- **Load_C= loadc_internal | LOAD_C**
- **Load_M= loadm_internal | LOAD_M.**




Mask and calibration latch of each pixel

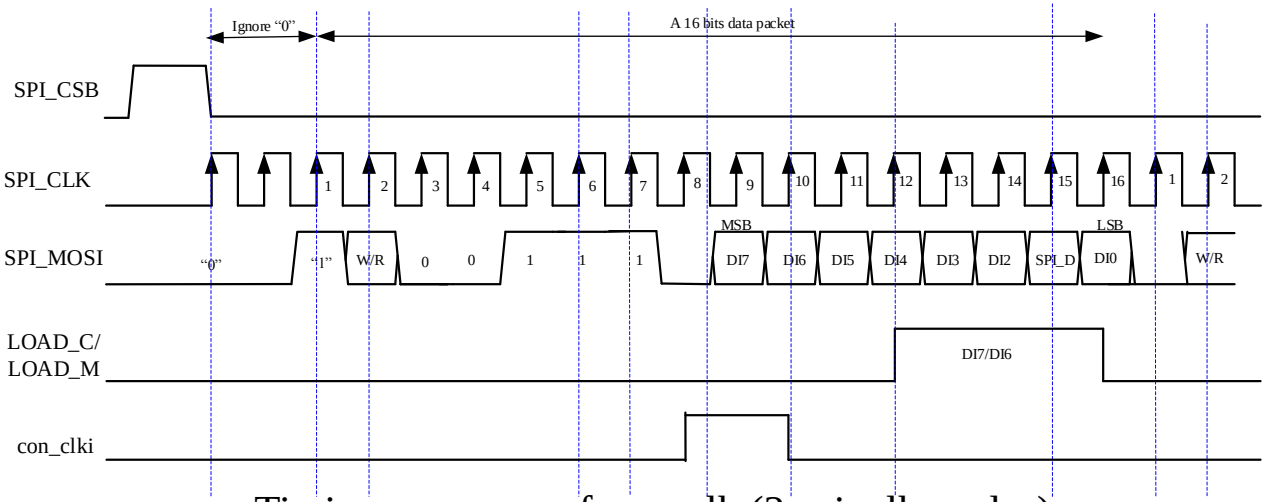
CON_DATA == 0 & Load_M =0, MASK_EN ==1 → to mask the pixel, Pixel state==0
CON_DATA == 0 & Load_C =0, PLSE_EN ==1 →inject an external pulse for calibration

# Timing sequences of Load_C and Load_M




Timing sequences of LOAD_M

from Tianya

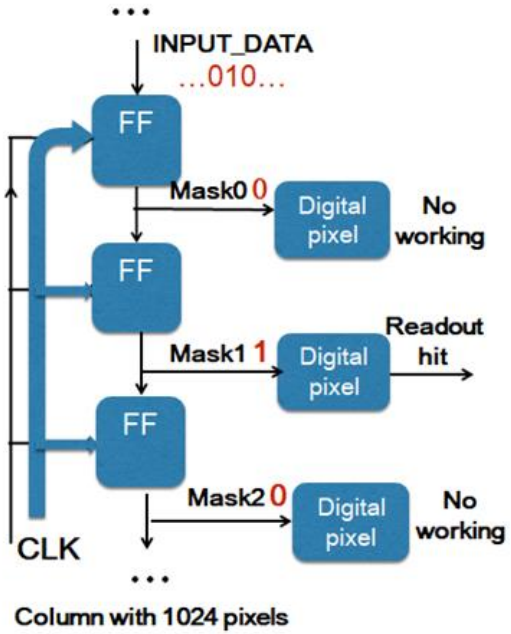



Timing sequence of con_clk (2 spi_clk cycles),
load_c/load_m (4 spi_clk cycles)

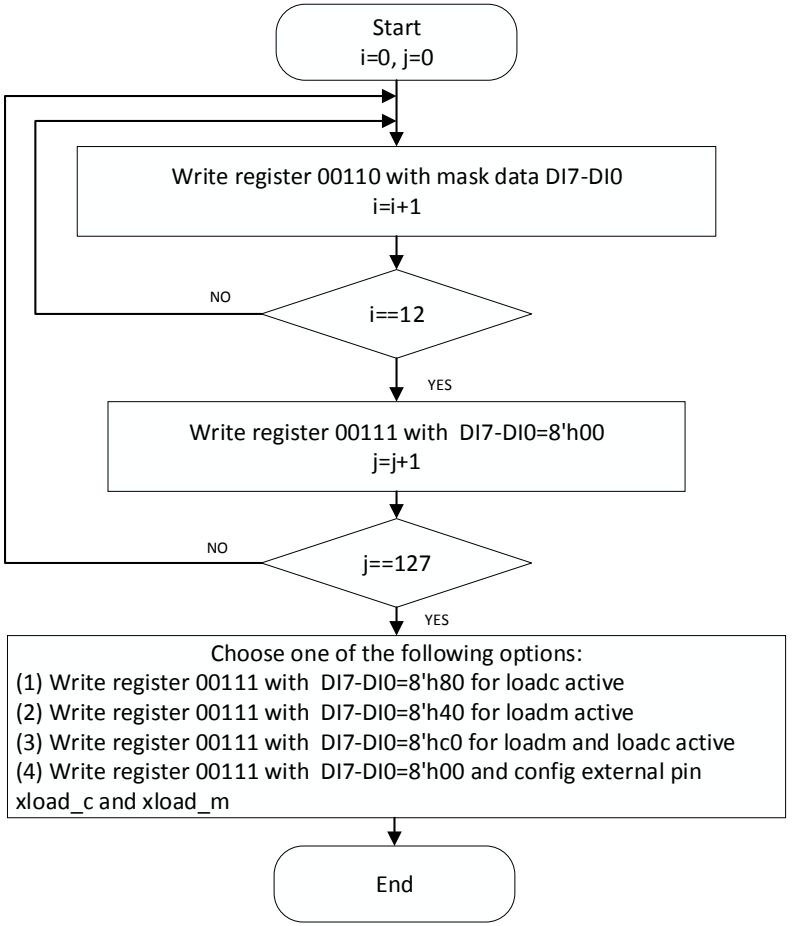
from Xiaomin

# Configuration of CON_DATA

One bit shifting register




Setting flow for pixel mask function




from Tianya

from Xiaomin

# DAC register setting

| No | Name | Description | Default |
|---|---|---|---|
| REG[0] | ENBGR | Bandgap enable | 1b |
| REG[3:1] | REG_BGR_OFFSET[2:0] | Bandgap output calibration | 100b |
| REG[4] | ENIBG | Ibias_gen output enable if bandgap esn't work | 1b |
| REG[12:5] | REG_CDAC0[7:0] | CDAC0 input code | |
| REG[13] | EN_CDAC[0] | CDAC0 enabl | |

from Zhang liang

| Register bit | Internal port name | Purpose | Description | Corresponding test Pad |
|---|---|---|---|---|
| REG[0] | ENBGR | Bandgap enable | 1'b1→ enable bandgap<br>1'b0→ disable bandgap<br>if bandgap has a problem | |
| REG[3:1] | G_BGR_OFFSET[2:0] | Bandgap output calibration | Nominal value 3'b100<br>→ Bandgap output VBG=0.75V<br>3'b101 → ?<br>3'b111 → 1.2 V | Pad #13, VBG_I0 |
| REG[4] | ENIBG | Enable the internal IBIAS_GEN block to generate a bias current for DACs if bandgap has a problem | If bandgap works, set ENIBG==1<br>If IBIAS_GEN needed, set ENIBG==0 | Pad #9, IPT_20U_IO for monitoring the generated current (nominal value is 20 μA) |
| REG[12:5] | REG_CDAC0[7:0] | CDAC0 input | To tune the current bias | Pad #10, TO_IO |

# DAC register setting

| | | | |
|---|---|---|---|
| REG[109:107] | REG_MUX[2:0] | 7 DACs to 1 ADC output | 000b |
| REG[111:110] | REG_MUXO[1:0] | Per ADC 3 to 1 output | 00b |

| MUX 7to1 | | MUX 4to1 | |
|---|---|---|---|
| 000 | AVSS | 00 | VDAC voltage test |
| 001 | VDAC1 | | |
| 010 | VDAC2 | 01 | VDAC/CDAC current test |
| 011 | VDAC3 | | |
| 100 | VDAC4 | 10 | VDAC/CDAC output voltage/current |
| 101 | CDAC0 | | |
| 110 | CDAC1 | 11 | Voltage reference for VDAC (0.8V) |
| 111 | CDAC2 | | |

Thanks for your attention !