Status of the Pixel Chip Design for high-rate CEPC Vertex Detector

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On behalf of the CEPC MOST2 Vertex detector design team

2019-8-21

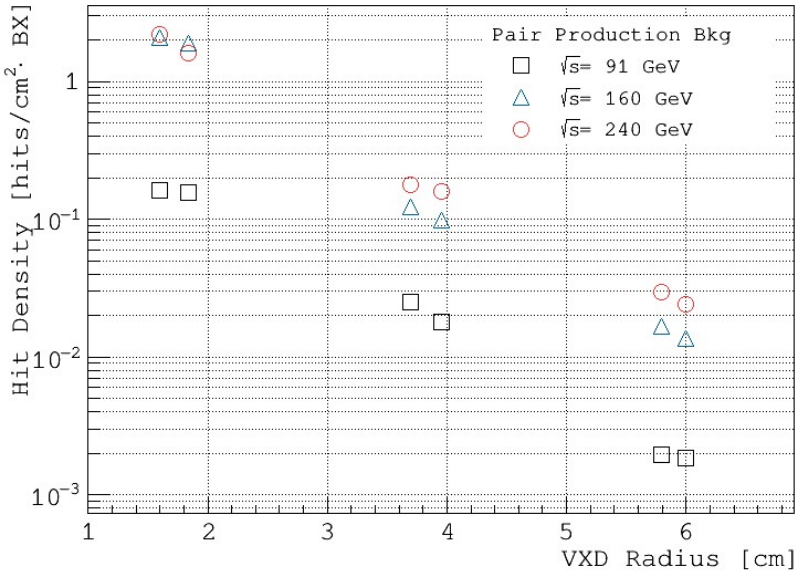
Outline

- **Status of the first MPW submission**
- **Status of the test preparation**
  - **Test board design**
  - **User manual**
- **Recent design status and plan**

Main specs of the full size chip for high rate vertex detector

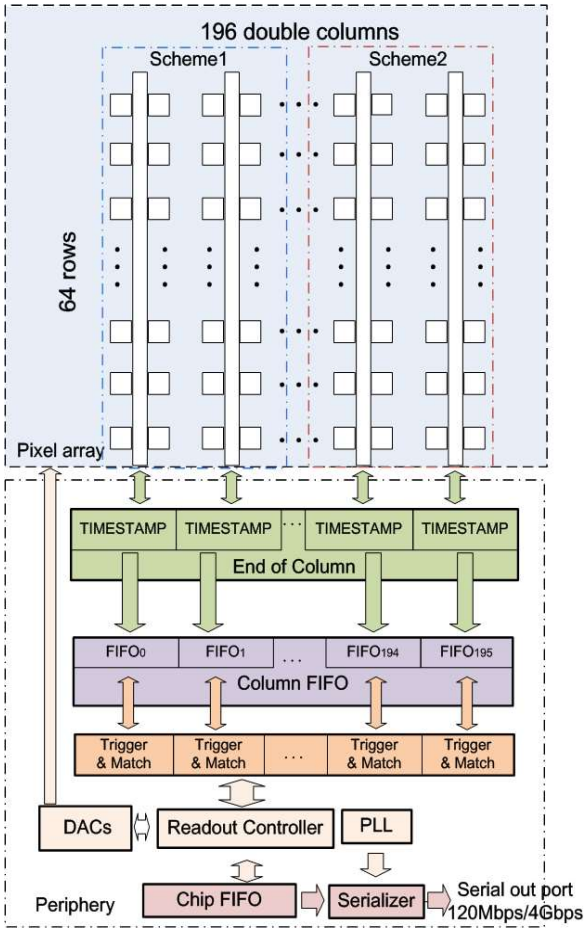
- **Bunch spacing**
  - **Higgs: 680ns; W: 210ns; Z: 25ns**
  - **Meaning 40M/s bunches (same as the ATLAS Vertex)**
- **Hit density**
  - **2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z**
- **Cluster size: 3pixels/hit**
  - **Epi- layer thickness：~18μm**
  - **Pixel size：25μm×25μm**

From the CDR of CEPC

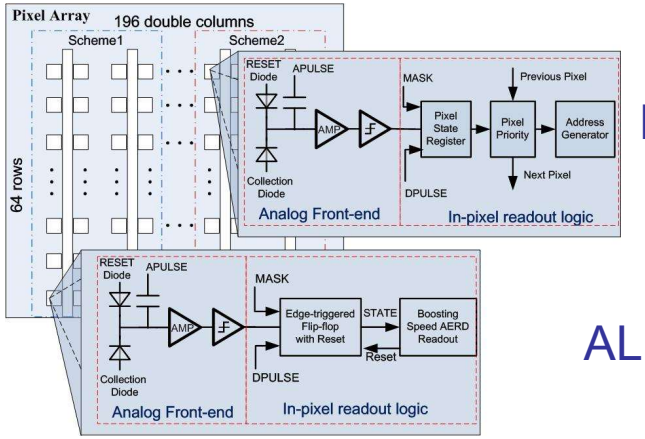


For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm^2 (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm

New proposed architecture for MOST2



From Tianya Wu in User Manual

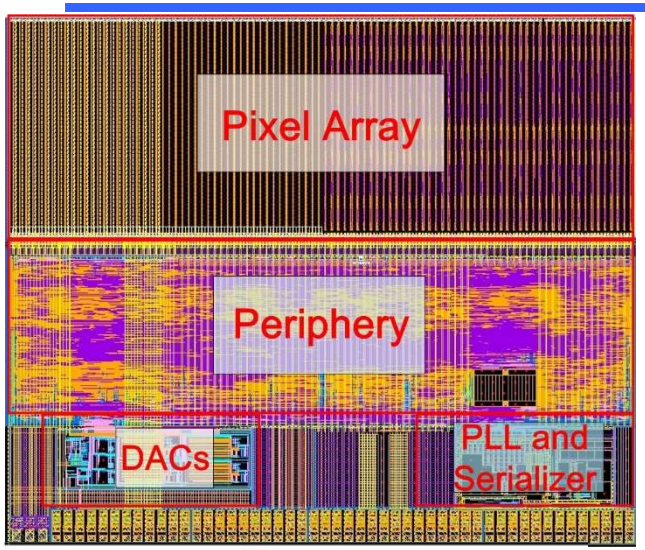


FE-I3-like Pixel

ALPIDE-like Pixel

- **Similar to the ATLAS ITK readout architecture: "column-drain" readout**
  - **Priority based data driven readout**
  - **Modification: time stamp is added at EOC whenever a new fast-or busy signal is received**
  - **Dead time: 2 clk for each pixel (50ns @40MHz clk), negligible compared to the average hit rate**
- **2-level FIFO architecture**
  - **L1 FIFO: In column level, to de-randomize the injecting charge**
  - **L2 FIFO: Chip level, to match the in/out data rate between the core and interface**
- **Trigger readout**
  - **Make the data rate in a reasonable range**
  - **Data coincidence by time stamp, only matched event will be readout**

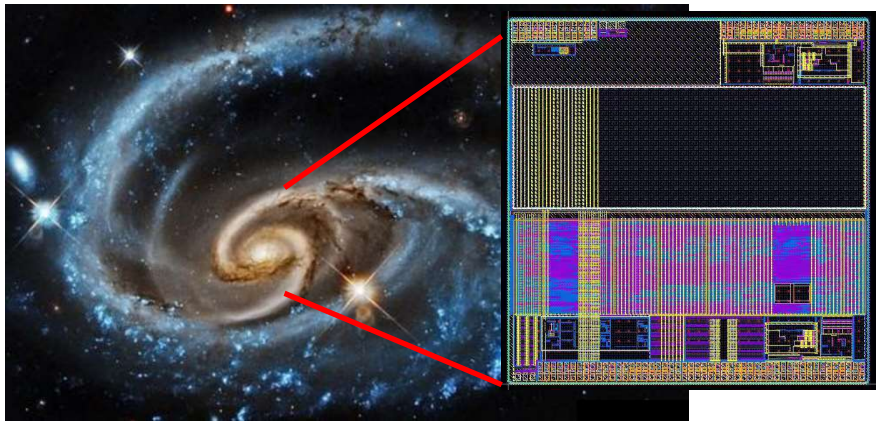
Chip Status



Chip size：5mm×5mm
Pixel size：25μm×25μm

- First MPW tapeout was submitted in June
  - Thanks IFAE for their tunnel for submission to TJ
- Expected to be delivered on Sep. 26
  - With 60 chips
- One block area of 5mm×5mm was fully occupied
  - A full functional pixel array (small scale)
    - 85% of the block area
    - A 64×192 Pixel array + Periphery + PLL + Serializer
    - Bias generation included
    - I/O arranged in one edge, as the final chip
  - other independent test blocks (less critical)
    - LDO + PLL
- It was supposed that we can use both standard and modified TJ process to make two parallel chip fabrications, but we failed at last, due to the too complicated paperwork
  - At least we see the chance to use modified TJ

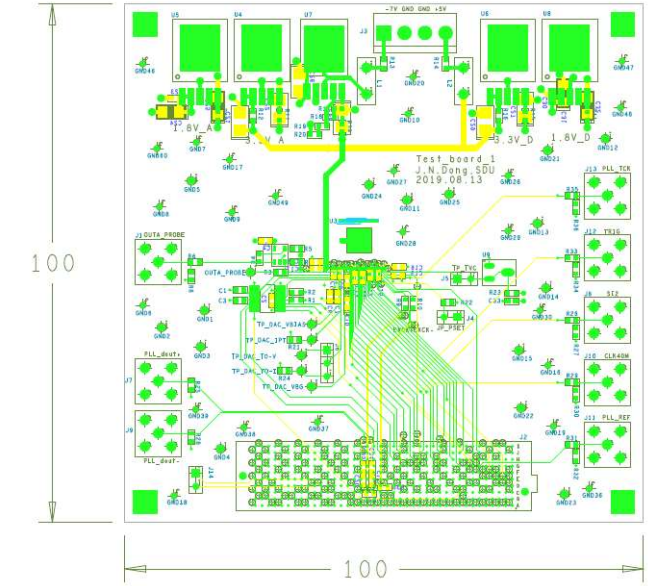
The chip got her name

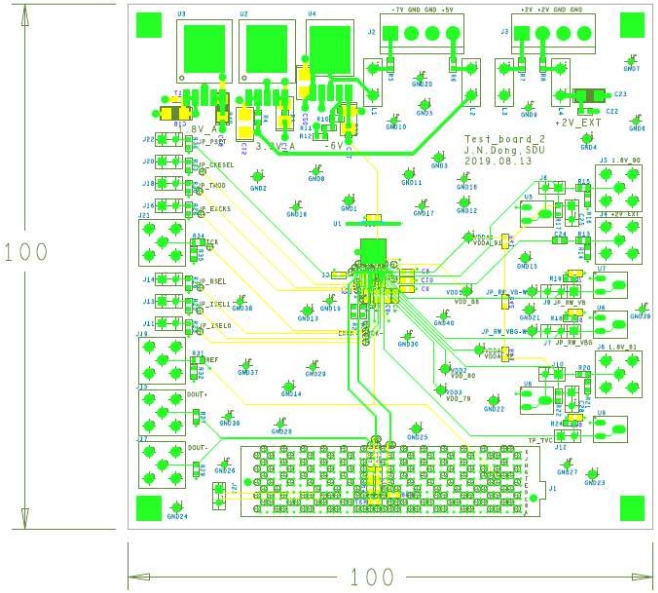


	MAC	CePix	CEPAS	Appollo	Zhulong(烛龙)	ChongMing(重明)	Baize(白泽)	TanCeQi(探测器)	TaiChu(太初)	TaiChuShenYan(太初神眼)	HuoYanJinGang(火眼金刚)	XiZhao(晞照)	ZhaoYaoJing(照妖镜)
13 participants	✔0	✔5	✔0	✔0	✔1	✔9	✔1	✔2	✔7	✔1	✔0	✔2	✔0
Wei Wei													
Ying Zhang		✔							✔				
Weiguo Lu		✔				✔							
Liang Zhang						✔			✔				
WANG Jia						✔				✔		✔	
Mei Zhao		✔				✔			✔				
Zhijun Liang						✔							
xiao min		✔					✔		✔				
ranzheng									✔				
Tianya Wu						✔			✔			✔	
Tian Xingcheng		✔											
Wu Kewei						✔		✔					
Li Xiaoting						✔			✔				
Wei Wei					✔	✔		✔					

- The chip was named as TaichuPix1
- Taichu (太初) means the very beginning of the world. As CEPC is exploring the origin of the matter， TaichuPix will act as her eyes
- To name the chip, we collected ~12 nominations and made a doodle
  - ChoMin（重明）,Taichu（太初），and CePix were the most voted names
  - We chose TaichuPix to be name

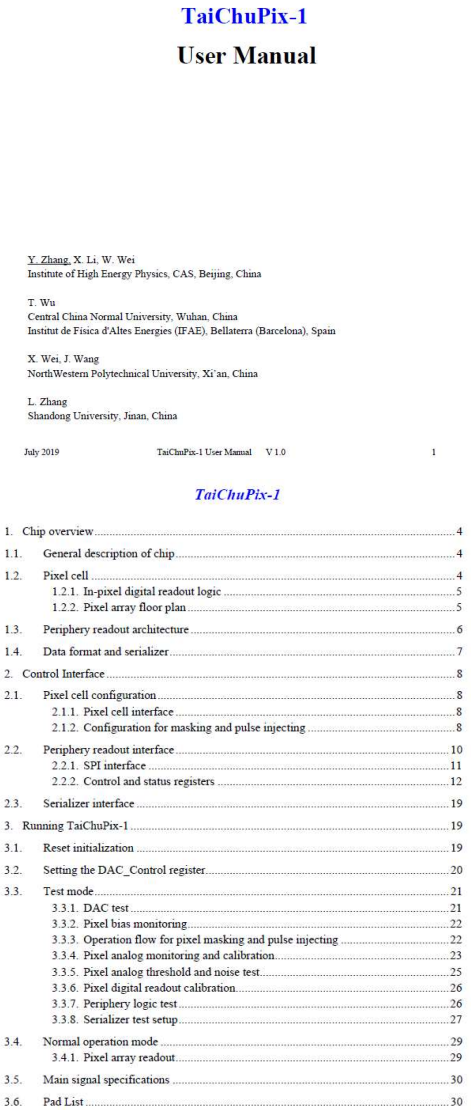
Test board is about to submit





- Two test boards design completed recently by SDU
  - One to test the main chip will full test features
  - The other to test building blocks (LDO+PLL)
- They will be submit for fabrication very soon (~3weeks)
- Common interface to KC705 FPGA Evaluation Board
  - The Eva board is also commonly used worldwide
- 30 main boards + 20 block boards will be fabricated for the first batch
- IHEP, IFAE expressed interests for FPGA test coding

User manual of the chip



TaiChuPix-1

User Manual

Y. Zhang, X. Li, W. Wei
Institute of High Energy Physics, CAS, Beijing, China

T. Wu
Central China Normal University, Wuhan, China
Institut de Fisica d'Altes Energies (IFAE), Bellaterra (Barcelona), Spain

X. Wei, J. Wang
NorthWestern Polytechnical University, Xi'an, China

L. Zhang
Shandong University, Jinan, China

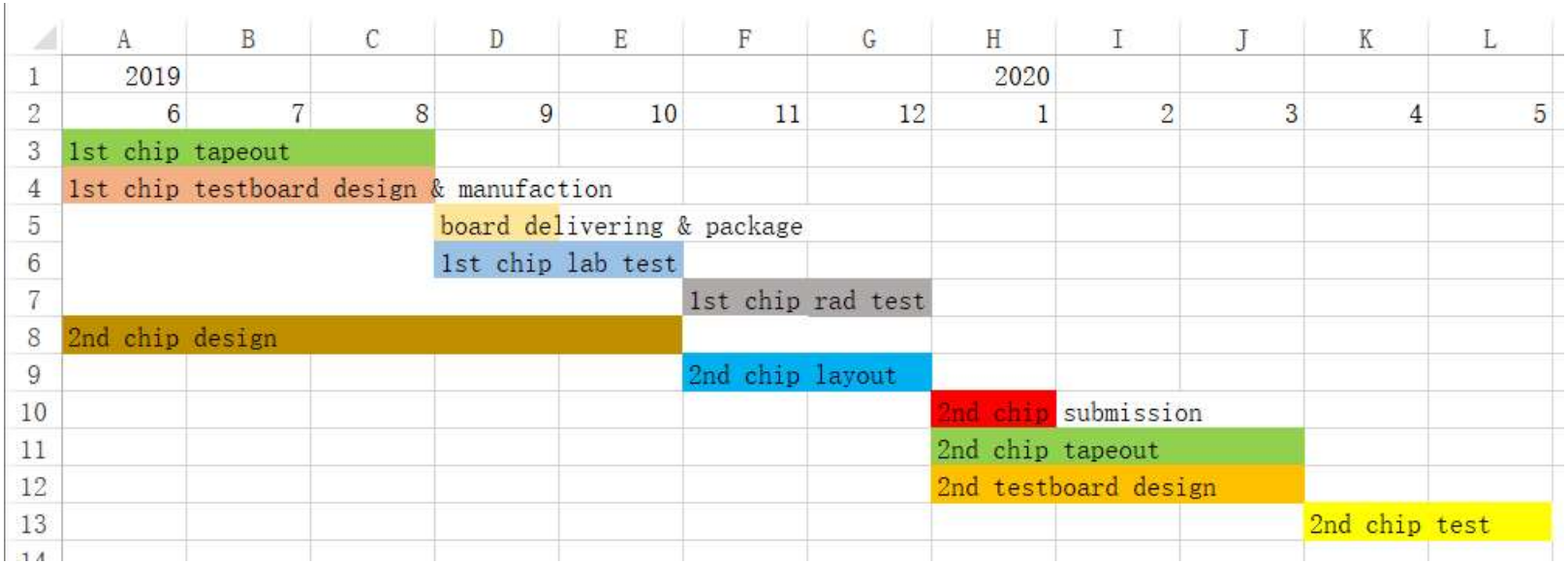
TaiChuPix-1

- **Detailed user manual for test and users was completed by the corresponded designer**
- **All were collected and edited by Zhang Ying**
- **About to release**

Recent chip design status

- **Possible improvements and optimizations for the next version were proposed and discussed**
  - **Design is progressing according to those directions**
- **Optimization directions**
  - **Readout scheme**
    - **To make larger headroom for the timing**
      - **Data latching @ 1clk -> 1.5clk**
  - **Area optimization**
    - **Compress the size of periphery and others + pad**
    - **Smaller pixel size**
  - **Data interface finalization**
    - **Serializer frequency and data stream protocol**
  - **Design refine**
    - **High-Z state elimination, address latch, dynamic DFF enhancement …**

Proposal for the schedule of the next version



- **Goals for this year:**
  - **submit the 2nd MPW prototype, complete the 2nd prototype test**
  - **Deadline: 2020. 5**
- **Estimated date for the 2nd MPW tapeout:**
  - **2019.12.31**
- **Potential problems**
  - **The design of 2nd MPW will start in parallel and without the test results from 1st MPW**

Thank you !

Ladder Prototype

Silicon Vertex Detector Prototype – MOST (2018–2023)

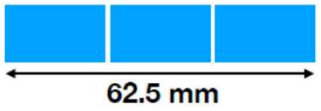
Sensor technology CMOS TowerJazz

- Design sensor with large area and high resolution
- Integration of front-end electronic on sensor chip

Benefit from MOST 1 research program

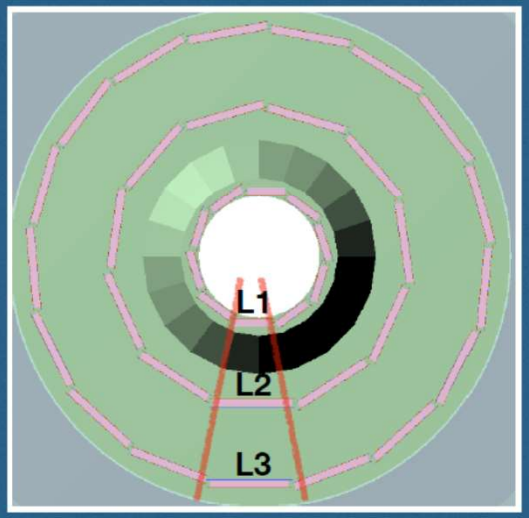
Double sided ladder

Layer 1 (11 mm x 62.5 mm)
Chip size: 11 mm X 20.8 mm



3 X 2 layer = 6 chips

3-layer sector



Baseline MOST2 goal:
3-layer prototype

Default layout requires different size ladders

Keep it simple for baseline design

L1
L2
L3

3-layers
same size
same chip

Goals:
1 MRad TID
3-5μm SP resolution

Integrate electronics readout

Design and produce light and rigid support structures

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- Ref: Introduction to the Pixel MOST2 Project, Joao Costa, 2018.6

Team organization

- Slides from Y. Zhang, Satellite meeting of MOST2 in Oxford, 2019.4

- **Design team:**
  - **IHEP, SDU, NWPU, IFAE & CCNU**
  - **Biweekly/weekly video design meeting on chip design (convened by IHEP)**

Institutes	Tasks	Designers
IHEP	Full chip modeling & simulation Pixel Analog, TCAD simulation High speed interface: PLL + Serializer	Wei Wei, Ying Zhang Xiaoting Li, Weiguo Lu, Mei Zhao
CCNU/IFAE	Pixel Digital	Tianya Wu, Raimon Casanova
NWPU	Periphery Logic, LDO	Xiaomin Wei, Jia Wang
SDU	Bias generation	Liang Zhang

- **Chip characterization**
  - **Test system development: SDU & + other interested parties**
  - **Electrical test: all designers supposed to be involved in the related module + other interested parties**
  - **Irradiation test: X-ray irradiator + beam line**