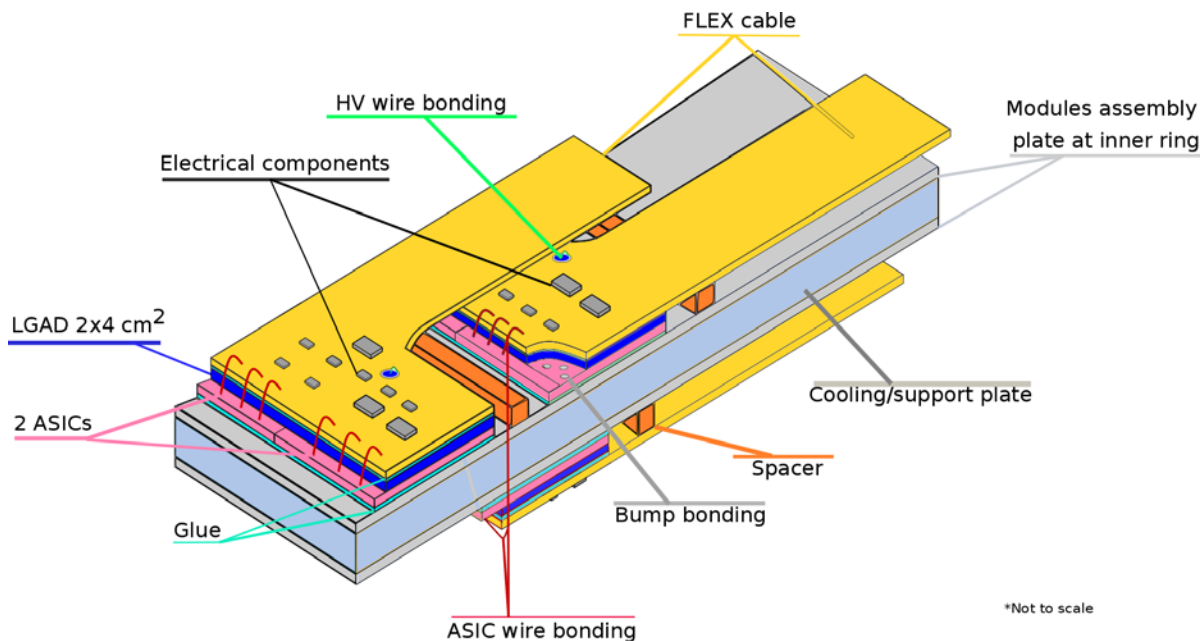# Discussion on flex cable

Mingyi Dong

2019.8.22

Module Flex cable

- Module flex cable is for all connections between the ASIC and the peripheral electronics
- The bare module is glued to the back side of the sensor with accurate positioning on the flex modules
- All the signals are wire bonded between the ASIC and the flex cable （HV between sensor and the flex cable）
- Connectors are used between the flex cable and the peripheral electronics

FLEX cable

HV wire bonding

Electrical components

Modules assembly plate at inner ring

LGAD 2x4 cm^2

2 ASICs

Cooling/support plate

Glue

Spacer

Bump bonding

ASIC wire bonding

*Not to scale

L shape design to reduce the total thickness of the flex cables

A maximum of 10 flex cables is stacked.

Type and Number of lines

From TDR

Signal name	Signal type	No. of wires	Comments
HV	1 kV max.	1	Clearance
POWER	$1 \times$ Vdda, $1 \times$ Vddd, 1.2 V	2	2 planes, $R < 2.7\,\mathrm{m}\Omega\,\mathrm{cm}^{-1}$
GROUND	Analog, Digital	1(2) plane(s)	Dedicated layer $R < 0.7\,\mathrm{m}\Omega\,\mathrm{cm}^{-1}$
Slow control	Data, Ck (opt. + rst, error)	2 to 4	$\mathrm{I}^2\mathrm{C}$ link
Input clocks	320 MHz, Fast command e-link (opt. 40 MHz (L1))	4 or 8	CLPS
Data out lines	Readout data (TOT, TOA, Lumi)	4 pairs	4 e-links differential CLPS
ASIC reset	ASIC_rst	1	Digital
Monitoring	Temperature, Vdda, Vddd	6	DC voltage
Debugging	ASIC_debug	2	Analog

- HV : 1
- Other lines

# Type and Number of lines

From Maria Robles Manzano, JuanAn

Signal name	Signal type	No. of wires	Comments
HV	1 kV max.	1	Clearance
POWER	$1\times$ Vdda, $1\times$ Vddd, 1.2V	2	2 planes, R < 2.7mΩcm^{-1}
GROUND	Analog, Digital	2 planes	Dedicated layer R < 0.7mΩcm^{-1}
Slow control	Data, Ck (opt. + rst, error)	2 or 4 single line	I^{2}C link
Input clocks	320 MHz, Fast command e-link(opt. 40MHz (L1))	2(differential pair) 2(differential pair)	CLPS
Data out lines	Readout data (TOT, TOA, Lumi)	4 differential pairs (2 for lumi data, 2 for time data)	4 e-links differential CLPS
ASIC reset	ASIC_rst	1	Digital
Monitoring	Temperature, Vdda, Vddd	6 (3 / ASIC)	DC voltage
Debugging	ASIC_debug	1 (common/ 2 ASICS)	Analog

Key points

- HV: 1 kV max.
  - Excellent Insulation , shielding
- Different Length: max. 750mm, (min. 250mm)
  - Signal attenuation
- Speed of the data transmission
  - 1.28Gbit s^{-1} for the inner radius
  - 320Mbit s^{-1} for the outer radius
- ASIC power supplies (1.2V)
  - a strong constraint on the flex plane resistance
  - To minimize the voltage drop and the power dissipation (< 200mΩ, / 2.7mΩcm^{-1}) for the longest cable
- Connectors
  - local additional enhanced plate for connectors

Make samples of the old version

- Four-layer design, L-shape
- A width of 39.5mm for module region, and A width of 19mm for the tail
- Length: 750mm, thickness: <350μm
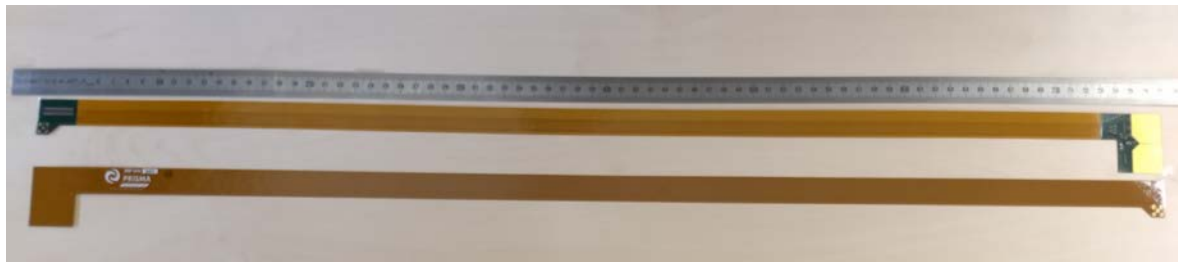
- Already contacted the ShenNan compony in China
- Sent the gerber files from Marisol Robles from Mainz University
- 20 pieces will be made

- Have some discussion, and waiting for the feedback (quotation) from the company

Discussion

- Components on the flex cables

- How to test them after we get the samples?
  - The university Mainz has the test system

- New design