Power consumption of digital pixel

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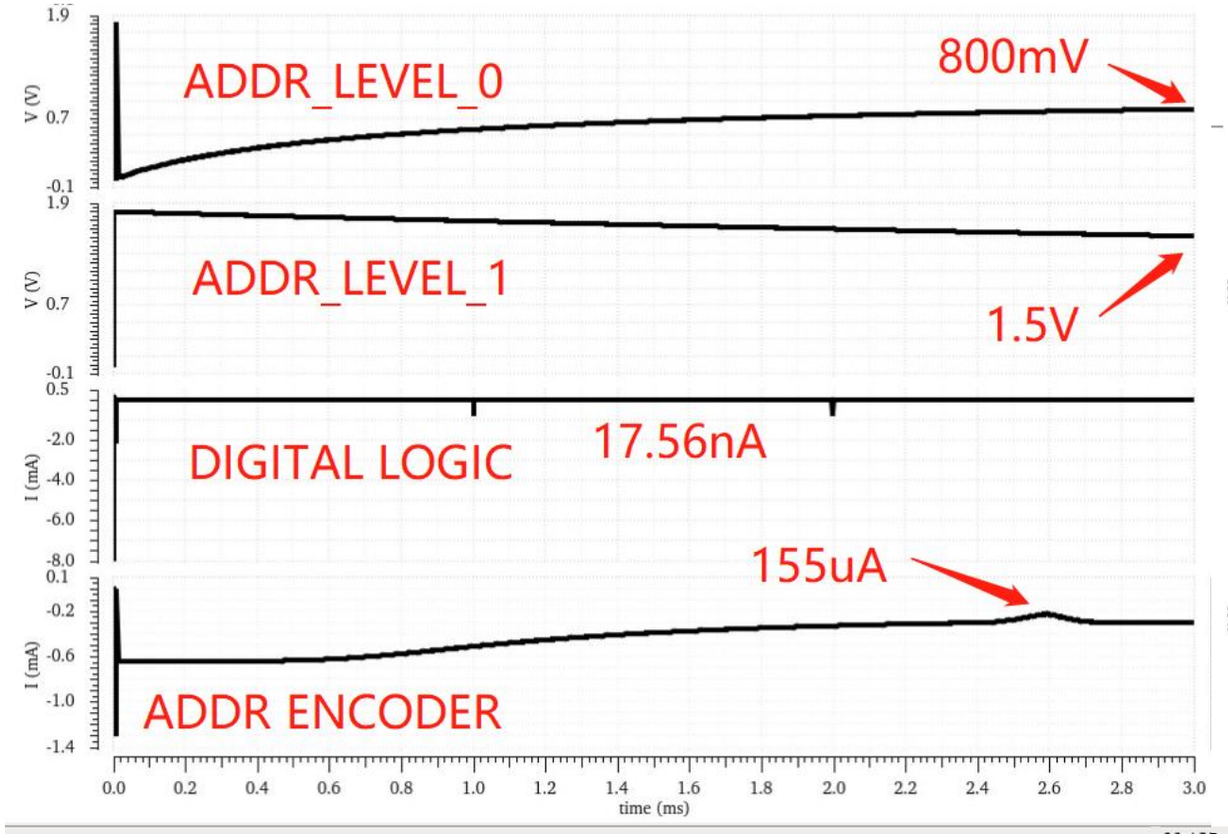
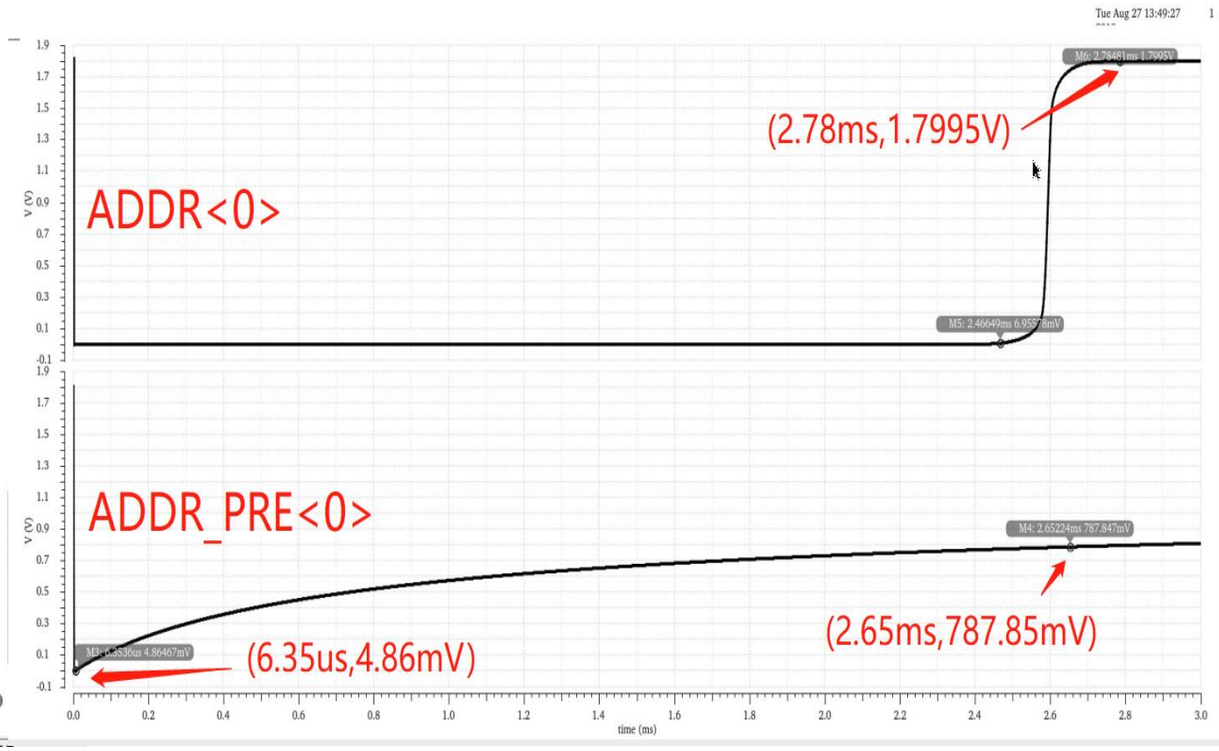
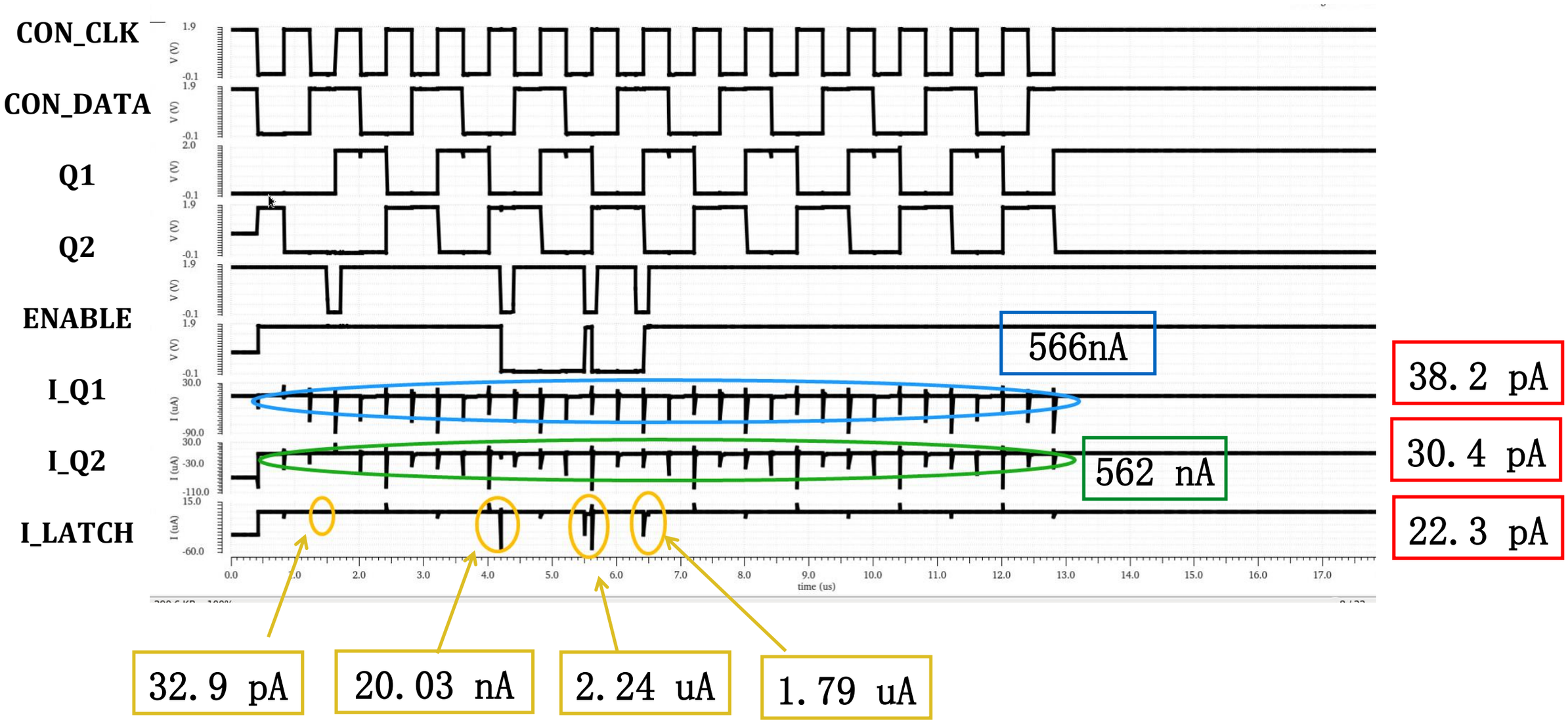
Power dissipation of in-pixel readout





- This is schematic level simulation of general trend of the transient current.
- Simulation stop at 3ms.
- The static current of FE-I3 digital logic is stable at 17.56 nA, but the current of address encoder is rising.
- The rising output voltage of address encoder lead to the inverse of buffer and cause the increase of current

Power dissipation of in-pixel readout



- This is schematic level simulation of DFF and LATCH
- Simulation stop at 3ms.
- The static current of Q1, Q2 and ENABLE are 38.2pA,30.4pA and 22.3pA respectively
- The average current is different for LATCH when it works in a different situation

Thanks for your attention.