Status of digital pixel

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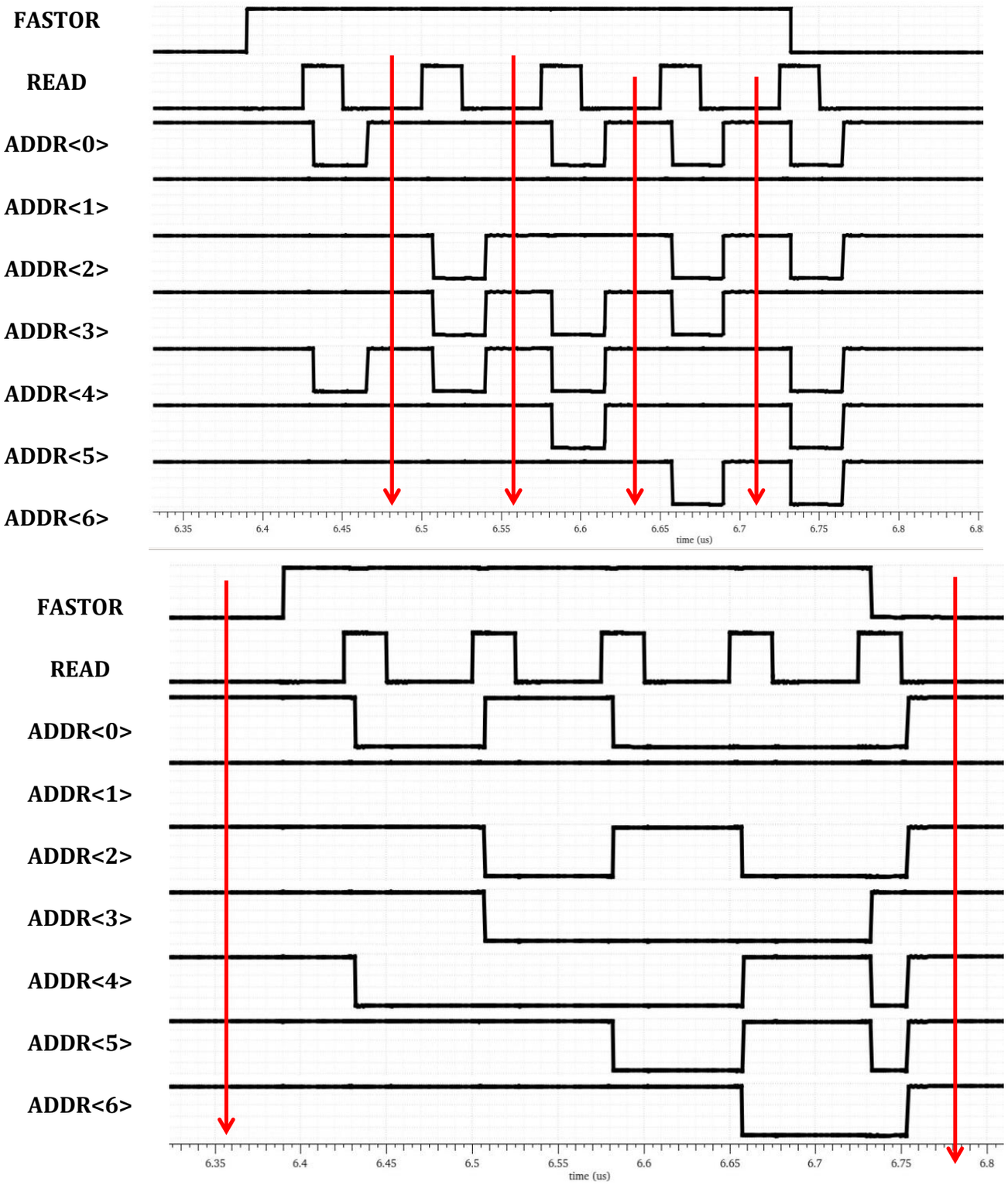
Verification of solution of FE-I3 high-z

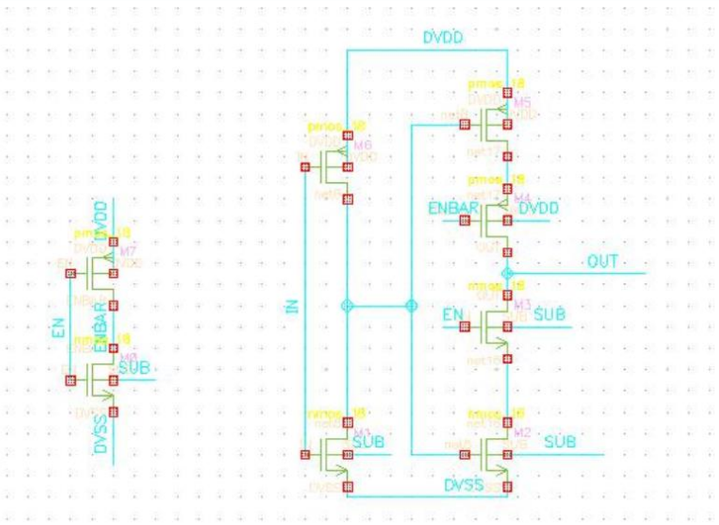


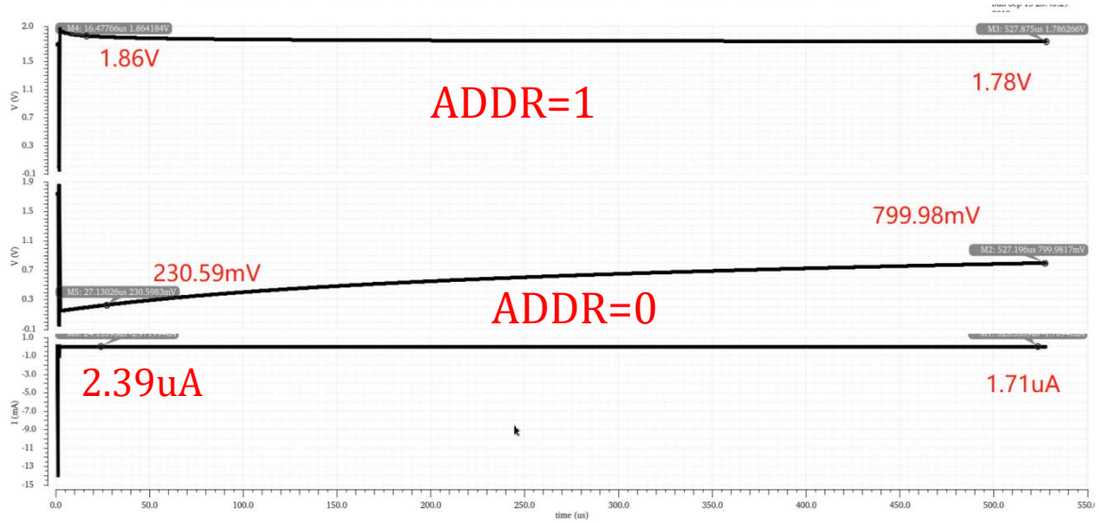
This is the schematic level simulation of FE-I3, the top one connected the pull-up cell without controlling signal, address encoder will be a refresh to the high level before next hit.

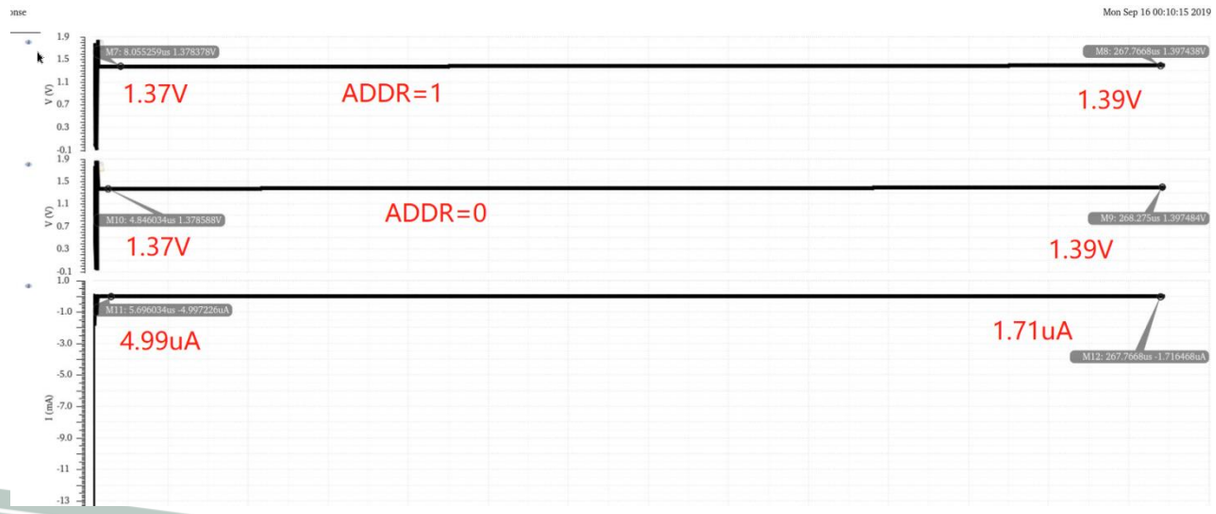
The bottom one connect the pull-up cell with the FASTOR as the controlling signal. The final hit will be last for 21ns more after FASTOR shut down.

The static current of digital pixel is 18.6nA. And it is 1.447uA for address encoder. Total static power dissipation is 3.4mW/cm2

Verification of solution of ALPIDE high-z







This is the schematic level simulation of ALPIDE, the top one connected the pull-up cell only before the buffer. The voltage level of ADDR not stable, but the current is under control.(within 3uA)

The bottom one add the extra pull up cell after the buffer. And the voltage level of ADDR keeps at 1.4V.

The static current of digital pixel is around 1.7uA. Total static power dissipation is 3.96mW/cm2

Thanks for your attention.