New structure of digital pixel

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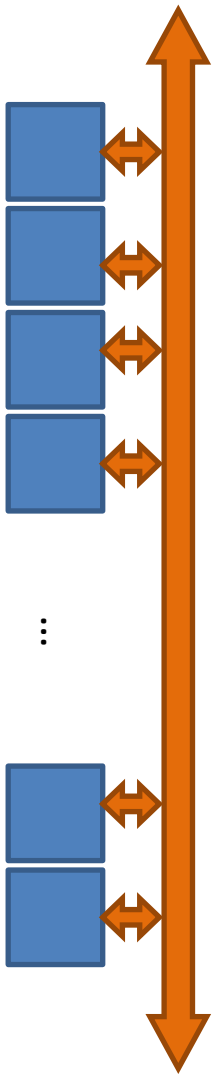
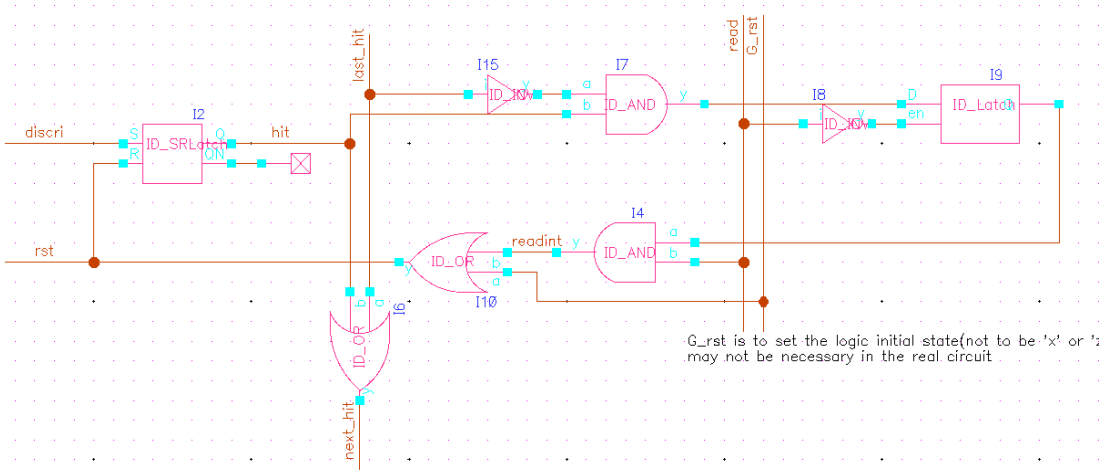
Column drain architecture

Single column

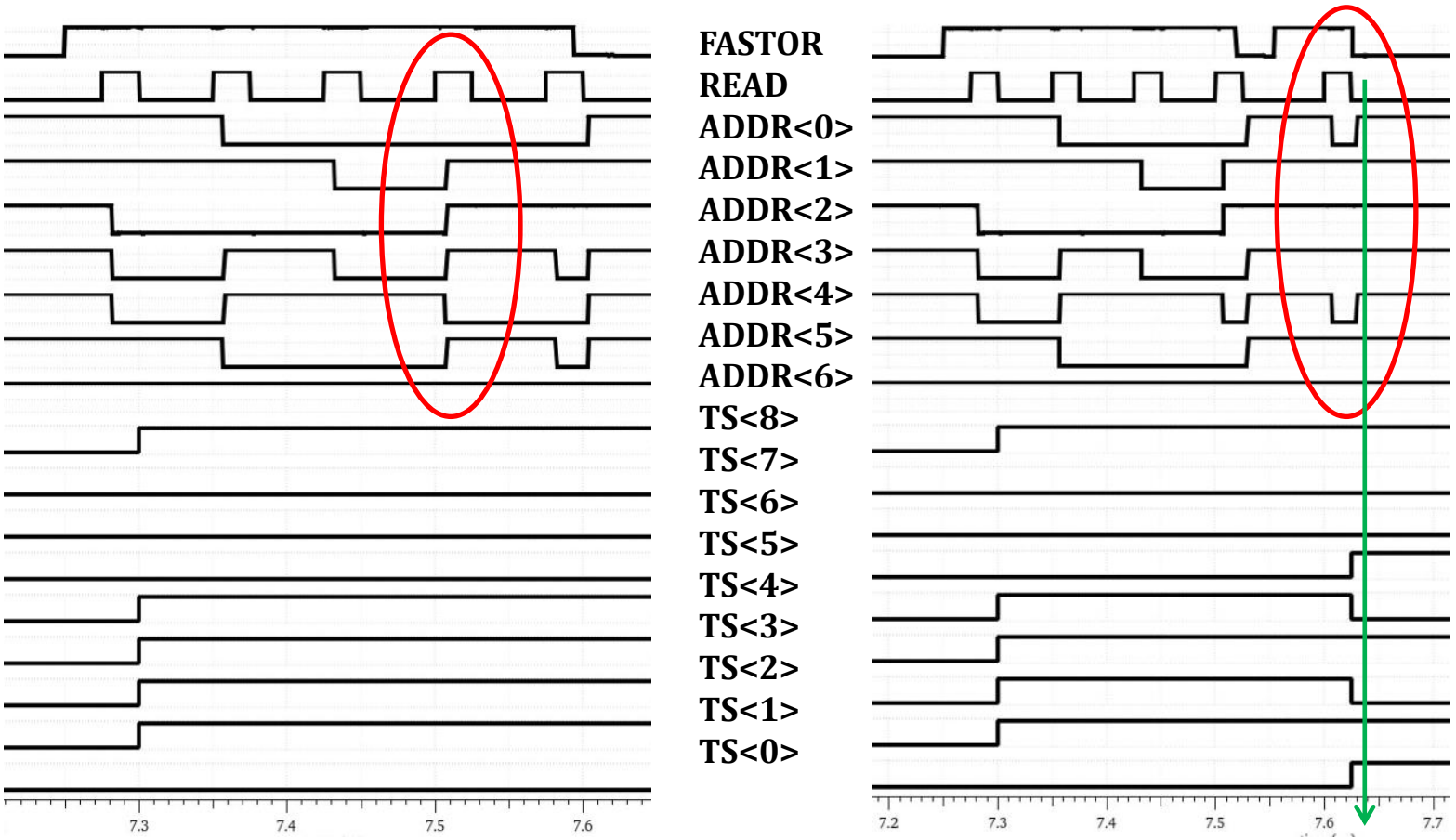


- FEI-3 column drain architecture:
  - HIT generation and reset
  - Priority arbitrary & Pixel readout
  - Latch to store time stamp when a hit is detected
- MOST2 limitations:
  - No room to store the time stamp
  - Time stamp added at the end of column
  - During the readout of a hit, no other hit can be detected (a wrong time stamp would be assigned)



Problem of column drain architecture

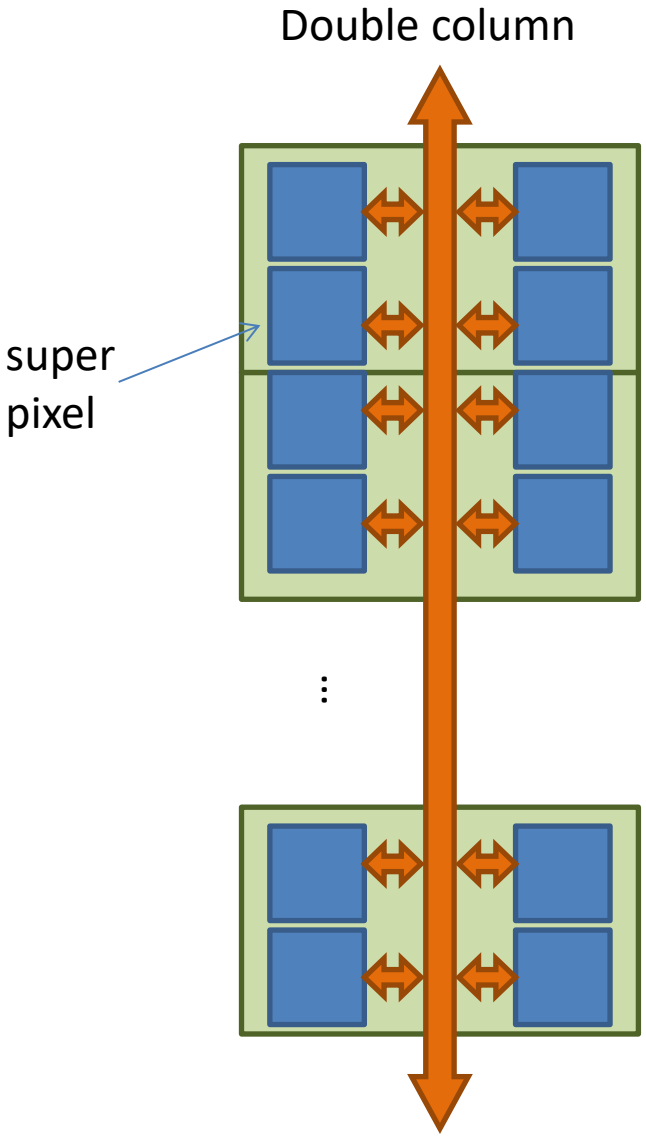
- Simulation condition: inject 4 random hits(index 70, 80,90,99) at the same moment, after a little while, give another hit at index110(the highest priority).



- The time spacing of Pixel<110> (ADDR[0:7]=1101110) is 200ns
- Timestamp(TS) is the same with the other four

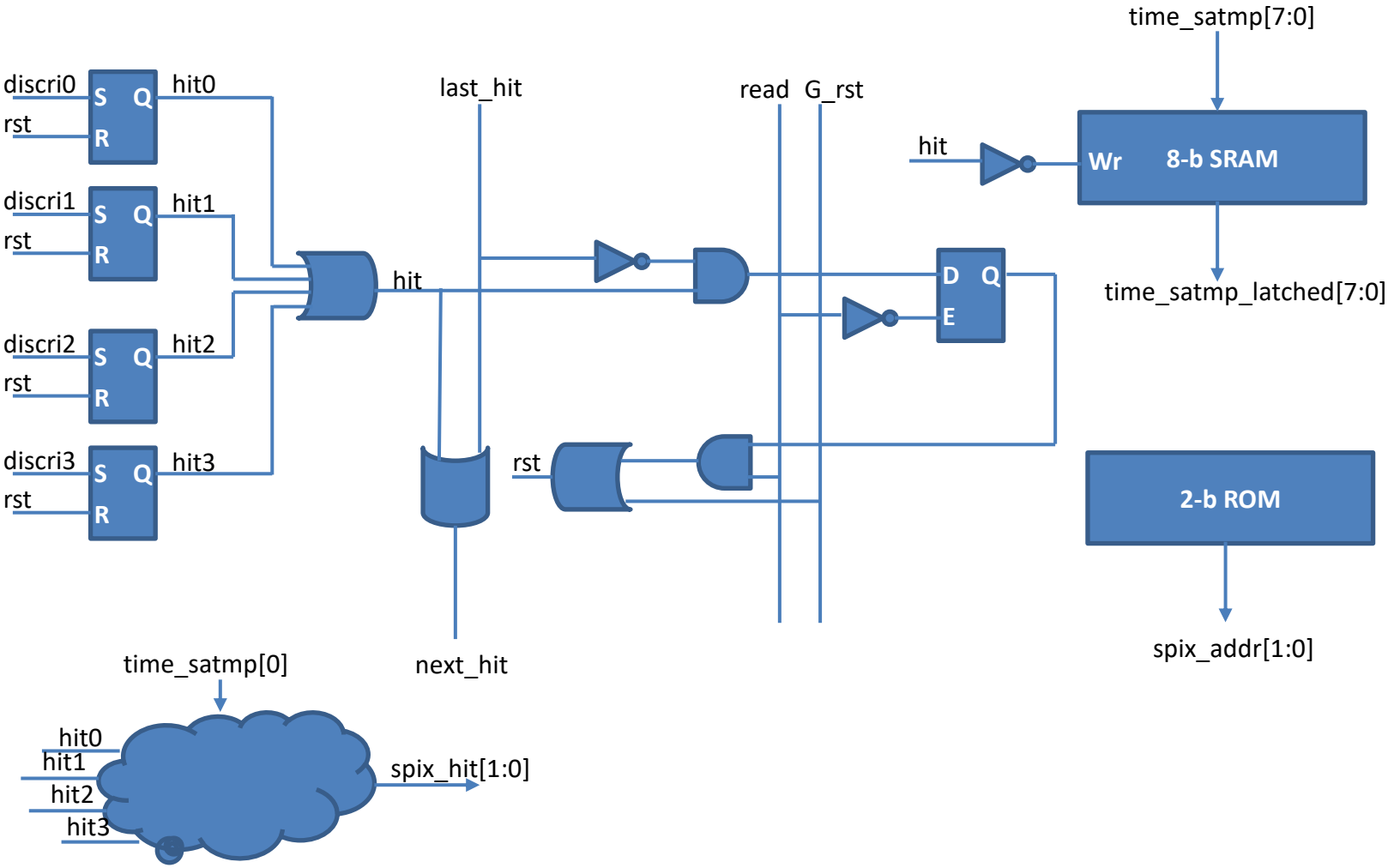
- The time spacing of Pixel<110> (ADDR[0:7]=1101110) is 300ns
- TS is different

Column drain architecture

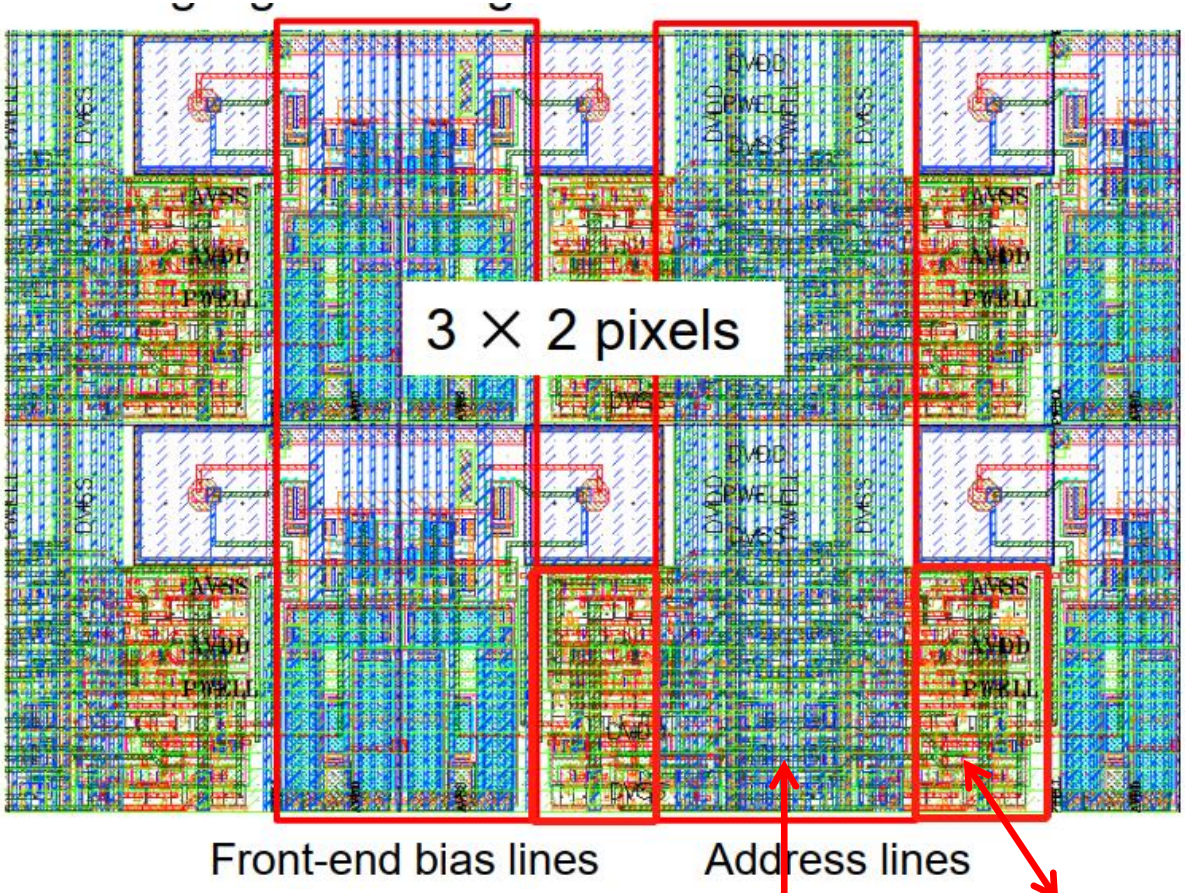


- Super pixel formed by to 4 pixels (2 rows, 2 columns)
- FEI3 logic shared between the 4 pixels:
  - Priority arbitrary & Pixel readout
  - Reset
  - Latch to store time stamp when a hit is detected (time_stamp_latched[7:0])
- HIT generation circuit per pixel
- 2-b register to indicate which of the 4 pixels were hit in the same bunch crossing (spix_hit[1:0])
- ROM address (spix_addr[1:0])
- Super pixel column drain architecture allows to capture different hits in different bunch crossing while reading pixels from the double column
- 2 buses:
  - Global time stamp
  - Pixel information: time_stamp_latched, spix_addr and spix_hit

Super pixel FEI3 shared logic



The evaluation of the area



The area of Super pixel:

- The address encoder is the same.(36 transistors)
- Share the in-pixel digital logic but keep the initialization part.(56transitors X4)
- 8bit RAM for timestamp.(6x8bitx4byte=192)
- Extra logic(?).

➢ Total:450+?

Thanks for your attention.