HERD - fi**B**re track**E**r readou**T** **A**sic (β)

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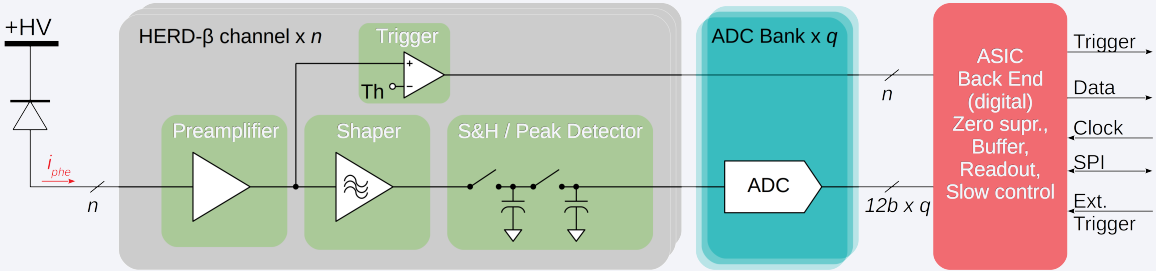
HERD-β specifications

Specification	Target
Channels	64 or 128
Input rate	1kHz max
Power draw	**0.3mW/ch**
Radiation hardness	80 Gray
Dynamic range	676 MIP (18748 phe) or 12 bits
Minimum detectable charge	0.1 MIP (2 phe)
On chip digitization and zero suppression	Minimum lines for data output
Slow control	SPI
V_{anode} adjust	500mV
SNR for calibration	> 10*
SNR for operation	> 5 (to set 3.5phe threshold)

* Challenging with 10x10μm cell size

HERD-β architecture

- Classical analog processing:
  - –Preamplifier
  - –Shaper
  - –Peak-detect
- Few ADCs shared among channels
- Digital Back End for communications and control

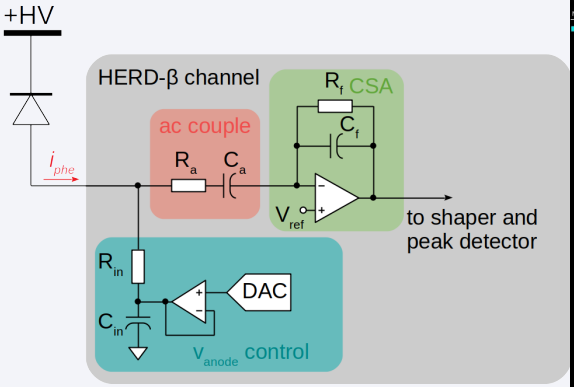


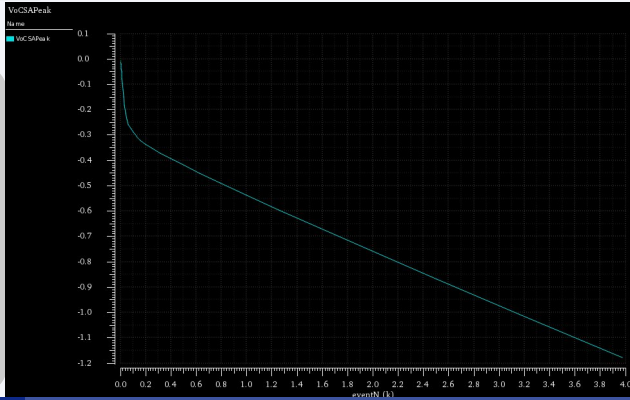
HERD-β initial simulations

Challenging preamplifier

Large current drawn by V_{anode} control and low power.
At least 2V capable input for adjust of $\approx$ 500mV.
Low noise and low power CSA.

Dynamic Compression of the signal in CSA using MOS cap in feedback.
Noise with ideal components at the limit for 1phe.
Simulation of CSA peak with input from 1 to 4000 fired cells:





HERD-β schedule

Tentative aggressive schedule!