New structure of digital pixel evaluation

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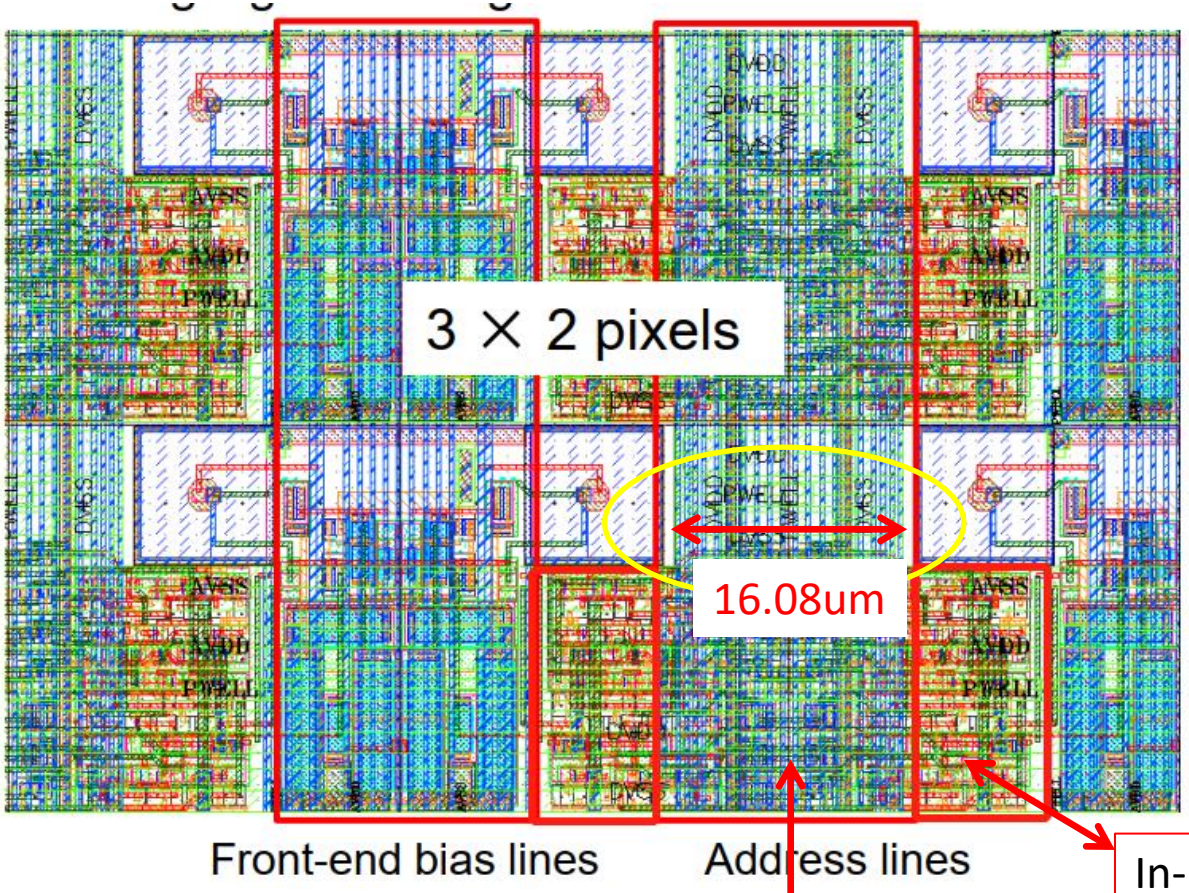
The evaluation of the area(Matrix size:512x1024)



The area of Super pixel:

- The address encoder is the same.(36 transistors)
- Share the in-pixel digital logic but keep the initialization part.(56transitors X4)
- 8bit RAM(Dynamic Latch) for timestamp.(6x8bit=48)
- Extra logic(?).

➢ Total:308+?< 440

The evaluation of the area(Matrix size:512x1024)

Total space for bus routing is 16.08um, the minimum width of M4 is 0.28um, the minimum space between two metal line is 0.28um.
Only 28 buses can survive.

	Current Metal line(M4)	Super Pixel Metal line
ADDRESS READOUT	10	10
TIMESTAMP	0	8x2
Initialization Calibration (Apulse/Dpulse/Load..)	4	4
Readout trigger (Fastor/read/)	2	2
1 bit shifting register (CLK and Data)	2	2
Global Reset	1	1
Total Metal line	19	35
Total width (M4 with minimum width)	10.64um	19.6um

From the analysis of the table, we can easily conclude that the space can only satisfy 4 bit timestamp.

The evaluation of the power consumption

The dynamic latch is used to generate timestamp. And the RC model (1.6mm metal line: 460ohm, 400fF) is for power evaluation.
All the results come from the Timestamp latching phase.

Timestamp Metal line	The width and length of Metal line	Power consumption	Power of Latch
TS0 (CLK: 25ns)	0.28um X 1.6mm	35.61n	5.19u
TS1(CLK: 50ns)	0.28um X 1.6mm	35.54n	3.80u
TS2(CLK: 100ns)	0.28um X 1.6mm	35.59n	2.86u
TS3(CLK: 200ns)	0.28um X 1.6mm	26.06n	3.47u
TS4(CLK: 400ns)	0.28um X 1.6mm	35.59n	3.44u
TS5(CLK: 800ns)	0.28um X 1.6mm	22.71n	835.34n
TS6(CLK: 1600ns)	0.28um X 1.6mm	26.61n	736.04p
TS7(CLK: 3200ns)	0.28um X 1.6mm	26.62n	733.65p
Total		244.3nA	19.6uA

From the analysis of the table, the increasing current of Timestamp bus is around 20uA, which causes 46.7mW/cm2 of power density.

Thanks for your attention.