

New structure of digital pixel evaluation

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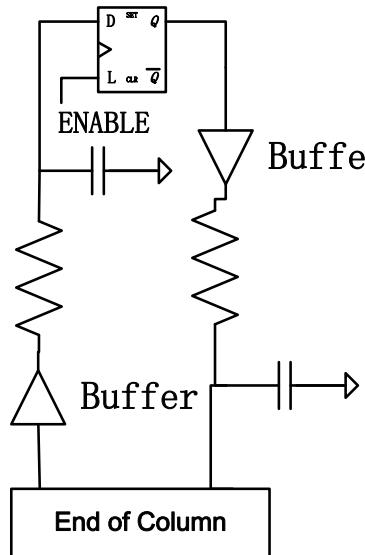
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The evaluation of the power consumption

The dynamic latch is used to generate timestamp. And the RC model (1.6mm metal line: 460ohm, 400fF) is for power evaluation.
All the results come from the Timestamp latching phase.



| Timestamp Metal line | The width and length of Metal line | Power consumption | Total Power with Buffer and Latch |
|----------------------|------------------------------------|-------------------|-----------------------------------|
| TS0 (CLK: 25ns) | 0.28um X 1.6mm | 2.54u | 29.54u |
| TS1(CLK: 50ns) | 0.28um X 1.6mm | 1.27u | 14.80u |
| TS2(CLK: 100ns) | 0.28um X 1.6mm | 635.98n | 7.37u |
| TS3(CLK: 200ns) | 0.28um X 1.6mm | 318.47n | 3.73u |
| TS4(CLK: 400ns) | 0.28um X 1.6mm | 159.81n | 1.90u |
| TS5(CLK: 800ns) | 0.28um X 1.6mm | 80.01n | 967.68n |
| TS6(CLK: 1600ns) | 0.28um X 1.6mm | 40.42n | 486.61n |
| TS7(CLK: 3200ns) | 0.28um X 1.6mm | 21.25n | 287.76n |
| Total | | 5.062u | 59 uA |

From the analysis of the table, the increasing current of Timestamp bus is around 59uA, which causes 132mW /cm² of power density.[unacceptable]

The contrast of two schemes

| Average Power | TaichuPix1 /FE-I3 like | FE-I3 upgrade | TaichuPix1 /ALPIDE like | ALPIDE upgrade |
|---------------------------------|------------------------|-------------------------|-------------------------|-------------------------|
| Initialization | 87uA | 51.52uA | 374uA | 23.23uA |
| Static | 81.2uA (Max) | 30nA | 155uA (Max) | 1.86uA |
| Each hit | 55uA | 500uA | 21uA | 32.09uA |
| Total average | 1.36uA | 5.18uA | 2.2uA | 3.52uA |
| Average Power density (Average) | 3.04mW/cm ² | 11.58mW/cm ² | 4.93mW/cm ² | 7.89mW/cm ² |
| Hit power density | 123mW/cm ² | 1120mW/cm ² | 49mW/cm ² | 71.88mW/cm ² |

Thanks for your attention.