Development of TaichuPix prototypes for the CEPC vertex detector

Zhang Ying

On behalf of the CEPC MOST2 Vertex detector design team

2021-8-17

Outline

- **Project motivation and TaichuPix chip overview**

- **Small scale prototypes design and test results**

- **Full size chip design**

- **Summary**

MOST2 project requirements on pixel chip

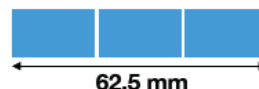## Silicon Vertex Detector **Prototype** – MOST (2018–2023)

Sensor technology CMOS TowerJazz

✦ Design sensor with large area and high resolution
✦ Integration of front-end electronic on sensor chip

Benefit from MOST 1 research program

Double sided ladder   Layer 1 (11 mm x 62.5 mm)
Chip size: 11 mm X 20.8 mm

3 X 2 layer = 6 chips

62.5 mm

Ref: Introduction to the Pixel MOST2 Project, Joao Costa, 2018.6

3-layer sector

L1
L2
L3
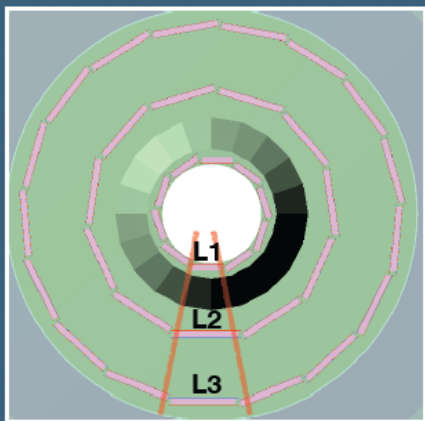
Baseline MOST2 goal:
3-layer prototype

Default layout requires different size ladders

Keep it simple for baseline design

L1
L2   3-layers
         same size
L3   same chip

Goals:
1 MRad TID
3-5µm SP resolution

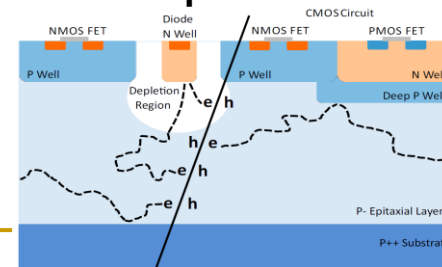**Integrate electronics readout**

Design and produce light and rigid support structures

8

- ■ **Motivation for TaichuPix chip design**
  - ➢ Large-scale & full functionality pixel chip
  - ➢ Fit to be assembled on ladders with backend Elec. & DAQ

CMOS pixel sensor

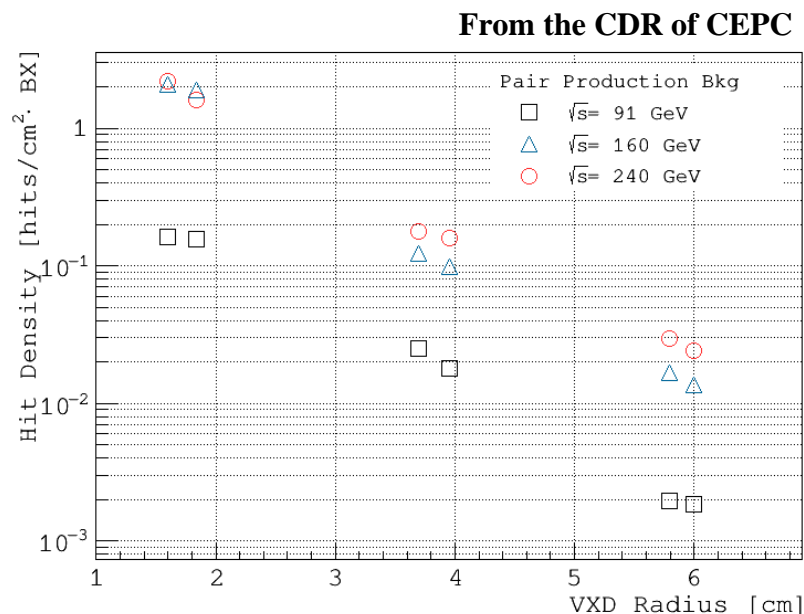# Main specs of the full size chip for high rate vertex detector

- **Bunch spacing**
  - ➢ Higgs: 680 ns; W: 210 ns; Z: 25 ns
  - ➢ Meaning 40M/s bunches (same as the ATLAS Vertex)

- **Hit density**
  - ➢ 2.5 hits/bunch/cm² for Higgs/W; 0.2 hits/bunch/cm² for Z

- **Cluster size: 3pixels/hit**
  - ➢ Epi-layer thickness：~18 μm
  - ➢ Pixel size：25 μm × 25 μm

From the CDR of CEPC

For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<= 25 μm	Hit rate	120 MHz/chip	Pixel array	512 row × 1024 col
TID	>1 Mrad	Date rate	3.84 Gbps --triggerless ~110 Mbps --trigger	Power Density	< 200 mW/cm² (air cooling)
		Dead time	< 500 ns --for 98% efficiency	Chip size	~1.4 cm×2.56 cm

TaichuPix architecture
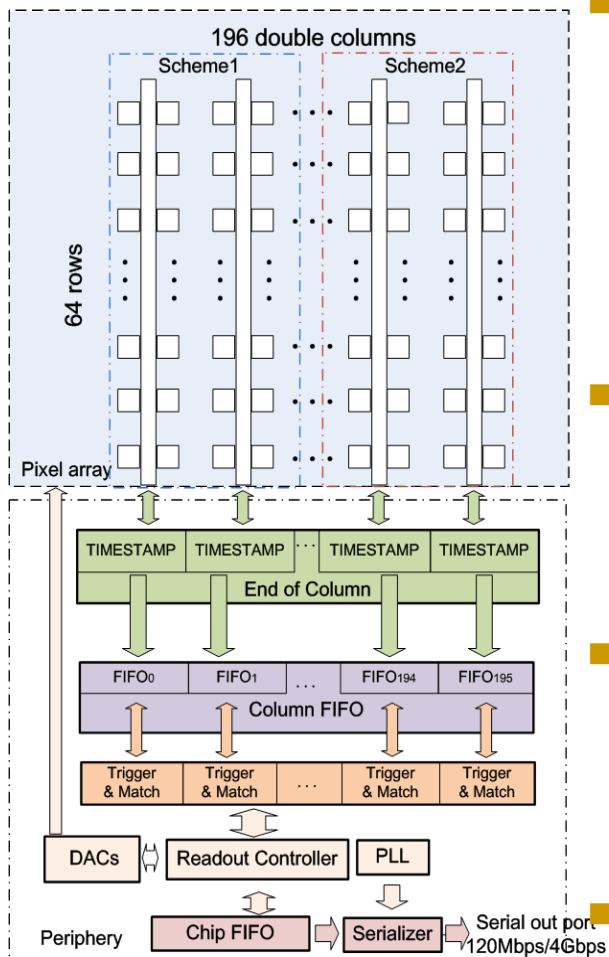
- **Similar to the ATLAS ITK readout architecture: "column-drain" readout**
  - Priority based data driven readout, zero-suppression intrinsically
  - Modification: time stamp is added at EOC whenever a new fast-or busy signal is received
  - Dead time: 2 clk for each pixel (50 ns @40MHz clk)

- **Two parallel pixel digital schemes**
  - ALPIDE-like: Readout speed was enhanced for 40MHz BX
  - FE-I3-like: Fully customized layout of digital cells and address decoder for smaller area

- **2-level FIFO architecture**
  - L1 FIFO: In column level, to de-randomize the injecting charge
 - L2 FIFO: Chip level, to match the in/out data rate between the core and interface

- **Trigger readout**
  - Make the data rate in a reasonable range
  - Data coincidence by time stamp, only matched event will be readout

Outline

- **Project motivation and TaichuPix chip overview**

- **Small scale prototypes design and test results**
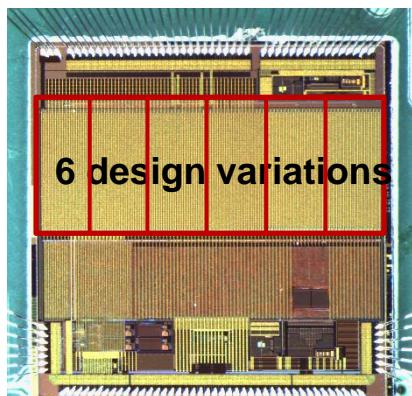
- **Full size chip design**

- **Summary**

TaichuPix small prototypes overview
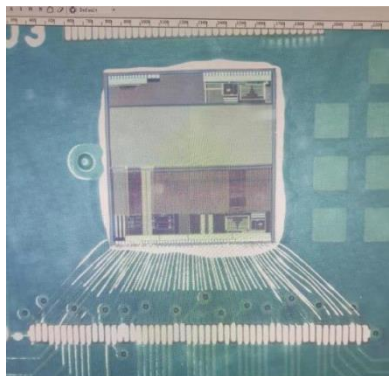
TaichuPix-1
Chip size：5 mm × 5 mm
Pixel size：25 μm × 25 μm
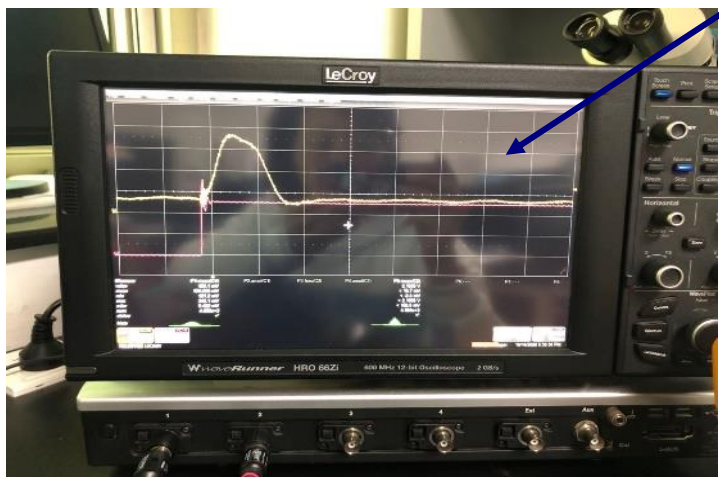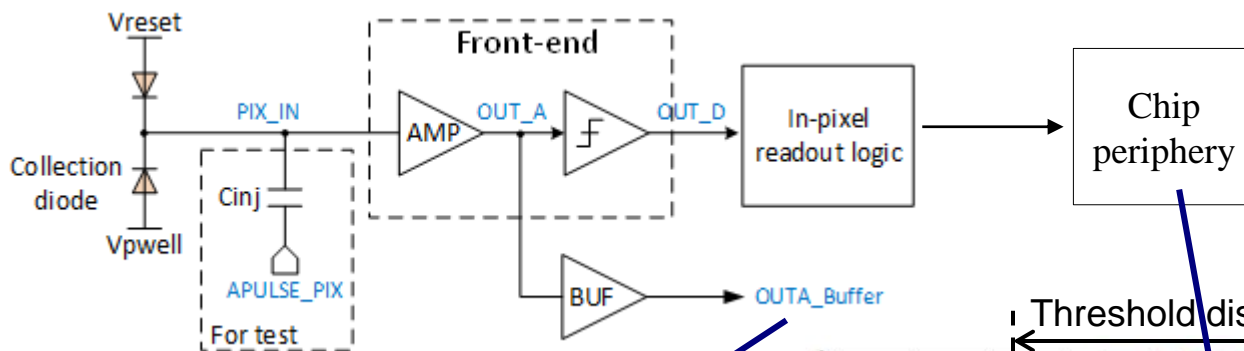

TaichuPix-2
Chip size：5 mm × 5 mm
Pixel size：25 μm × 25 μm

- **Two MPW chips were fabricated and verified**
  - TaichuPix-1: 2019.06~2019.11
  - TaichuPix-2: 2020.02~2020.06

- **Chip size 5 mm×5 mm with standalone features**
  - In-pixel circuitry:
    - Continuously active front-end
    - Two digital schemes, with masking & testing config. logics
  - A full functional pixel array (64×192 pixels)
  - Periphery logics
    - Fully integrated logics for the data-driven readout
    - Fully digital control of the chip configuration
  - Auxiliary blocks for standalone operation
    - High speed data interface up to 4 Gbps
    - On-chip bias generation
    - Power management with LDOs
    - IO placement in the final ladder manner
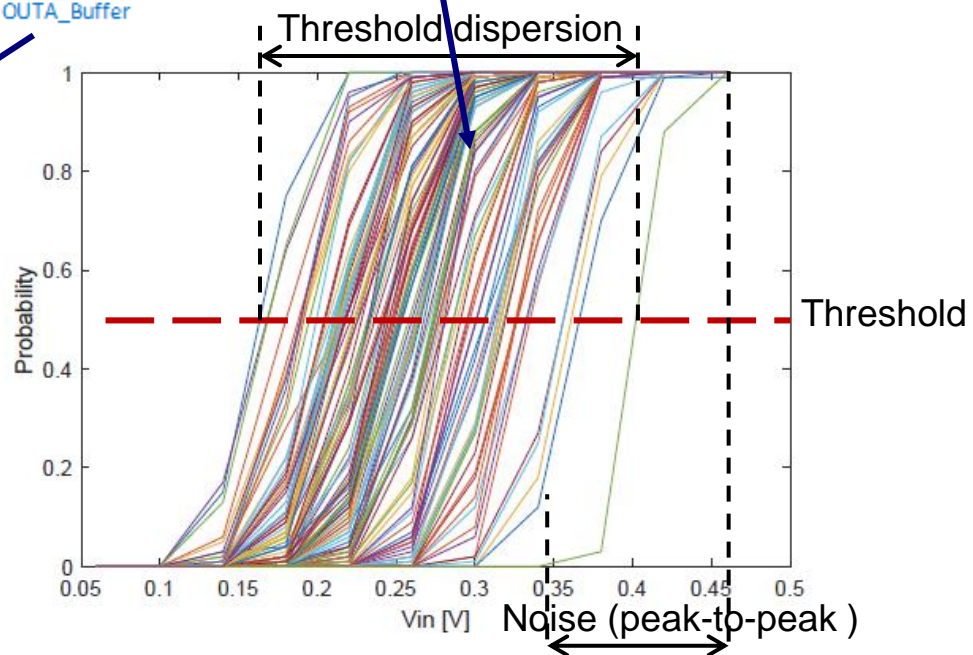   - Multiple chip interconnection features included

Electrical test

- **Electrical performance verified by injecting external voltage pulses into pixel front-end**

Analog output of a pixel @ Vin = 0.9 V
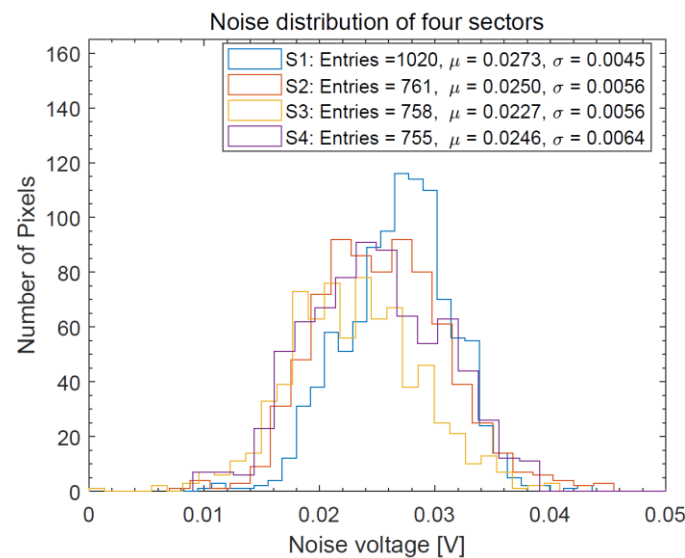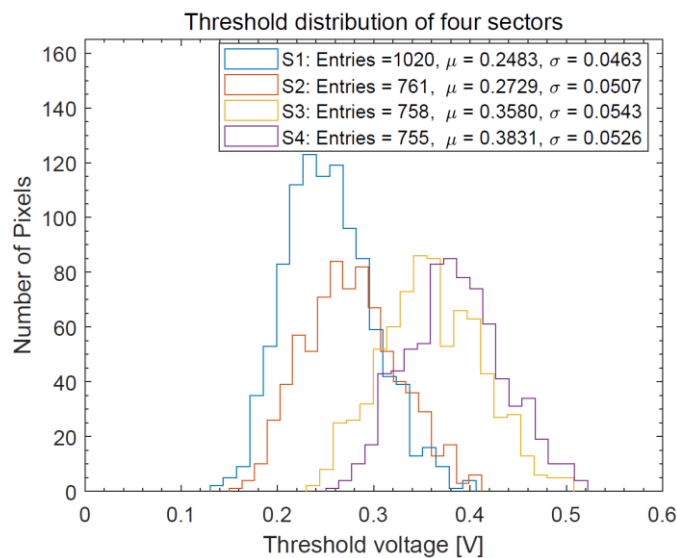
Measured "S-curve" for 128 pixels

Performance of threshold and noise of TaichuPix2

- **Bias setting: ITHR = 6.2 nA, VSUB = 0 V**

 ➢ Threshold can be tuned by changing ITHR (a global current bias)

Chip4	Threshold Mean (e-)	Threshold rms (e-)	Temporal noise (e-)	Total equivalent noise (e-)
S1	272.9	50.9	30.0	59.1
S2	299.9	55.7	27.5	62.1
S3	393.4	59.7	24.9	64.7
S4	421.0	57.8	27.0	63.8

Threshold distribution of four sectors
- S1: Entries =1020, μ = 0.2483, σ = 0.0463
- S2: Entries = 761, μ = 0.2729, σ = 0.0507
- S3: Entries = 758, μ = 0.3580, σ = 0.0543
- S4: Entries = 755, μ = 0.3831, σ = 0.0526

Noise distribution of four sectors
- S1: Entries =1020, μ = 0.0273, σ = 0.0045
- S2: Entries = 761, μ = 0.0250, σ = 0.0056
- S3: Entries = 758, μ = 0.0227, σ = 0.0056
- S4: Entries = 755, μ = 0.0246, σ = 0.0064

TaichuPix response to radioactive

- **Functionality of TaichuPix1&2 proved by various tests**
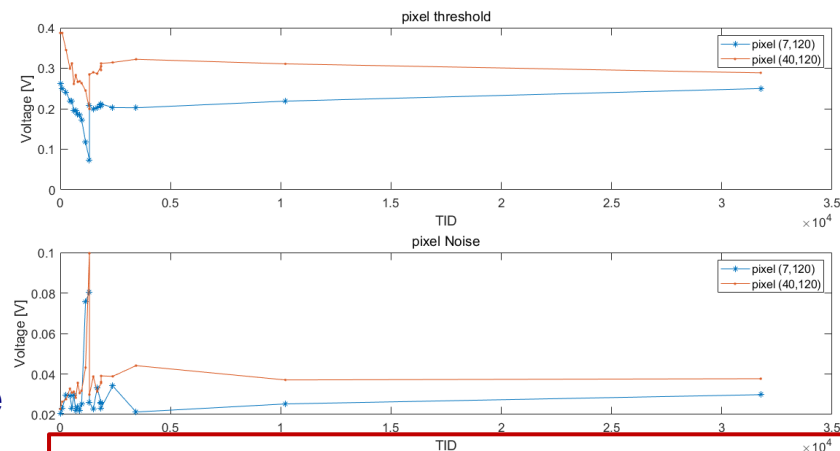

OUTA under Sr-90 injected
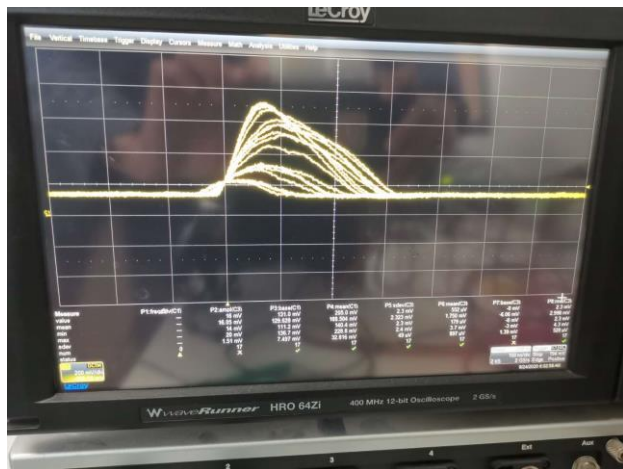
Analog output of a pixel response to **X-ray** tube
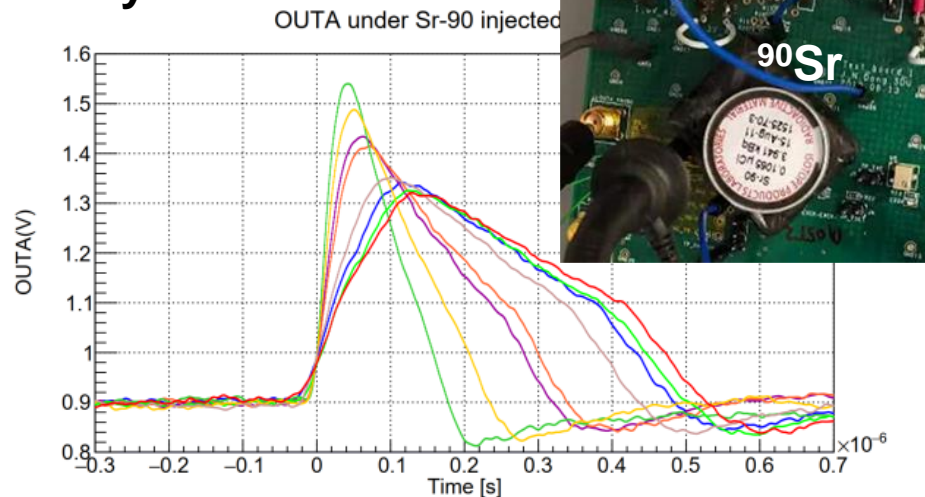
Analog output with **^{90}Sr** exposure
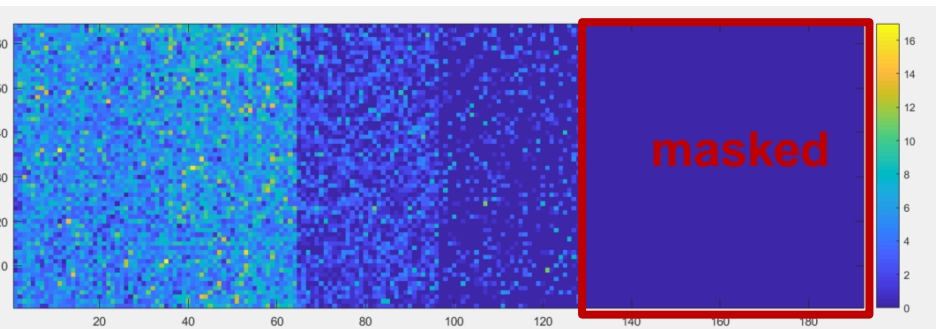
X-ray imaging with 5 min exposure @ 8 kV X-ray tube

Good chip functionality and noise performance proved up to **30 Mrad TID**

Outline

- **Project motivation and TaichuPix chip overview**

- **Small scale prototypes design and test results**

- **Full size chip design**

- **Summary**

Overview of the full size engineering run

1. **Pixel array 1024*512**
2. **Periphery**
3. **DAC & Bias generation**
4. **Data interface**
5. **LDO (test blocks)**
6. **Chip inter-connection features**
7. **Scribe-able top power connection features**

- **Process: 180 nm CMOS Imaging Sensor process (7 metal layers)**

- **Pixel cell copied exactly from MPW + scaled logic with new layout Periphery + debugged/improved blocks + enhanced power network**

Flex cable design consideration

2mm margin for wire bonding and PCB Pads
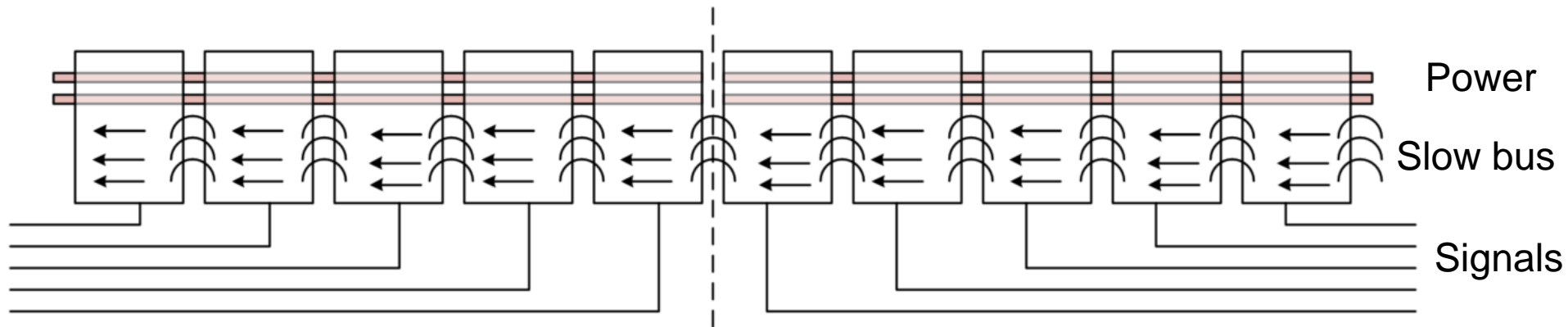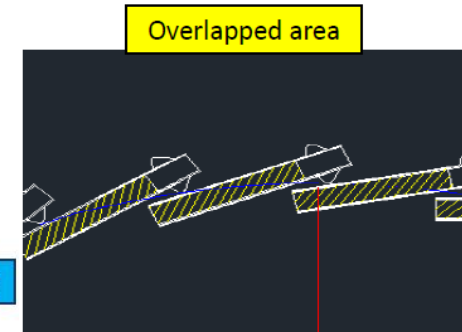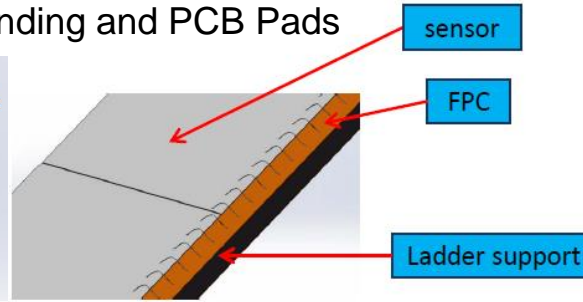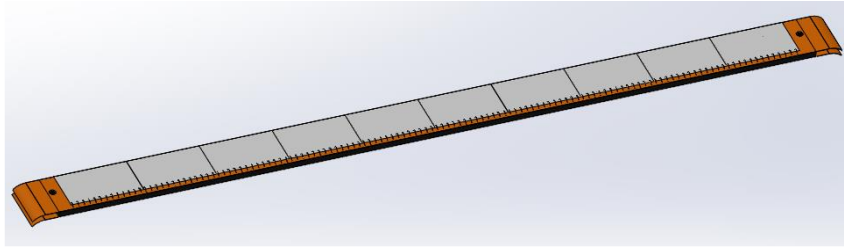
- **Design goals & considerations for the Flex PCB**
  - Minimum material budget
    - Minimum dead zone extension, limited height of PCB
      - Minimum set of signals on Flex
      - Slow buses to go on chip area by chip interconnection buses
    - Robust power supply
  - Manufacturability

Testability design & test plan consideration

- **All test features reserved, while the connected IOs will decrease at diff stages depending on chip test & study results**
  - ➢ Analog probe signals at the top part, accessible from the top pads
  - ➢ When mounted on ladder, only minimum self test possibilities can be reserved

1. **Probe Card design for the wafer test**
   - ➢ For all the pads at both sides

2. **Single chip test board design**
   - ➢ Designed with all the test features for the chip functional study

3. **Multiple chip test board for the ladder debugging**
   - ➢ Designed following the same manner as the ladder but on PCB
   - ➢ Signals and power supplies will be limited just with the ladder's dimension
   - ➢ Extra test signals can be connected to the extended area, to help debugging

4. **The real flex cable design for the ladder**
   - ➢ Core design and lessons will be exported from 3
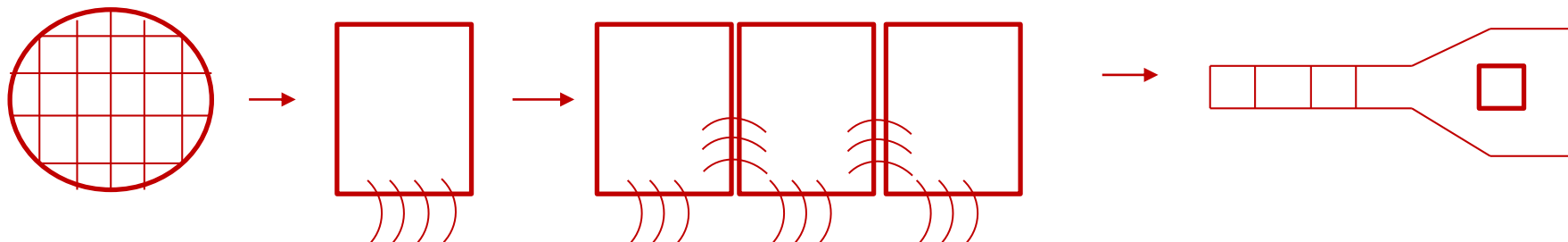
Summary

- **TaichuPix small prototypes were fully verified and preparing to submit the full size tape-out**

  - Full signal chain & functionality verified with both electrical & radioactive test

  - TID performance satisfied with CEPC's requirement with a large headroom

  - Full size chip design finished

- **Recent plan**

  - Design will be submitted for the engineering run

  - Preparation for the chip test (probe card, test PCB, flex cable …)
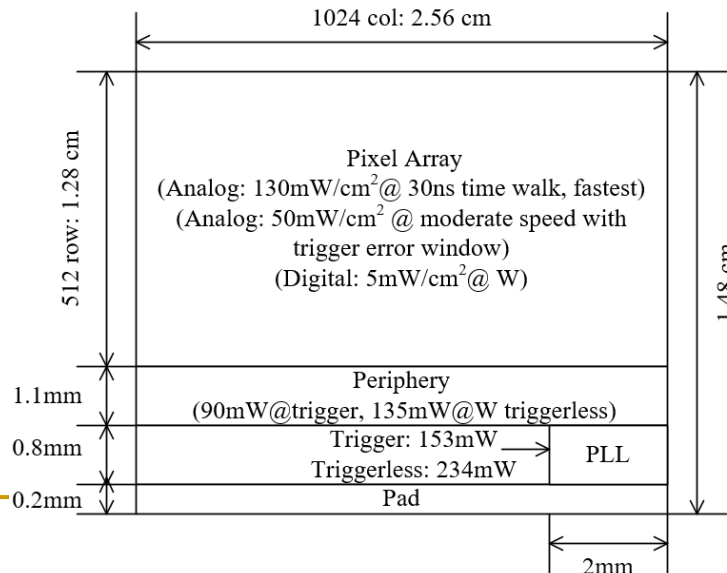
Thank you for your attention!

Backup

Chip Power consuming test
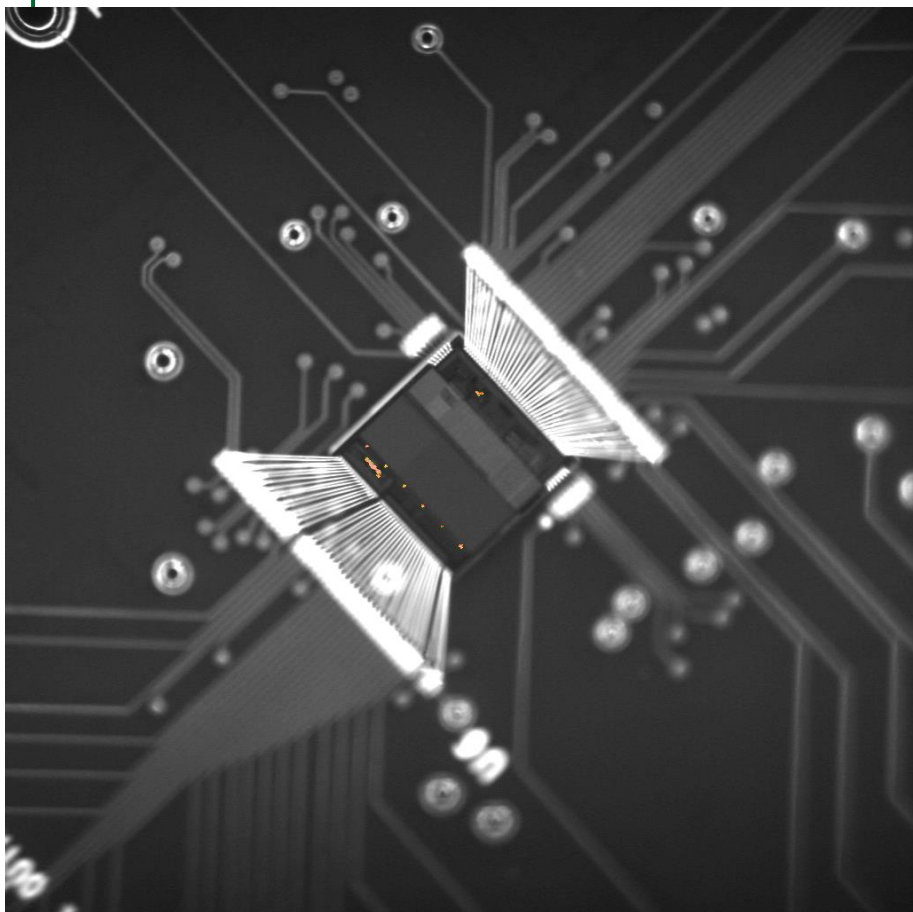
- **Tcpx2 chip current consuming tested of 210mA (380mW@1.8V)**

- **Almost agreed with simulation**
  - PLL@trigger speed: 306mW
    - Read by triggerless but at 160Mbps
    - Two PLLs in Tcpx2
  - Analog biased at fastest: 15mW (192*64 pixel array)
    - With 16 probe buffers
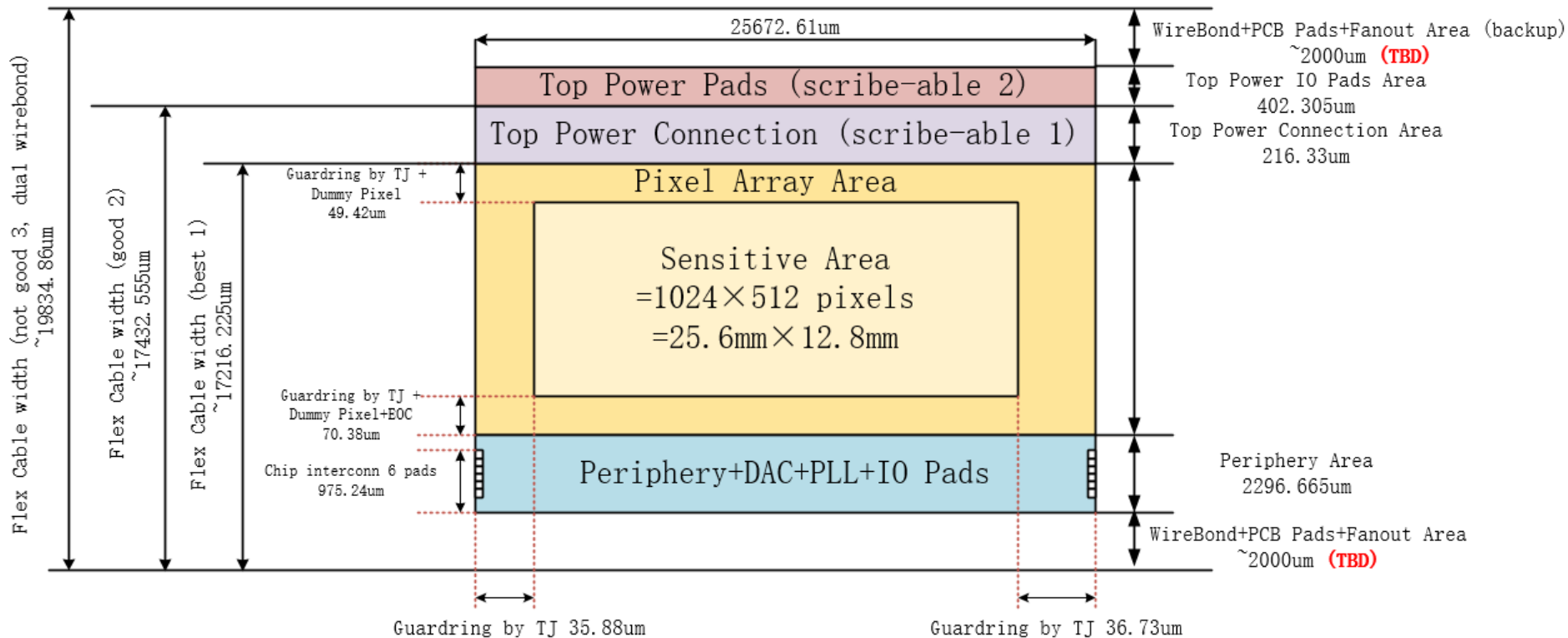 - Periphery@trigger speed: 90mW
    - Read by triggerless but at 160Mbps

- **The EMMI (Emission Microscope) test showed the hot points were exactly as expected**
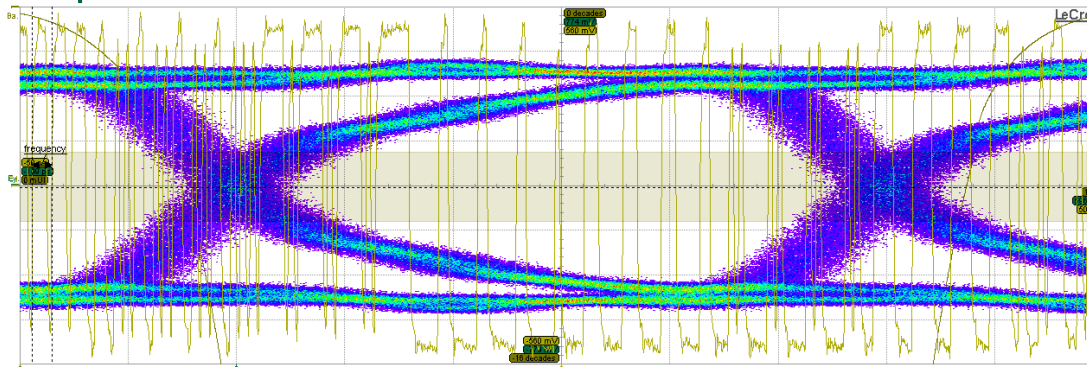 - quiet pixel array & periphery = no leakage point

1024 col: 2.56 cm

512 row: 1.28 cm

Pixel Array
(Analog: 130mW/cm^2@ 30ns time walk, fastest)
(Analog: 50mW/cm^2 @ moderate speed with trigger error window)
(Digital: 5mW/cm^2@ W)

1.48 cm

Periphery
(90mW@trigger, 135mW@W triggerless)

1.1mm

0.8mm
Trigger: 153mW
Triggerless: 234mW
PLL

0.2mm
Pad

2mm

All the four edges need at least ~50um for chip dicing remains

25672.61um

Top Power Pads (scribe-able 2)

Top Power Connection (scribe-able 1)

Pixel Array Area

Sensitive Area
=1024×512 pixels
=25.6mm×12.8mm

Guardring by TJ +
Dummy Pixel
49.42um

Guardring by TJ +
Dummy Pixel+EOC
70.38um

Chip interconn 6 pads
975.24um

Periphery+DAC+PLL+IO Pads

Flex Cable width (not good 3, dual wirebond) ~19834.86um

Flex Cable width (good 2) ~17432.555um

Flex Cable width (best 1) ~17216.225um

WireBond+PCB Pads+Fanout Area (backup)
~2000um (TBD)
Top Power IO Pads Area
402.305um
Top Power Connection Area
216.33um

Periphery Area
2296.665um

WireBond+PCB Pads+Fanout Area
~2000um (TBD)

Guardring by TJ 35.88um

Guardring by TJ 36.73um

Test of the data interface

@2.24Gbps

@3.36Gbps

Bit rate	2.24Gbps	3.36Gbps	4.48Gbps
Clk freq	1.12GHz	1.68GHz	2.24GHz
BER	6.59e-18	9.14e-13	3.23e-5
Tj@e-12	141.63ps	123.27ps	147.14ps
Rj	5.39ps	4.84ps	5.35ps
Dj	64.77ps	54.26ps	70.90ps

- **Data readout in DDR mode**
- **Data interface was tested by the on chip PRBS source, a high speed oscilloscope (@16Gsps), and code stream verified in FPGA**
- **BER qualified till 3.36 Gbps, failed at 4.48 Gbps**
- **Concerning the highest data rate for triggerless at 4Gbps, at least 2 SER interface ports needed**
- **Thus bit rate @2.24Gbps is safe and power optimized**

Readout & Periphery
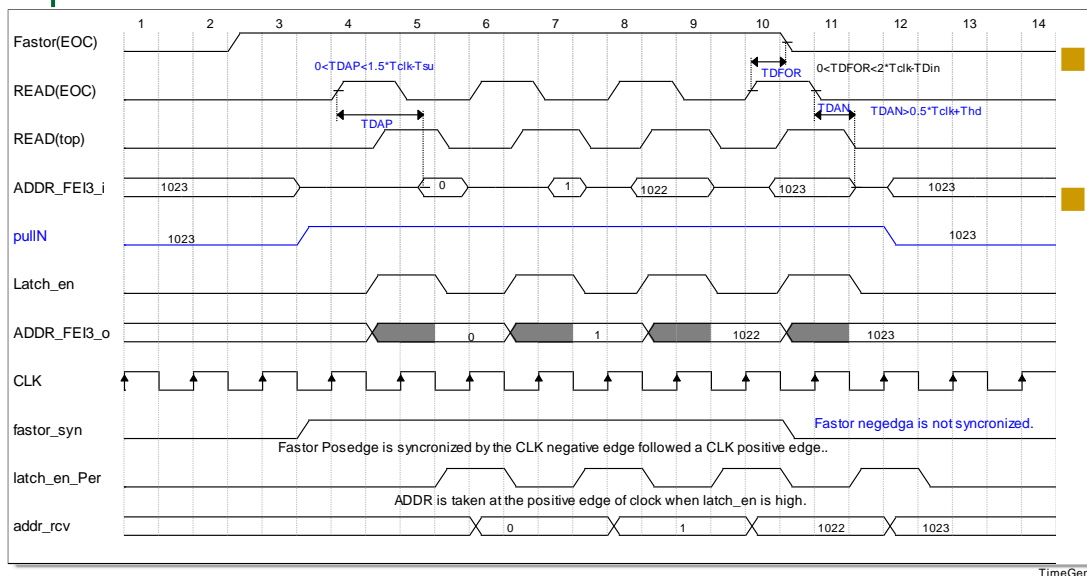
Time stamp recorded when Fastor is valid

Each pixel readout by 2 clocks (50ns)

- ↬ Worst delay ~ 25ns
  - ➤ Sim by 512 rows (full size)
  - ➤ TDA: read sent –addr come
- ↬ Address latch @ 37.5ns
  - ➤ @1.5 clock
  - ➤ Enough headroom for all corners

- **Designed for low power**
  - ↬ Only the hit (fastor) info & address are fannout from the pixel array
  - ↬ Only the read (acquisition) signal is fanned in to the pixel array
    - ➤ Clock & time stamp are localized only in the EOC, different from FE-I3

- **Optimized @ CEPC hit rate**
  - ↬ Common time stamp recorded for a full double column
    - ➤ For low power
    - ➤ Column is hit every 8.3us / pixel is readout in 2 clocks (50ns) / cluster size 3 pixels
    - ➤ Dead time 500ns – 98% trigger efficiency