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中国物理学会高能物理分会第十三届全国粒子物理学术会议

CMOS像素芯片JadePix3的性能测试

Yunpeng Lu

On behalf of the JadePix3 study group

2021/8/17

内容概要

- 背景介绍
- 物理需求
- 设计理念
- 测试流程
- 测试结果
- 结论

硅像素探测器

混合型（Hybrid）

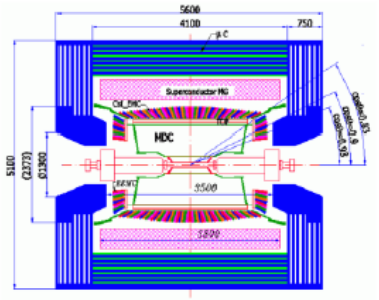
- ATLAS和CMS实验为代表
- 按Sensor可分为Planar，3D和Diamond
- 主要特点
  - 高抗辐照性能，TID~O(100) Mrad, NIEL~O(10^{15}) n_{eq} / cm^2
  - Time stamp per bunch, 25 ns
- 发展方向
  - HL-LHC：抗辐照性能和trigger rate提高>10倍
  - 物质科学 (X-ray)：高计数率~O(10^7) Hz / pixel 和高帧率~O(10^6) Frame / sec

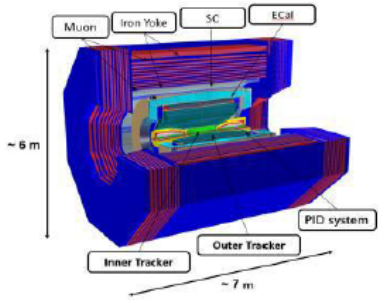
单片型（Monolithic）

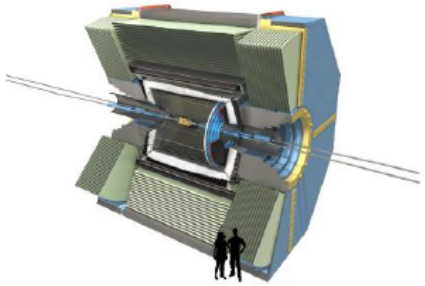
- ALICE和STAR实验为代表
- 按工艺可分为**CMOS**，DEPFET和SOI
- 主要特点
  - 极低物质量（0.15%辐射长度）
  - 大面积低成本（商业化CMOS生产）
- 发展方向
  - ALICE-ITS3: 65nm工艺 ~O(100) cm^2 拼接芯片
  - ATLAS和CLIC tracker：抗辐照性能~O(10^{15}) n_{eq} / cm^2

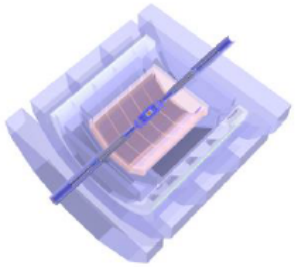
不同能区的e^+e^-对撞实验需求

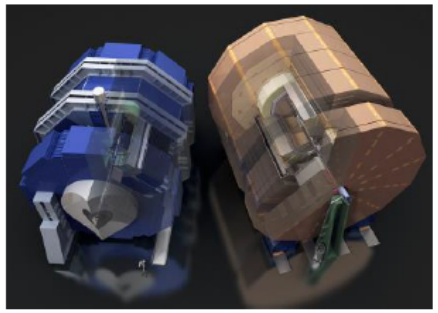
- 单片型像素探测器能够覆盖不同的实验需求
  - 采用两种有共性的技术：CMOS和SOI
  - 针对特定需求进行像素芯片的设计











Charm: 2-5 GeV → **Bottom: ~10.58 GeV** → **Higgs: 240-250 GeV**

BESIII upgrade/super-τC
物质量最敏感

BELLE II upgrade
亮度最高

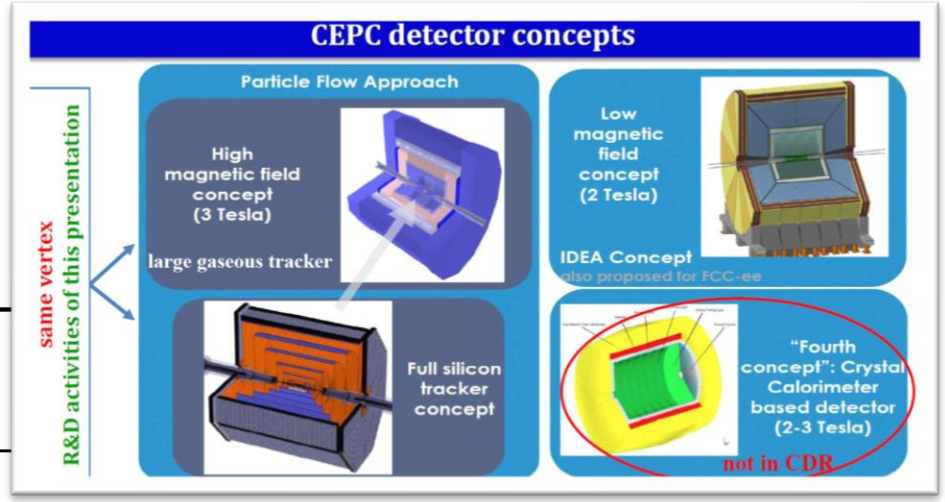
CEPC/ILC
精度最高

高精度、快读出、低功耗单片型硅像素探测器

工艺细节差别

JadePix3像素芯片的研发背景

- 科技部重点研发计划项目支持，《高能环形正负电子对撞机相关的物理和关键技术预研究》
- 针对High magnetic field探测器概念的指标要求设计
  - 也可用于Full silicon tracker探测器概念
- 物理测量与子探测器的关键性能



Physics process	Measurands	Detector subsystem	Performance requirement
$ZH, Z \to e^+e^-, \mu^+\mu^-$ $H \to \mu^+\mu^-$	$m_H, \sigma(ZH)$ $\mathrm{BR}(H \to \mu^+\mu^-)$	Tracker	$\Delta(1/p_T) =$ $2 \times 10^{-5} \oplus \frac{0.001}{p(\mathrm{GeV})\sin^{3/2}\theta}$
$H \to b\bar{b}/c\bar{c}/gg$	$\mathrm{BR}(H \to b\bar{b}/c\bar{c}/gg)$	Vertex	$\sigma_{r\phi} =$ $5 \oplus \frac{10}{p(\mathrm{GeV}) \times \sin^{3/2}\theta}(\mu\mathrm{m})$
$H \to q\bar{q}, WW^*, ZZ^*$	$\mathrm{BR}(H \to q\bar{q}, WW^*, ZZ^*)$	ECAL HCAL	$\sigma_E^{\mathrm{jet}}/E =$ $3 \sim 4\%$ at 100 GeV
$H \to \gamma\gamma$	$\mathrm{BR}(H \to \gamma\gamma)$	ECAL	$\Delta E/E =$ $\frac{0.20}{\sqrt{E(\mathrm{GeV})}} \oplus 0.01$

顶点探测器的关键参数优化

- Material budget, Spatial resolution, Radius of the inner most layer
  - Br (H -> cc) 对顶点探测器参数**显著敏感**，探测器性能至关重要
  - Br (H -> bb) 对顶点探测器参数不敏感

$$\frac{\delta_\mu}{\mu} \propto \frac{\sqrt{S+B}}{S} = \sqrt{\frac{1}{S}}\sqrt{\frac{S+B}{S}} \propto \frac{1}{\sqrt{\epsilon \cdot p}}.$$

Table 3. Maximum $\epsilon \cdot p$ value comparison for the $Br(H \to c\bar{c})$ measurement.

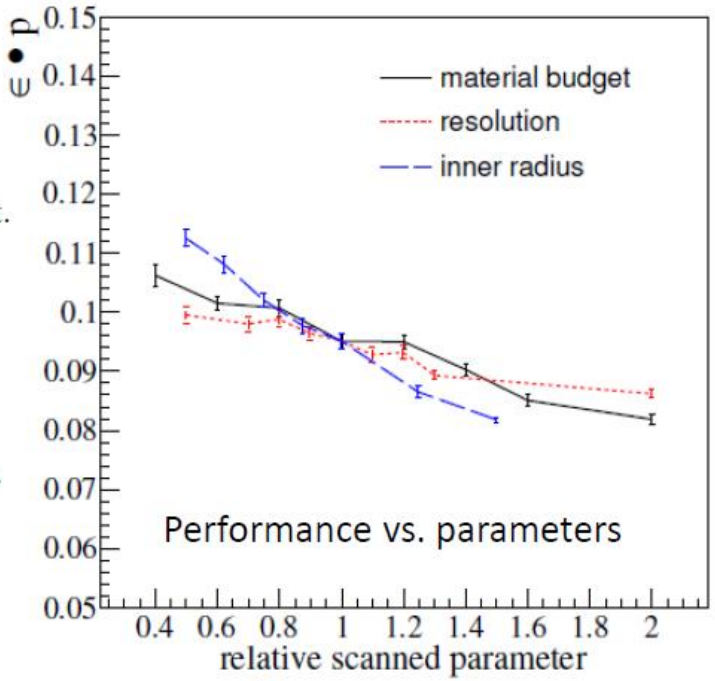
	Scenario A	Scenario B	Scenario C
$\epsilon \cdot p$	0.133 ± 0.002	0.095 ± 0.001	0.078 ± 0.001

41% -22%

Table 4. Maximum $\epsilon \cdot p$ value comparison for the $Br(H \to b\bar{b})$ measurement.

	Scenario A	Scenario B	Scenario C
$\epsilon \cdot p$	0.925 ± 0.001	0.914 ± 0.001	0.900 ± 0.001

1% -1.5%



$$\epsilon \cdot \mathrm{p} = 0.095(1 - 0.14\frac{\Delta x_{material}}{x_{material}})(1 - 0.09\frac{\Delta x_{resolution}}{x_{resolution}})(1 - 0.23\frac{\Delta x_{radius}}{x_{radius}})$$

ZG Wu, optimization on silicon detectors at CEPC, CEPC workshop, Nov. 2019

ZG Wu, MQ Ruan et al., Study of vertex optimization at the CEPC, 2018 JINST 13 T09002

像素芯片的预研方向（CDR阶段）

Impact parameter resolution

$$\sigma_{r\phi} = 5\mu m \oplus \frac{10}{p(GeV)\sin^{3/2}\theta}\mu m$$

Vertex detector specs

$\sigma_{s.p.}$ ~ 2.8um

Material budget ~ 0.15% X_0/layer

r of Inner most layer ~ 16mm

Pixel sensor specs

Side A

Small pixel ~ 16um

Thinning to ~ 50um

low power ~ 50mW/cm^2

fast readout ~ 1us

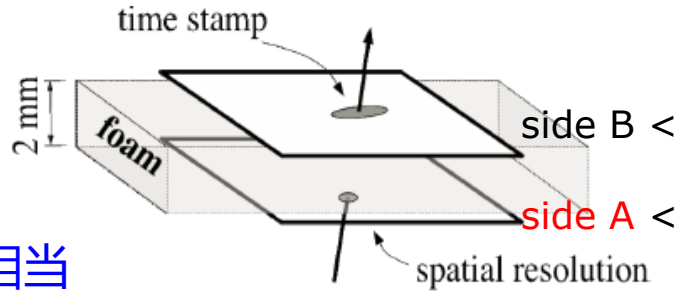
Side B

radiation tolerance ~

$\leq 3.4\ Mrad/year$

$\leq 6.2\times10^{12} n_{eq}/(cm^2\ year)$

- 预研方向1：Double-Sided ladder
  - Side A：小像素，低功耗（JadePix3设计目标）
  - Side B：快读出，低功耗（JadePix4备选方案）
- 预研方向2：新工艺（探测器发展方向）
  - 65 nm及以下 CMOS工艺
  - 或者180 nm 3D-SOI工艺 （周扬、董静报告）
- 优点：
  - 共用支撑结构，降低物质量
  - 像素芯片可在现有工艺上分别实现
  - 3层Double-sided与5层单面性能相当



side B < 1 μs积分时间

side A < 3 μm空间分辨

JadePix3的主要设计指标（与ALPIDE芯片对比）

- 空间分辨率进一步提高
  - 单像素面积为ALPIDE的一半
  - 代价是牺牲Time stamp granularity
- 平均功耗要尽量接近ALPIDE的水平
  - 像素减小，单位面积的通道数增加一倍
- 抗辐照能力要接近ALPIDE的水平
  - 同一个CMOS工艺，采用相同的抗辐照增强手段
  - 但是对辐照损伤机制的理解和经验还存在差距

	ALICE-ITS / ALPIDE	JadePix3
空间分辨率 (μm)	5	3
芯片减薄 (μm)	50	**目标：** 50
平均功耗(mW/cm^2)	<50	<100
Time stamp granularity (μs)	10	<100
抗辐照 TID，NIEL	1 Mrad/ year, 10^{12} n_{eq} / (cm^2 year))	**目标：** 1 Mrad/ year, $10^{12}$$n_{eq}$ / (cm^2 year))

Sensing Diode

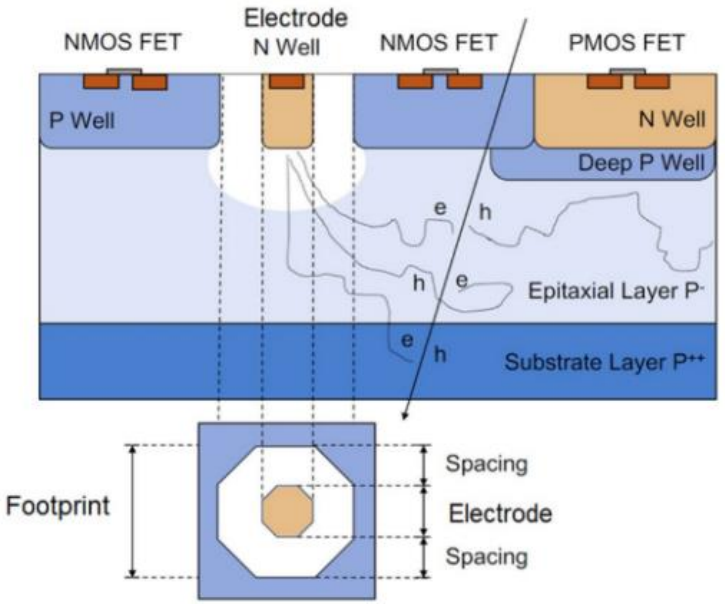
Ying Zhang, Zhou Yang

- 采用高阻外延层（EPI）的CMOS Imaging Sensor工艺
  - Small fill factor：Diode仅占像素面积的1/10，**电容小**（几fF）
  - 全像素面积灵敏：载流子在EPI中热扩散到Electrode，几乎100%收集
  - MIPs的信号电荷~1000e⁻，需要高增益放大器
- **电容小的好处一**：功耗与电容的平方成正比（**有利于低功耗设计**）

$$P \propto I \propto \left(\frac{S/N}{Q/C}\right)^{2a}$$

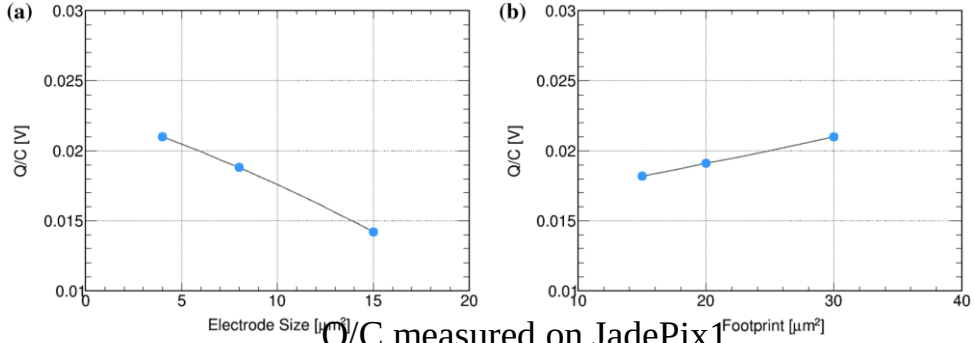
$a = 2$ in strong inversion
$a = 1$ in weak inversion

Fixing the S/N for a given bandwidth

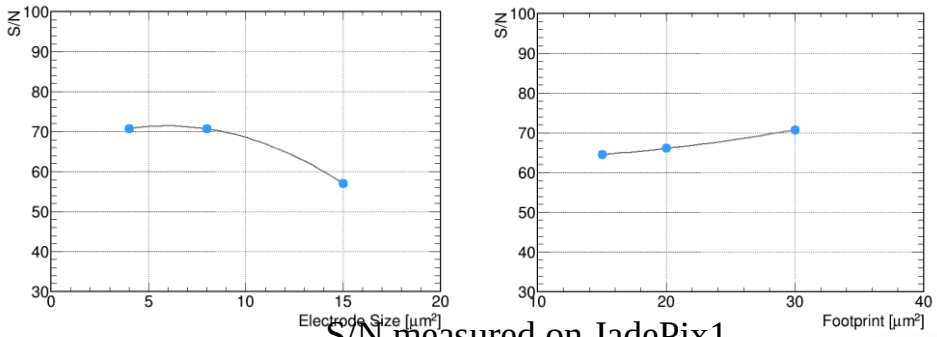


Schematic cross section of a CIS pixel

- 在JadePix1完成了几何尺寸的优化
  - Electrode size = 4 μm², Footprint = 36 μm²用于JadePix3



Q/C measured on JadePix1

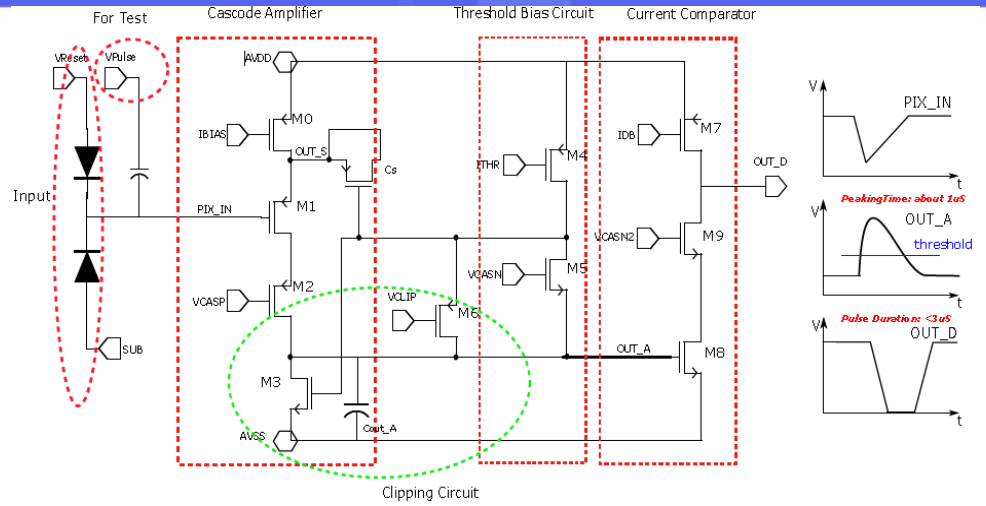


S/N measured on JadePix1

模拟前端

Ying Zhang, Weiping Ren

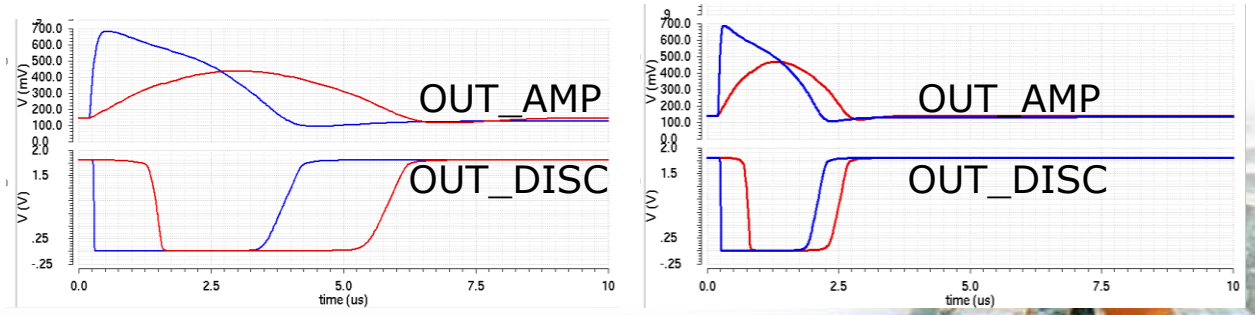
- **电容小的好处二**：基于电流比较器的放大和甄别电路
  - 单级增益高达2 mV/e⁻
  - 阈值一致性好，不需要DAC调阈值
  - 电路结构简单， ~10个MOS管，**有利于实现小像素**



- 模拟前端的主要设计结果：标称阈值=~150e⁻，阈值分布σ=~4e⁻，瞬态噪声=~4e⁻
  - 基于ALPIDE公开发表的电路优化结果
  - 压缩了FPN的设计冗余量→减小layout面积，缩小像素尺寸
  - **低功耗（20nA）版本**作为基准设计
  - **高功耗（60nA）版本**用于比较抗辐照性能

(增大电流减少MOS管阈值漂移带来的相对变化)

低功耗（左）和高功耗（右）模拟前端的仿真波形
(红：200e⁻；蓝：2000e⁻)

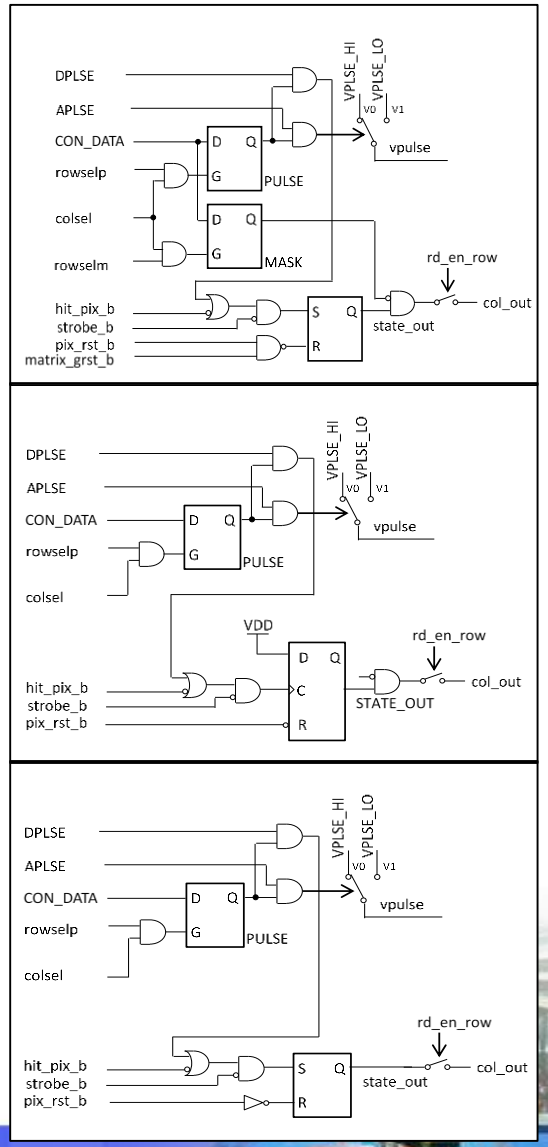


像素内逻辑

Ping Yang, Zhigang Wu, Yunpeng Lu

- HIT存储单元：两种结构
  - D-Flipflop，对甄别器输出的前沿敏感，用于连续读出（无触发）
  - D-Latch，对甄别器输出的电平敏感，用于触发读出
- 全局门控（Global shutter）：实现两种工作模式
  - 常开：**连续读出**（死时间可忽略）
  - 常关，有触发时才开：**先触发后读出**（读出时间为死时间），用于**测试对比 Noise hit rate**
- 必要的最小化的实用功能：
  - 测试脉冲产生电路
  - Test Pulse控制开关：每个像素单独控制测试输入
  - Pixel Mask控制开关：可单独关闭噪声像素
- 3个版本的像素内逻辑（digital front-end）
  - 以应对实际测试的各种可能情况

3种版本的像素内逻辑

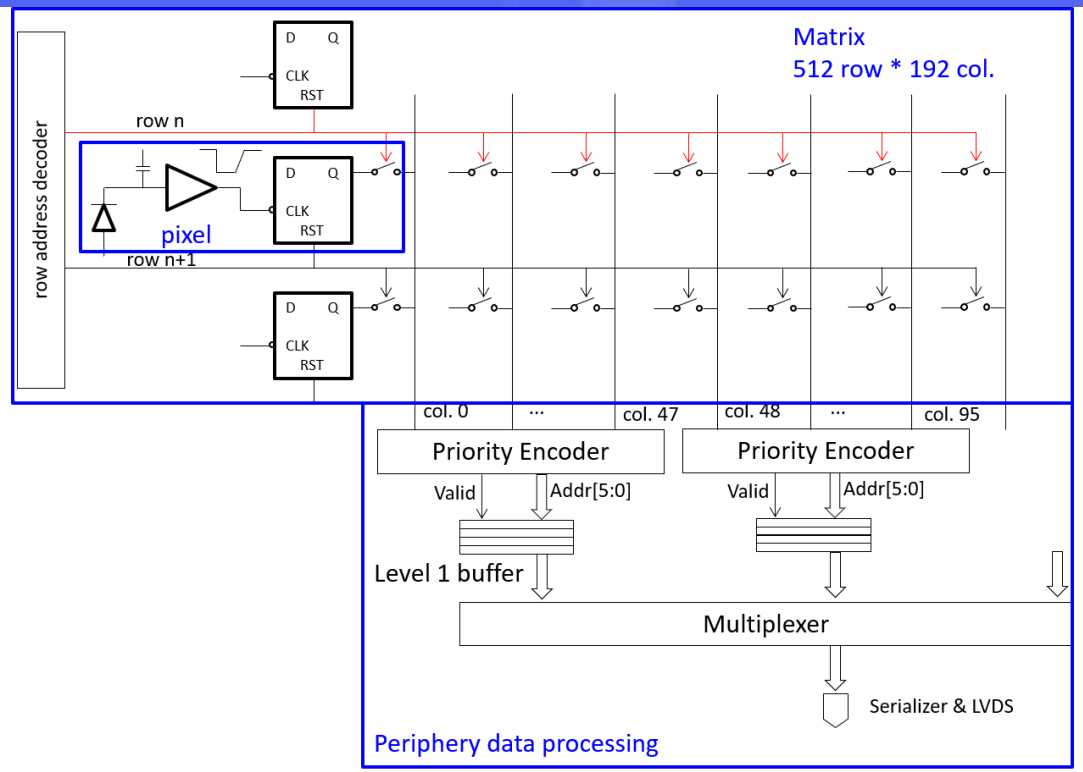


读出架构

Le Xiao, Yang Zhou, Zhigang Wu, Di Guo, Anyang Xu, Chengxin Meng, Yunpeng Lu

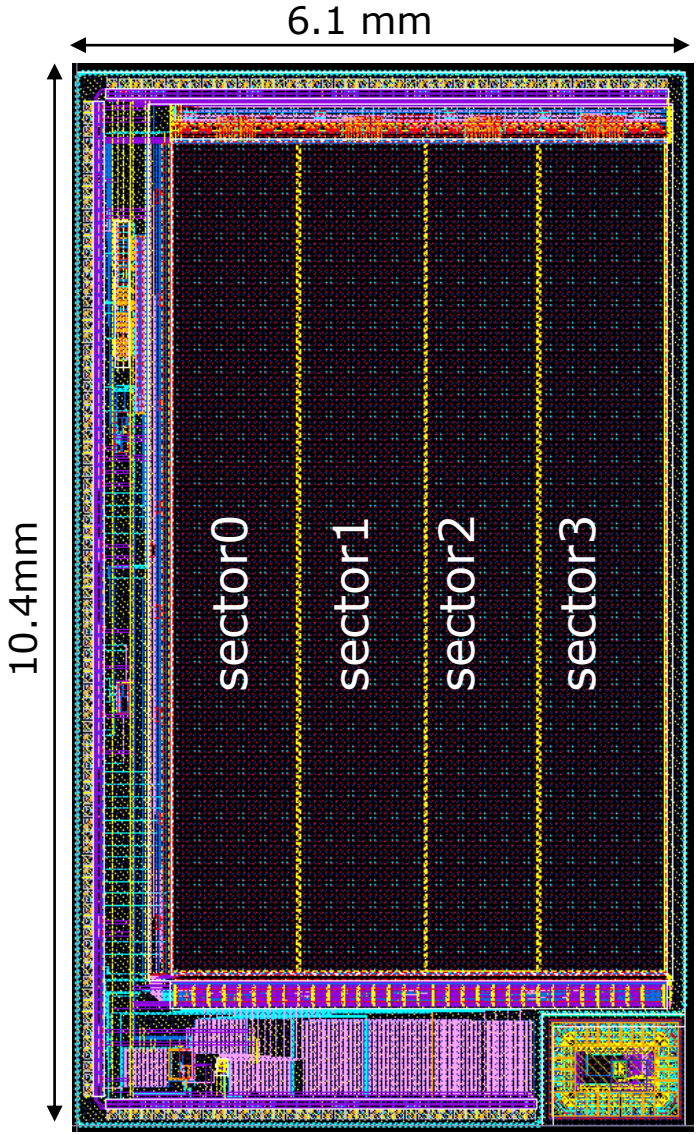
- Rolling Shutter（逐行扫描，按列共用输出线）
  - Matrix readout time:

    192ns/row * 512 rows = **98.3 μs/frame**
  - 地址编码在像素阵列外：相比于像素阵列内地址编码，**水平方向减小7 μm**
- End-of-Column零压缩
  - 优先级编码器（Priority Encoder）
  - 以行扫描的16倍速（12ns）搜索当前行中的HIT位置
  - 每个零压缩及缓存模块处理48列，共四个并行模块
- 数据传输模块
  - 8-bit并行输出端口（适用于单芯片读出）
  - 高速串行输出端口（适用于多芯片读出）

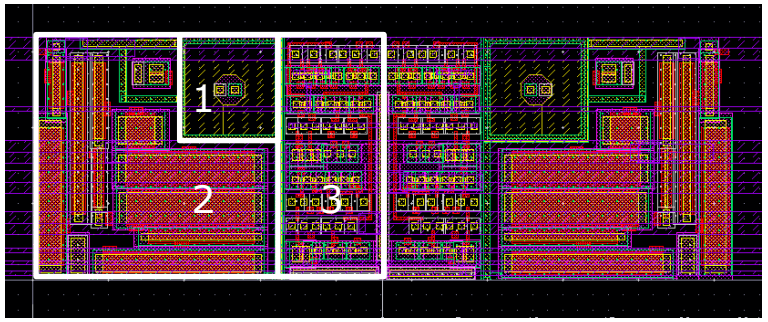


像素阵列的可扩展性

Yang Zhou, Yunpeng Lu



- 像素阵列512行，192列
- 垂直方向（φ方向）**达到实用尺寸**
  - 16 μm * 512 rows = 8.2 mm
  - 行数不再增加（帧扫描时间固定）
- 水平方向（z方向）可**按Sector扩展**
  - 48列/sector，共4个sector
  - 独立的零压缩和缓存模块
  - 共用80MByte/s的数据传输带宽



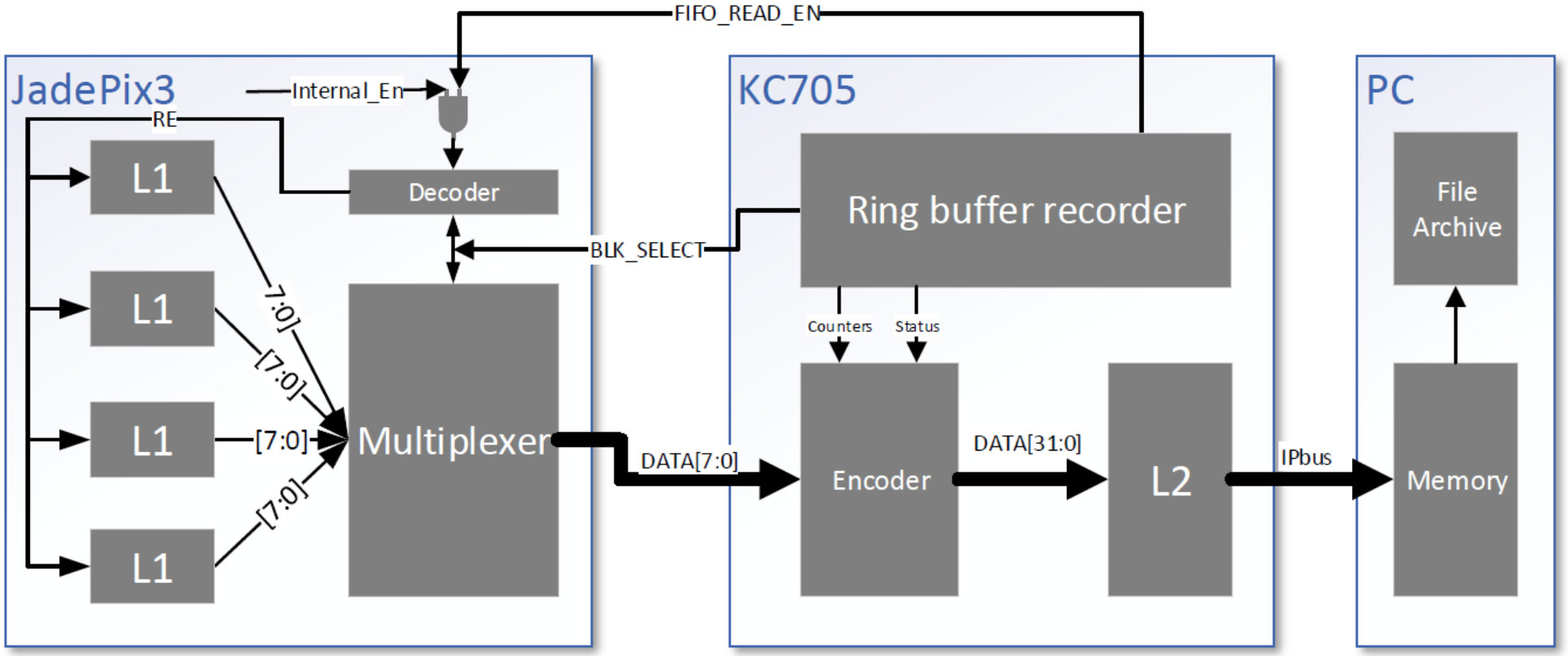
Minimal pixel footprint: **16 μm* 23.11 μm**
1: Sensing diode
2: Analog frontend
3: digital frontend

Sector	Diode	Analog	Digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	16×26 μm^2
1	2 + 2 μm	FE_V0	DGT_V1	16× 26 μm^2
2	**2 + 2 μm**	**FE_V0**	**DGT_V2**	**16× 23.11 μm^2**
3	2 + 2 μm	FE_V1	DGT_V0	16×26 μm^2

Test system

Sheng DONG, Hulin WANG, Yunpeng LU

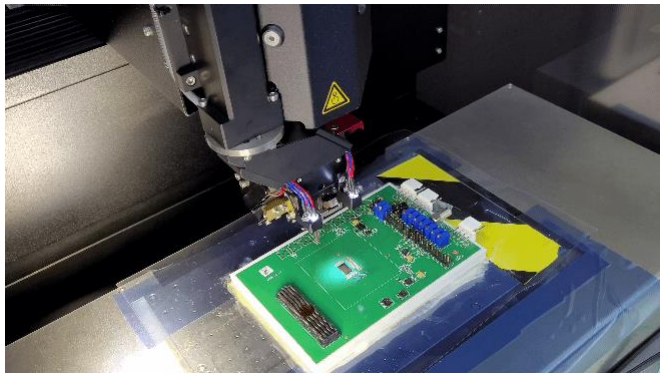
- General-purpose FPGA platform, KC705
  - Can be easily deployed and reused
- IPBUS protocol
  - Reliable high-performance **control link** for particle physics electronics
  - 700Mbps per TCP/IP link with **JUMBO PACKAGE** feature



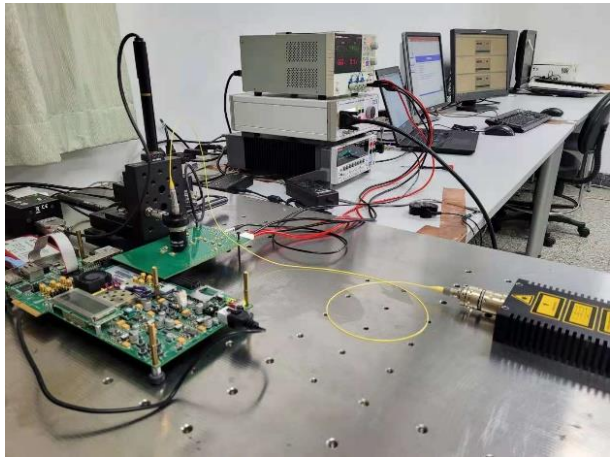
Chip-board assembly and test setup

- 7 boards assembled with the Jadepix3 chips
  - **All passed functional tests**
  - Counter measure of ESD proved effective
- Test setup deployment
  - IHEP, CCNU, JLU
  - To be deployed in USTC

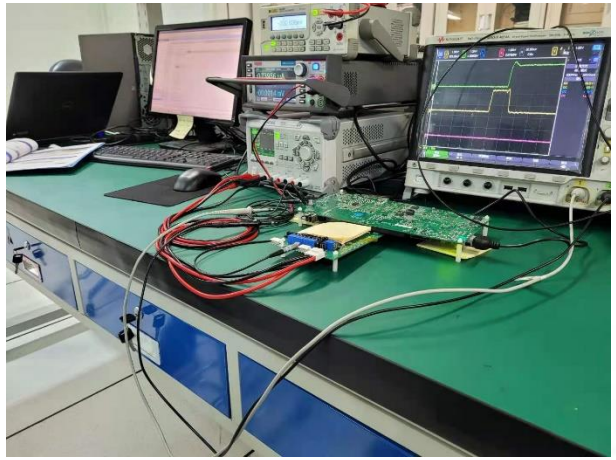
Daming SUN, Yunpeng LU



Wire bonding on the JadePix3 chip



Test setup in IHEP



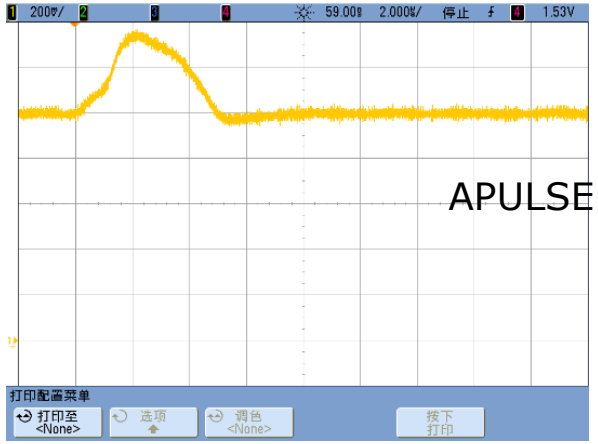
Test setup in CCNU

Functional verification

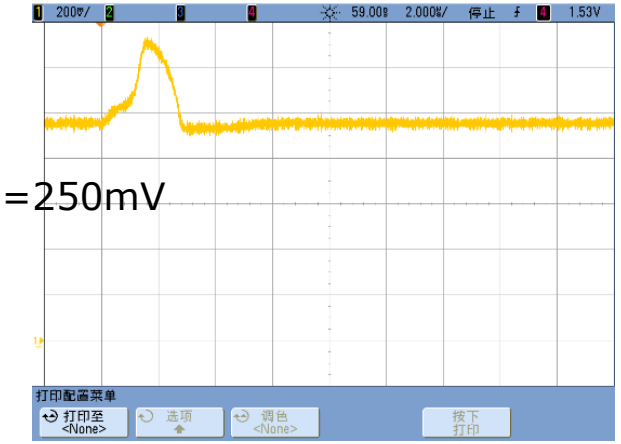
Sheng DONG, Yang ZHOU, Ying ZHANG, Zhan SHI, Yunpeng LU

- **All module** functions verified
  - Configuration of matrix registers
  - Configuration of Global DAC
  - Pulse test
  - Analog output waveform
  - Data readout
  - PLL clock
  - Serializer output pattern
- Response to the radiation as expected
  - Radiative source ^{55}Fe
  - Cosmic ray
  - **Pulsed laser beam**

Low power frontend

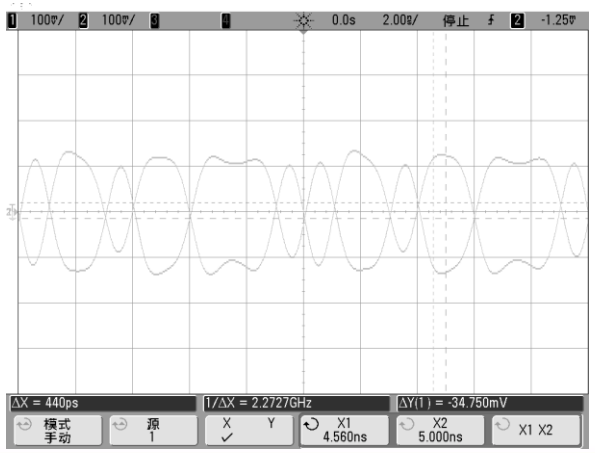


Radiation-enhanced frontend



APULSE=250mV

Output pattern of serializer @ 1Gbps

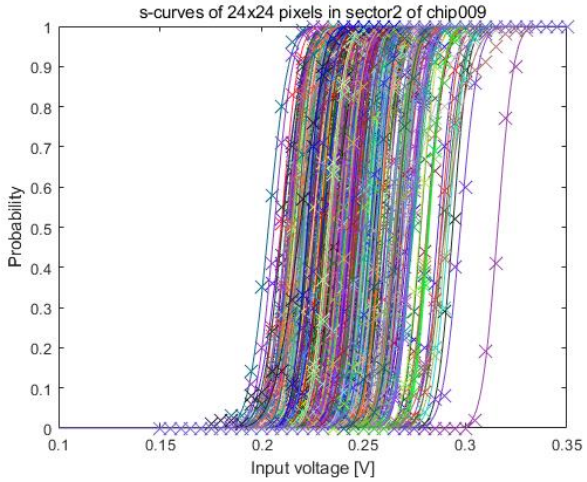


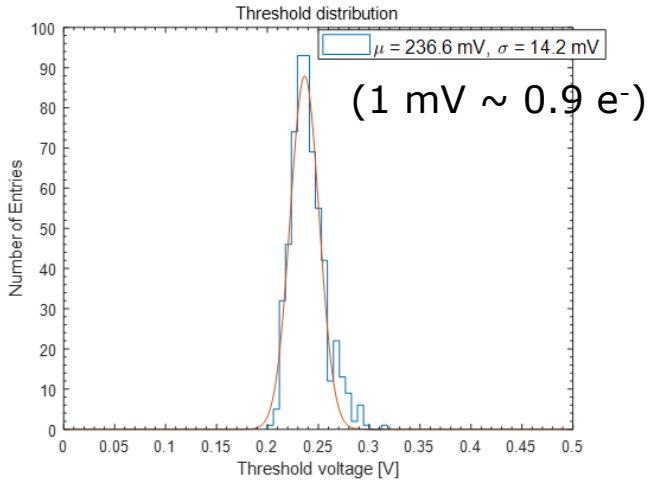
Threshold and Noise (Electrical pulse test)

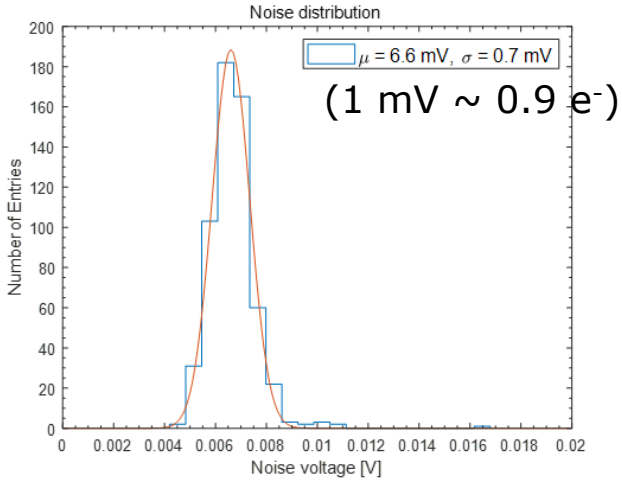
Ying ZHANG, Yang ZHOU, Jing DONG, Yunpeng LU

- Pulse amplitude scan and **S-curve*** fit @ nominal threshold

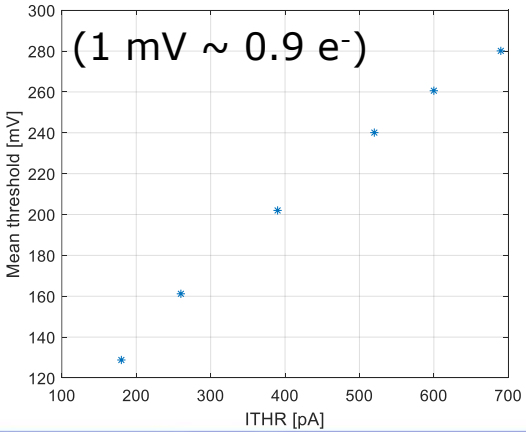
*S-curve: cumulative Gaussian distribution

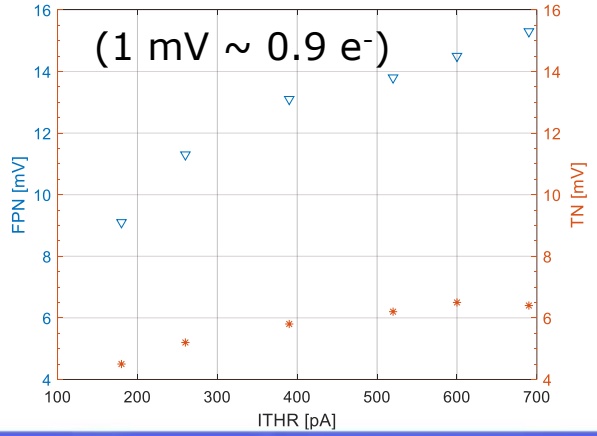


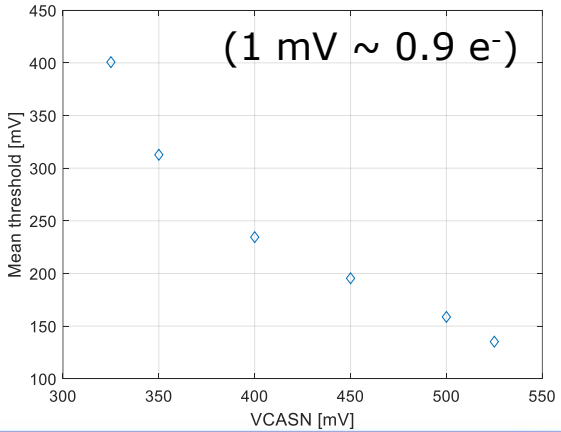


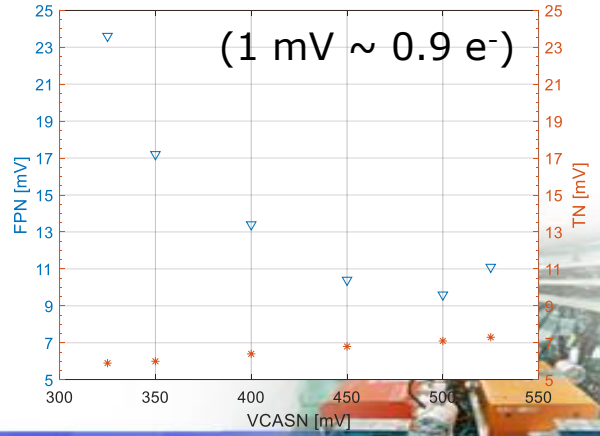


- **Input-referred threshold** as a function of the parameters Ithr and Vcasn
  - Nominal threshold = 220e$^-$ @ Ithr = 0.5 nA, Vthr= 400 mV





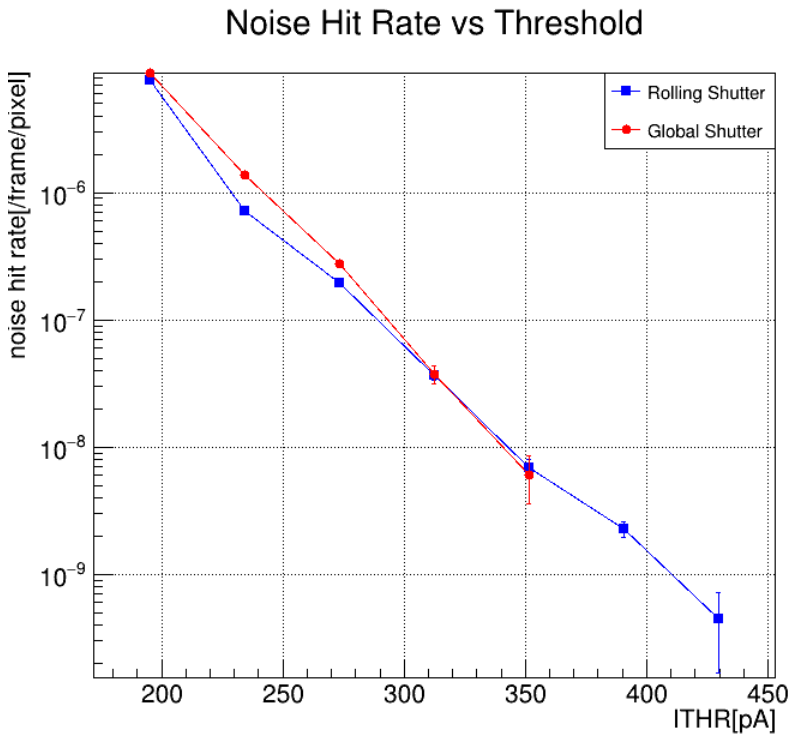


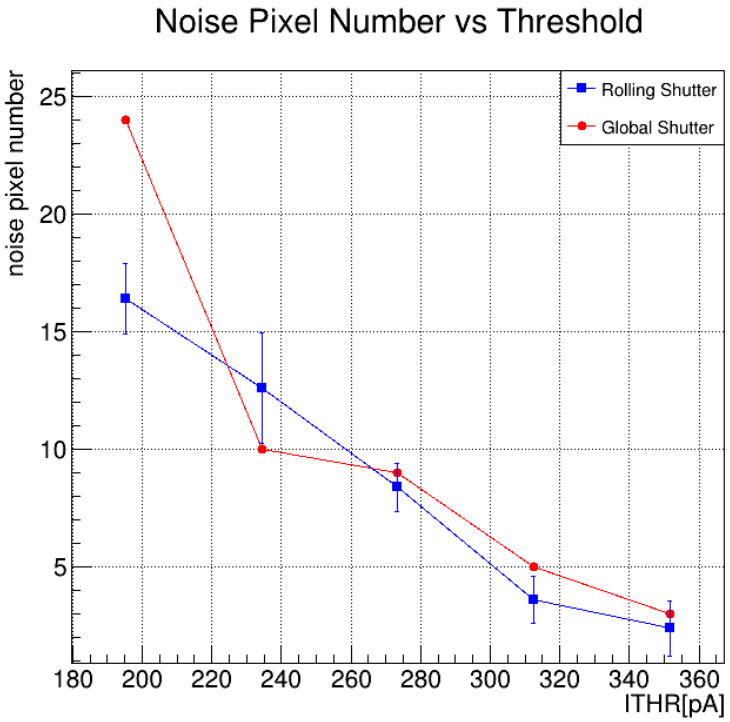


Noise hit rate

Chunhao Tian, Yunpeng LU

- Well below 10^{-6} hits / pixel per frame (98.3 μs)
  - Rolling shutter (**Continuous** readout mode) shows noise hit rate as low as the global shutter (**Triggered** readout mode)
  - No pixel masked



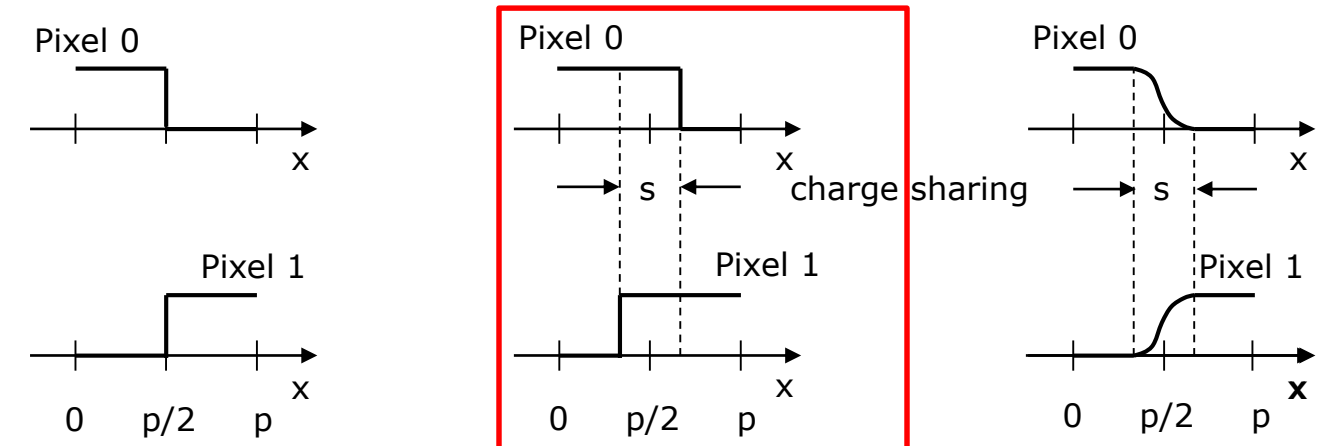


Charge sharing and spatial resolution

- Binary readout with charge sharing
  - $\sigma_{position} = \frac{p/2}{\sqrt{12}}$, when s = p/2 (namely average cluster size* = 1.5)

cluster size: number of fired pixels associated with one track hit

Signals in two adjacent pixels as function of the impact position x



Binary readout without charge sharing

$\sigma_{position} = p/\sqrt{12}$

Binary readout with charge sharing

$\sigma_{position} = s/\sqrt{12}$, inside the s region

$\sigma_{position} = (p-s)/\sqrt{12}$, outside the s region

Analog readout

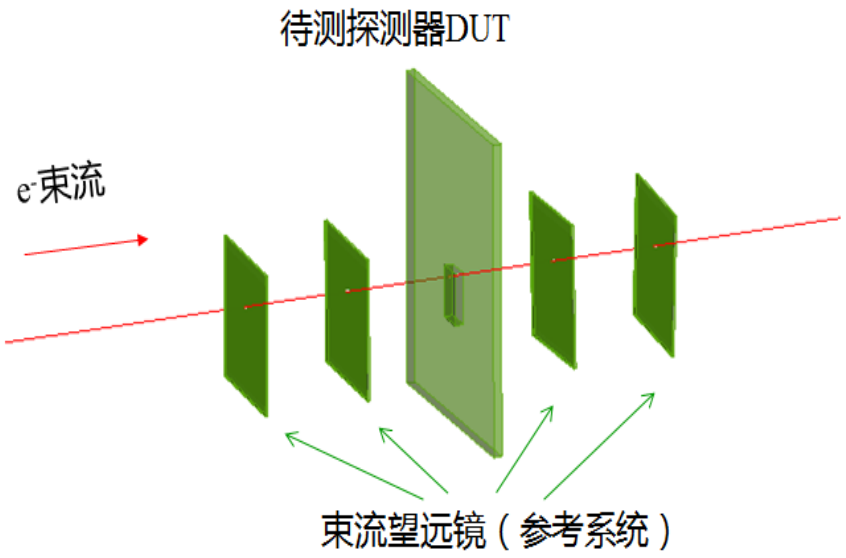
$\sigma_{position} = \frac{s}{S/N}$ inside the s region

$\sigma_{position} = (p-s)/\sqrt{12}$, outside the s region

Measurement method of position resolution

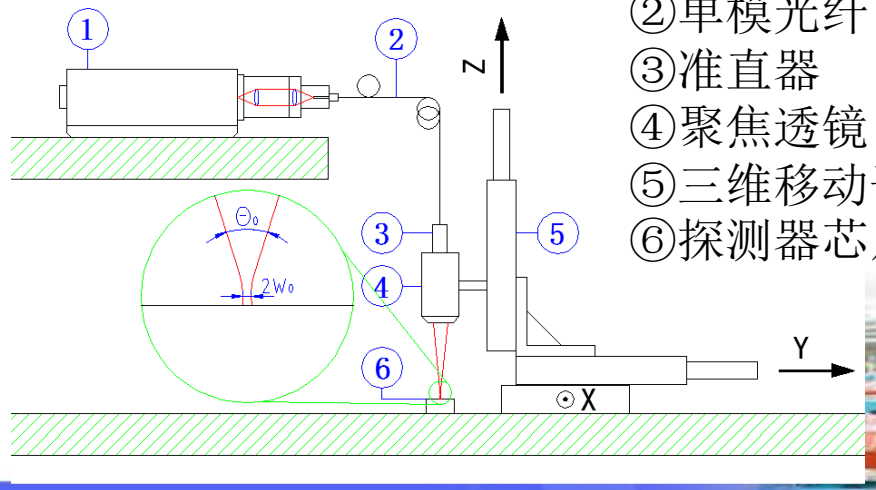
Charged particle beam

- Random hit position on the full matrix
  - One hit per particle
  - Reconstructed reference position by beam telescope
  - σ of residual = measured - reference
  - Cluster size can be adjusted by threshold tuning



Pulsed laser beam

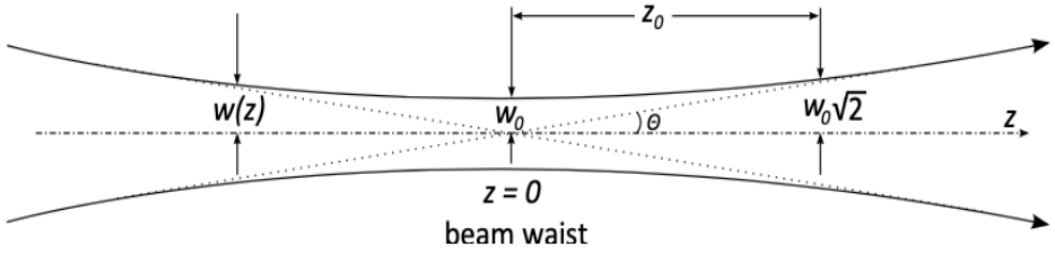
- Well controlled **scan of laser position** on a **single pixel**
  - One hit per laser pulse
  - Reference position given by the 3-D motion stage
  - σ of residual = measured - reference
  - Cluster size can be adjusted by threshold tuning and **laser power tuning**



①红外脉冲激光器
②单模光纤
③准直器
④聚焦透镜
⑤三维移动平台
⑥探测器芯片

Laser beam characteristics

Hulin WANG, Shen DONG, Yunpeng LU

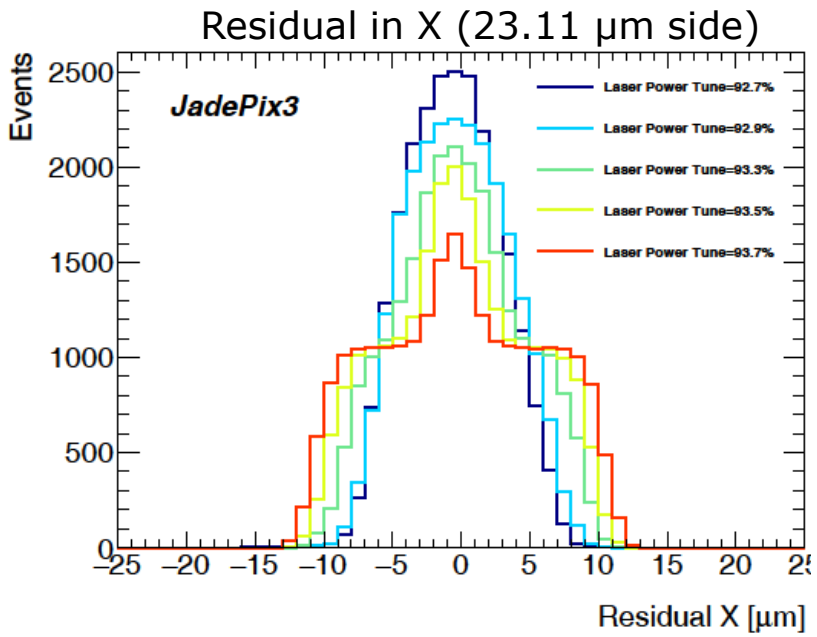


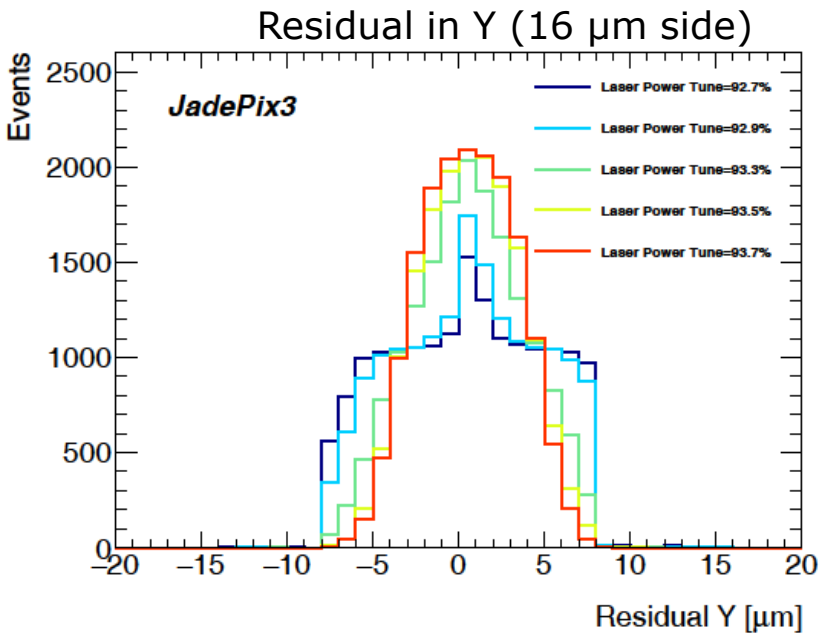
- Laser beam characterization
  - Wavelength: 1064 nm
  - Beam waist **ω_0 ~ 1.7 μm**
  - Rayleigh range z_0 ~ 8.5 μm
  - Divergence Angle **θ = ~ 11°**
  - Laser pulse duration ~100 ps
- Laser power tune and coarse calibration
  - 0% : maximum power; 100% : minimum power
  - For final results, use 92.7%, 92.9%, 93.3%, 93.5%, 93.7%
  - 92.7% ~ **4 × threshold** (threshold set to ~220 e-)
  - 93.7% ~ **2 × threshold**

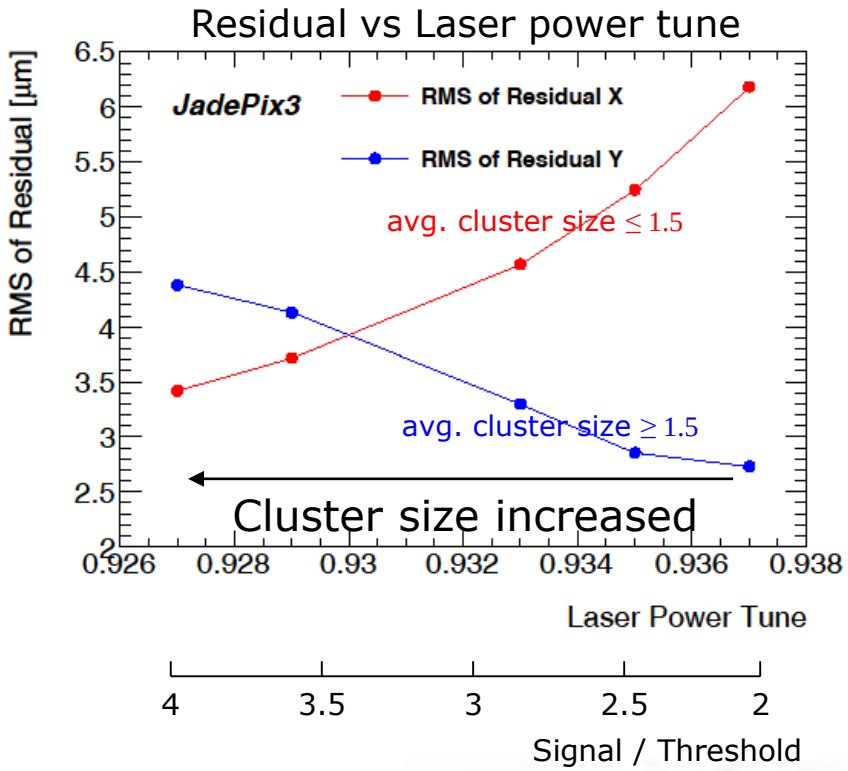
Position resolution

Hulin WANG, Shen DONG, Yunpeng LU

- Threshold set to 220e$^-$, tune the laser power to vary cluster size
- **Theoretical minimum value** can be approached on both sides
  - While cluster size approaching 1.5
  - 3.34 μm @ signal = 880e$^-$ in X
  - 2.31 μm @ signal = 440e$^-$ in Y







Power consumption

Ying ZHANG, Zhan SHI, Yunpeng LU

- Average power consumption with present chip size
  - (62.44-14.38-31.54 mA)*1.8V/(**1.04*0.61 cm²**)=**46.9 mW/cm²**
  - PLL and Serializer not included (single chip readout)
- Extrapolated to a full size chip of **1 cm*2.56 cm**
  - Sensitive area 0.819 cm*2.56 cm
  - PLL and Serializer included (multi-chip readout)
  - Average power **91.44 mW/cm²**
- Could be cut off further > 15 mA
  - Analog buffer (1.8mA)
  - LVDS receiver (1.74mA)
  - PLL test output (11.5mA)

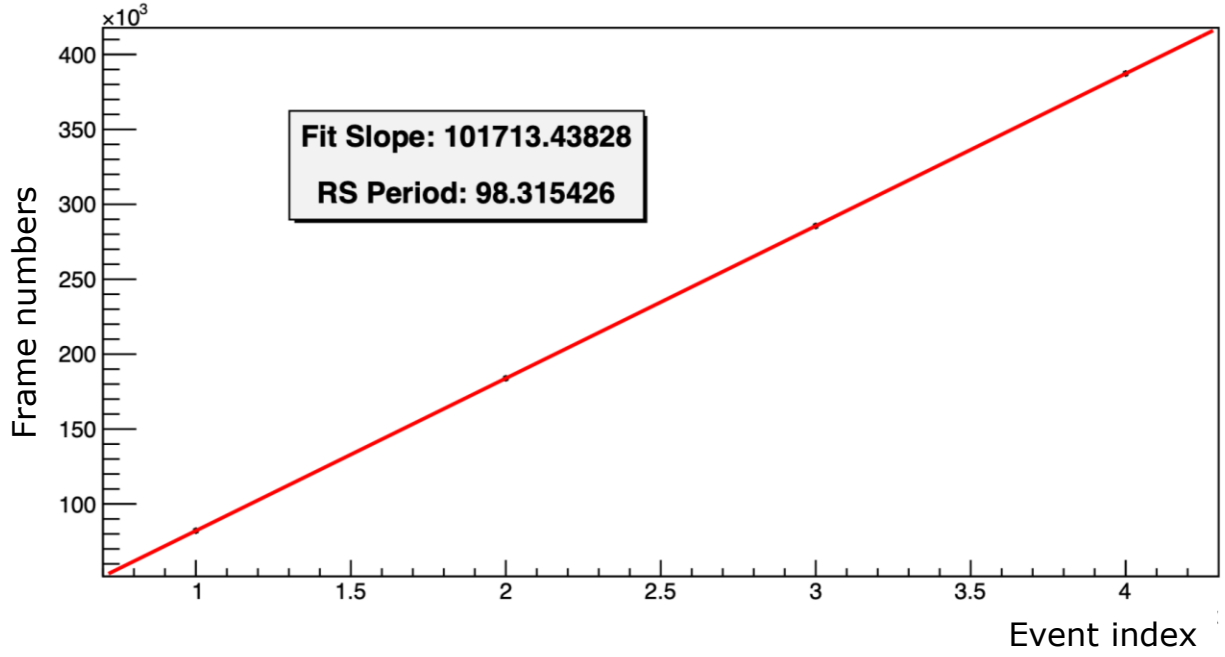
Extrapolation of average power consumption

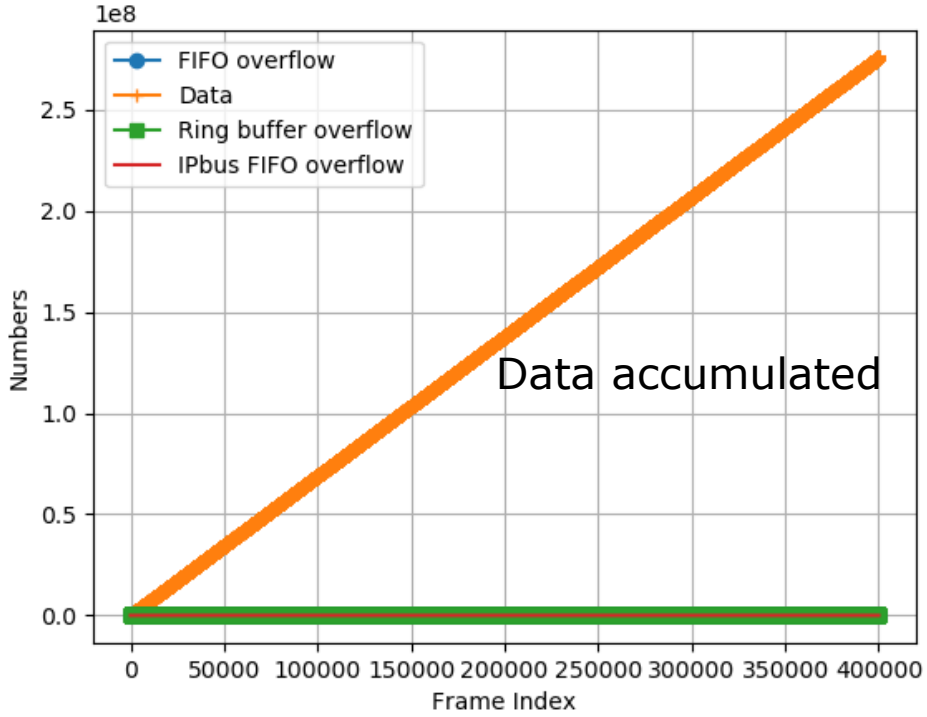
	512*192 (JadePix3)	**512*1024 (Full-sized chip)**
Matrix	3.15 mA	16.79 mA
Zero suppression and data buffering	12.47 mA	66.47 mA
Shared modules	46.82 mA	46.82 mA
Sum	62.44 mA	130.08 mA

Rolling Shutter Readout

Sheng DONG, Hulin WANG, Yunpeng LU

- Frame period (**Integration time**)
  - Event interval: 10 s
  - Count the frame numbers between 2 events
  - Frame period: **98.315 μs**
- Stability test
  - Hit number per event: 2048
  - Event interval: 110 μs
  - Data throughout: **595.8 Mbps * 39.3 s**

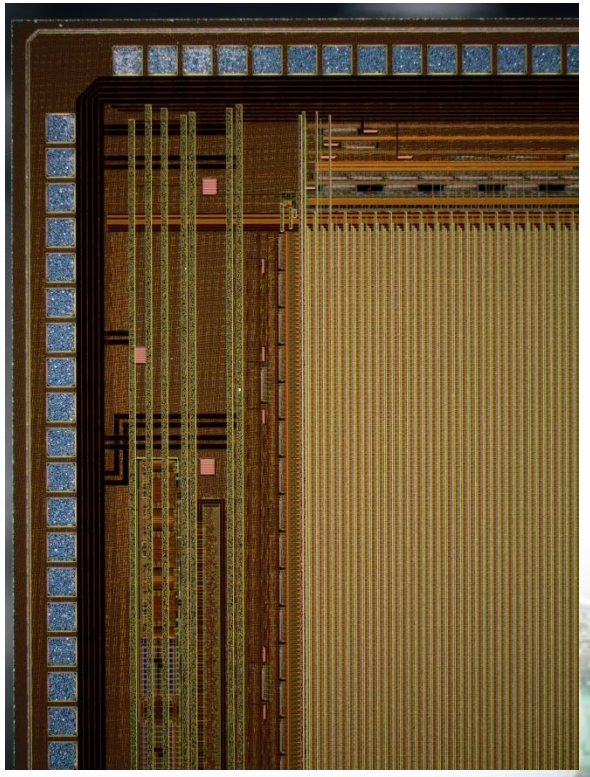




Summary

- JadePix3 is designed for the **double-sided** structure in line with the CDR study
  - Optimized for high resolution, low power and modest readout speed
- Performance **consistent with the design** targets
  - Low threshold and noise
  - Single point resolution 3 ~ 5 μm
  - Low power < 100 mW/cm^2
  - Integration time < 100 μs
- A success of collaboration and teamwork
  - Now working on the design of JadePix4

Microscopic view of JadePix3
(Top-left corner)



JadePix3 study group

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- SDU: Liang Zhang
- Dalian Minzu Unv: Zhan Shi

Acknowledgements

This work was supported partially by

- the National Key Program for S&T Research and Development (2016YFA0400400)
- the National Natural Science Foundation of China (11605217)
- the CAS Center for Excellence in Particle Physics (CCEPP)

Thank you for your time!