

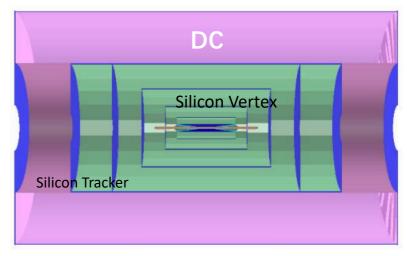
Particle identification with cluster counting technique for the drift chamber at CEPC

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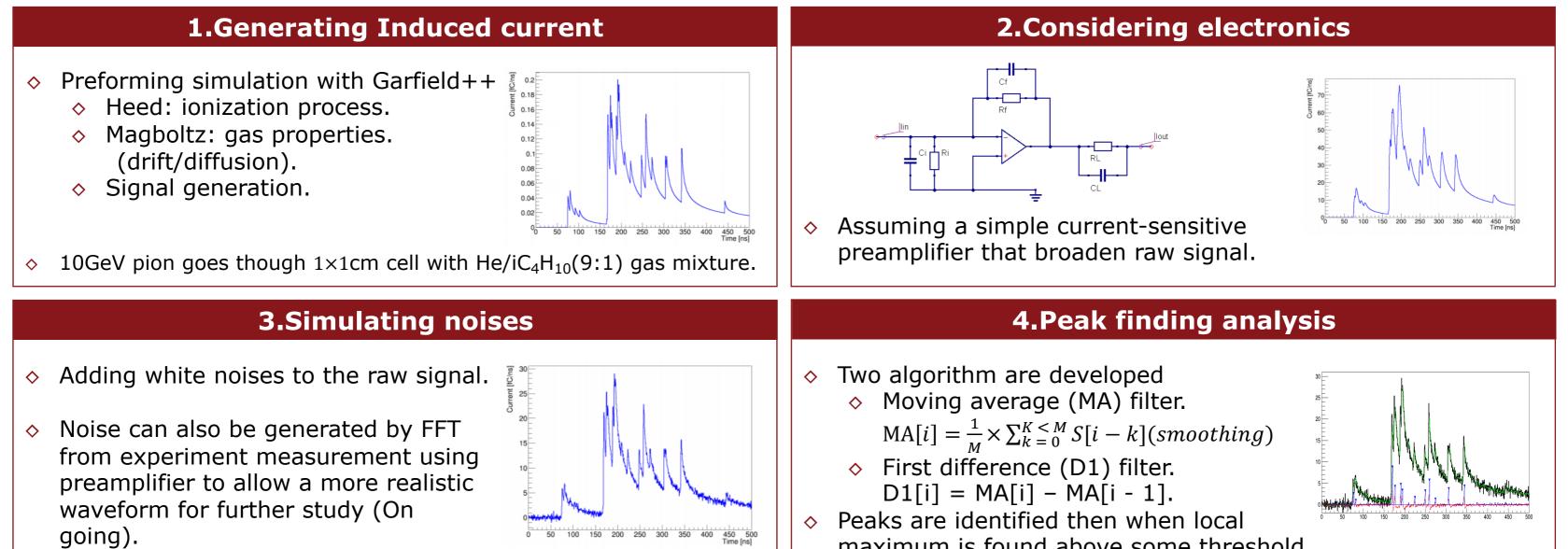
Introduction

One trillion Z bosons are going to be produced at the CEPC operated at Z-pole, which offers an unmatched opportunity for precision tests of the SM and searches for BSM physics for the flavor physics.

A good identification of charged kaons is essential for the flavor physics study and benefits the determination of jet flavor and jet charge at CEPC for Z-pole operation. To achieve these physics goals, a design of tracking system combining a silicon tracker and a drift chamber is proposed. The drift chamber could provide dN/dx measurements with cluster counting technique, as well as those of dE/dx.



The fourth conceptual detector design

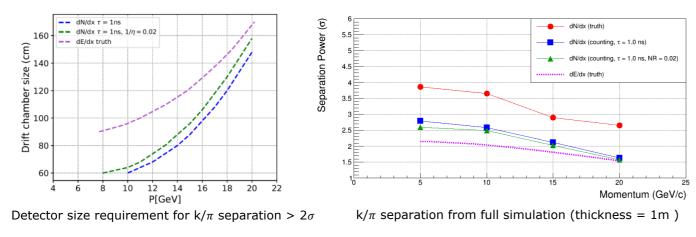


Full simulation method

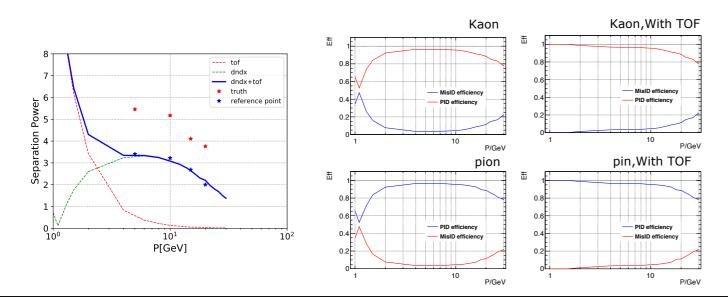
maximum is found above some threshold.

Performance study

- A fast simulation implemented in CEPCSW to replace time consuming full simulation enables the study of PID performance.
- To consider the degradation due to peak counting a effective \Diamond model is multiplied to primary ionization distribution. The counting efficiency is regarded as the function of number of clusters.



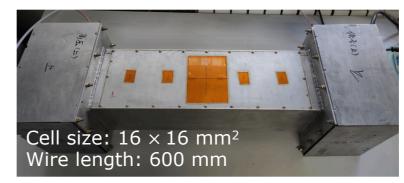
Combined with a TOF detector surrounded outer layer of \Diamond Drifter Chamber barrel at R = 1.8 m, with 50 ps precision, a PID performance result on K and π is given by fast simulation.



- Experiment setup \diamond
 - \diamond A 4 layer (6 cells/layer) prototype filled with He/iC₄H₁₀ (8:2).

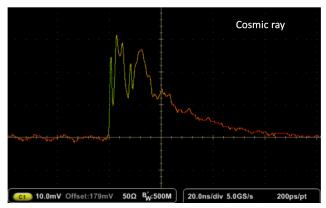
Prototype test

Read out by an oscilloscope connected to the preamplifier chip, LMH5401EVM Board.





- Signal with 1ns rise time can be \diamond observed.
- Gain is not enough to detect whole signal.
- ♦ Next plan : Change the R_f to improve the gain.



Summary

- A simulation workflow for the drift chamber with cluster counting method is ready. Preliminary results show that K/p separation can achieve 3(2) for 10(20) GeV/c with the thickness of DC about 1m.
- ♦ A fast simulation parameterized from full simulation is implemented and preliminary PID performances are studied.
- ♦ A prototype test system has been setup to validate the simulation and help to understand the requirements of electronics.