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Development of a SOI-3D pixel prototype for the CEPC vertex detector

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on behalf of the SOI-3D study group

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Outline

- ❖Introduction & overview of pixel sensor R&D
- ❖Introduction of SOI-3D process
- ❖Design of the CPV4-3D prototype
- ❖Summary, outlooks & acknowledgements

Introduction

◆ Physics motivation drives the required performance of the CEPC sub-detectors

Physics process	Measurands	Detector subsystem	Performance requirement
$ZH, Z \to e^+e^-, \mu^+\mu^-$ $H \to \mu^+\mu^-$	$m_H, \sigma(ZH)$ $\mathrm{BR}(H \to \mu^+\mu^-)$	Tracker	$\Delta(1/p_T) = 2 \times 10^{-5} \oplus \frac{0.001}{p(\mathrm{GeV}) \sin^{3/2}\theta}$
$H \to b\bar{b}/c\bar{c}/gg$	$\mathrm{BR}(H \to b\bar{b}/c\bar{c}/gg)$	Vertex	$\sigma_{r\phi} = 5 \oplus \frac{10}{p(\mathrm{GeV}) \times \sin^{3/2}\theta} (\mu\mathrm{m})$
$H \to q\bar{q}, WW^*, ZZ^*$	$\mathrm{BR}(H \to q\bar{q}, WW^*, ZZ^*)$	ECAL HCAL	$\sigma_E^{\mathrm{jet}}/E = 3 \sim 4\%$ at 100 GeV
$H \to \gamma\gamma$	$\mathrm{BR}(H \to \gamma\gamma)$	ECAL	$\Delta E/E = \frac{0.20}{\sqrt{E(\mathrm{GeV})}} \oplus 0.01$

Impact parameter resolution

◆ High spatial resolution, low material budget and fast readout pixel sensors constructed vertex detector required by the flavor tagging

Physics driven requirements	Running constraints	Sensor specifications	
$\sigma_{s.p.}$ 2.8um		Small pixel	~16 μm
Material budget 0.15% X_0/layer		Thinning to	50 μm
	Air cooling	low power	50 mW/cm^2
r of Inner most layer 16mm	beam-related background	fast readout	~1 μs
	radiation damage	radiation tolerance	≤3.4 Mrad/ year ≤6.2×$10^{12}$$n_{eq}$/ ($cm^2$ year)

Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector, http://cepc.ihep.ac.cn/

Overview of R&D activities

◆ Step #1: **Optimize the key performances** of pixel sensor with **current technologies**

➢ 200 nm SOI technology

- CPV1/2/3 Dr. Jing Dong' talk today

➢ 180 nm CMOS technology

- JadePix1/2/3/4, MIC4

Dr. Yunpeng Lu' talk today

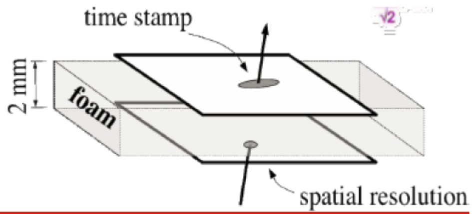
Spatial resolution: *3-5 μm*

Time resolution: *1- 100μs*

Power consumption: *50 -100 mW/cm²*

Thinning: *50μm for CMOS; 75μm for SOI*

Radiation tolerance: *~ 1Mrad*



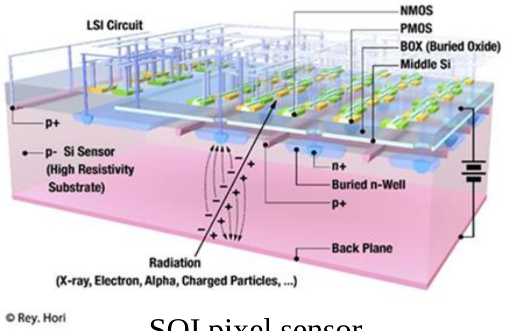
ILD-like double-sided concept without power-pulsing mode

◆ Step #2: **explore new technologies**

➢ 3D technology

- SOI-3D process: CPV4-3D this talk

- *Contradiction of more in-pixel functionalities vs fine spatial resolution*
- *Sensor & circuits technology could be different*
- ……



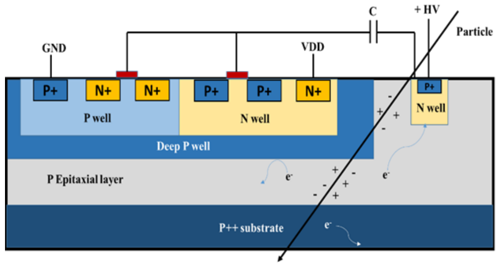
SOI pixel sensor

➢ Advanced process technology: 65nm or below

potentially lower power consumption; smaller pixel size or more in-pixel functionalities

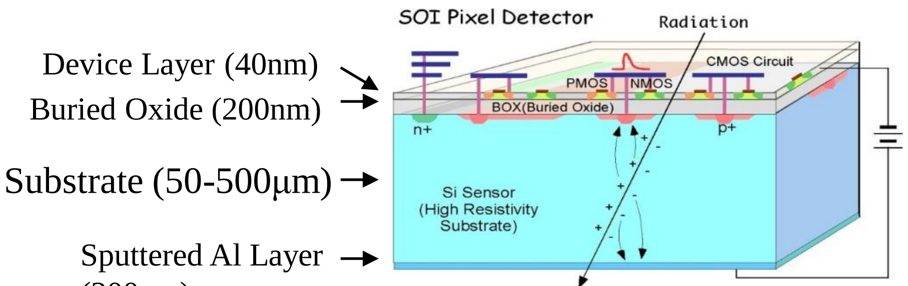
➢ Stitching CMOS technology: *potentially ultra light detector structures*

On going



CMOS pixel sensor

Introduction of SOI-3D process



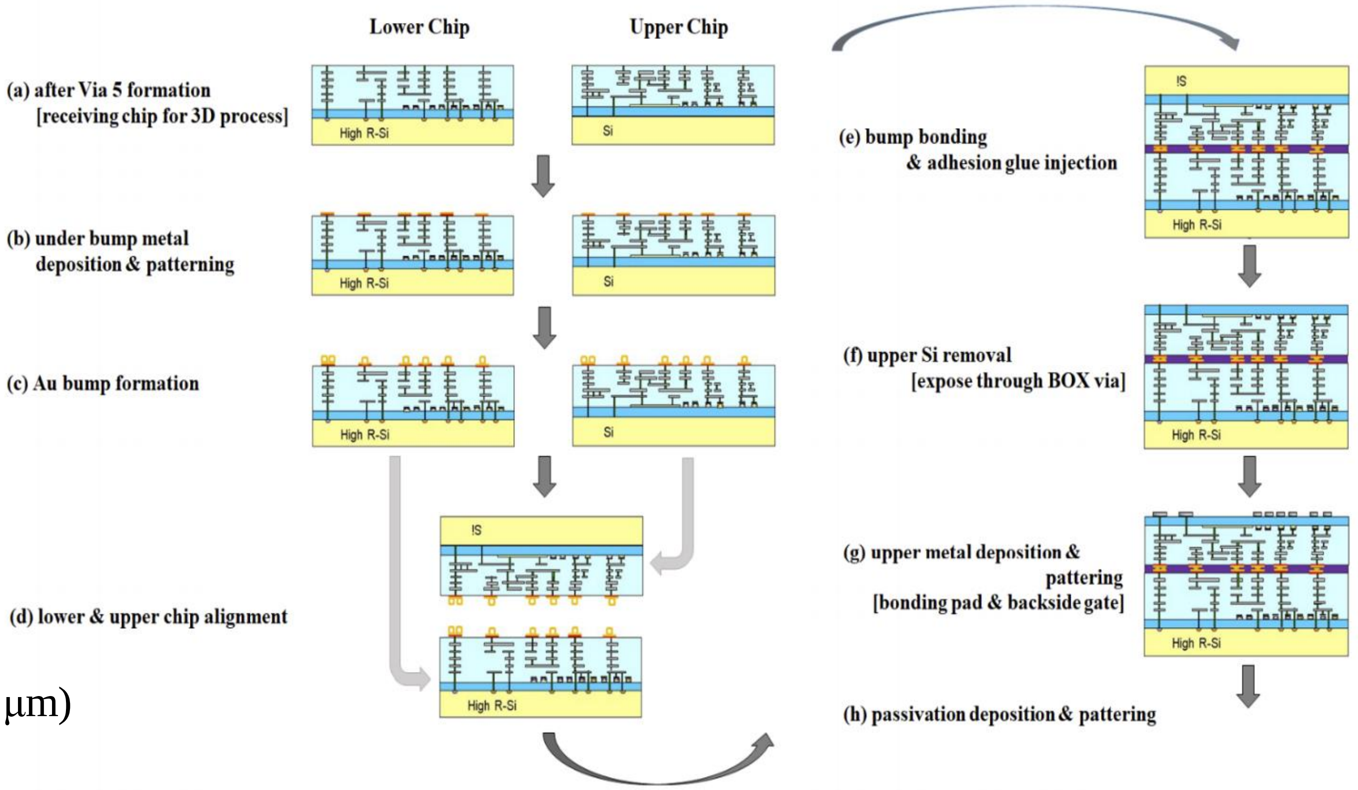
Sandwiched structure of SOI

SOI: Silicon-on-Insulator technology

- Utilize 0.2μm FD-SOI CMOS process by lapis Semiconductor Co. Ltd.

SOI pixel detector: monolithic type detector

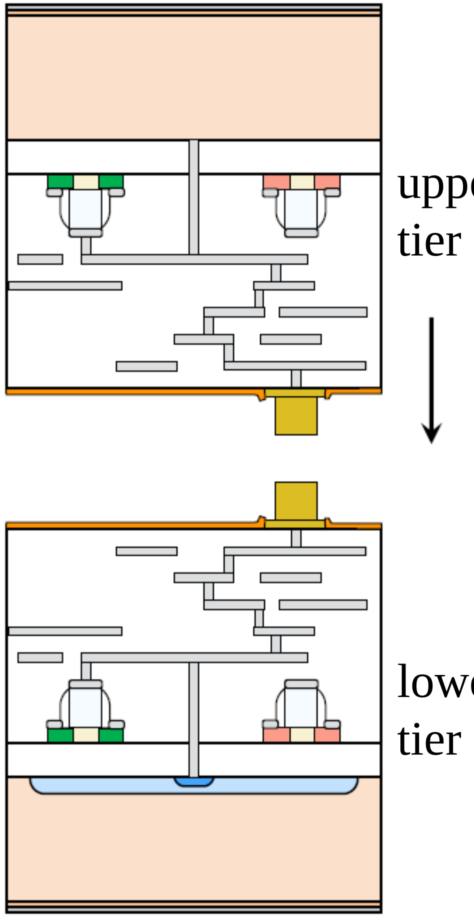
- High resistivity （>1 kΩ·cm）， thick (50-500 μm) sensitive layer; *more signal charges*
- Fully depleted (high basing voltage); *fast collection*
- *Low power dissipation*
- Almost no single event effects (SEE) probability; *radiation tolerance*



3D chip stacking process flow proposed for detectors using in High Energy physics Experiments

*@*Ikuo Kurachi， et all, Oct.7, Vertex 2020*

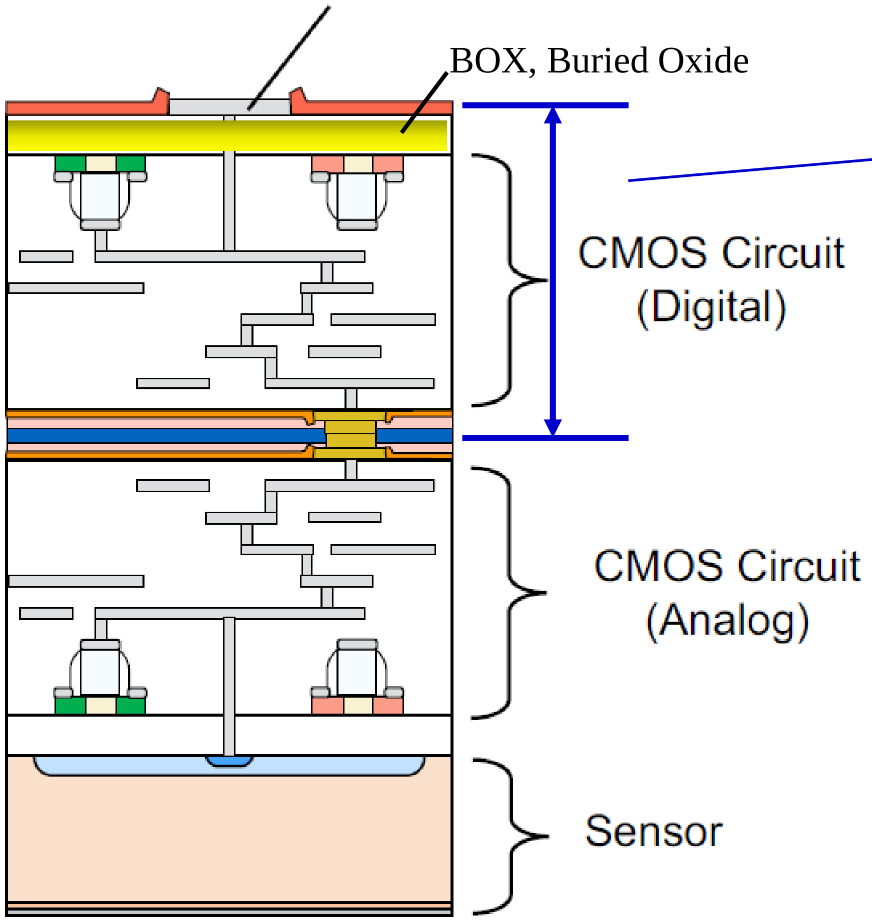
Introduction of SOI-3D: design resources



- Shrinking pixel size always pushed to the physical limit
  - **0.35μm CMOS process:** ~10 transistors and 6 metal layers, pixel size ~ 20*20 μm^2
    @ ALTIMATE for STAR, ~ 2000 - 2014
  - **0.18μm CMOS process:** ~100 transistors and 6 metal layers, pixel size ~ 26*28 μm^2
    @ALPIDE for ALICE, ~ 2014 - 2021
- 0.2μm SOI-3D process: ~100 transistors and 5 metal layers **in each tier**
  - lower tier: sensing diode and analog front-end
  - upper tier: digital readout
  - **Pixel size can be cut half without compromise of functionality**

**Credit of the conceptual drawing: Miho Yamada*

Introduction of SOI-3D: minimum increase of material

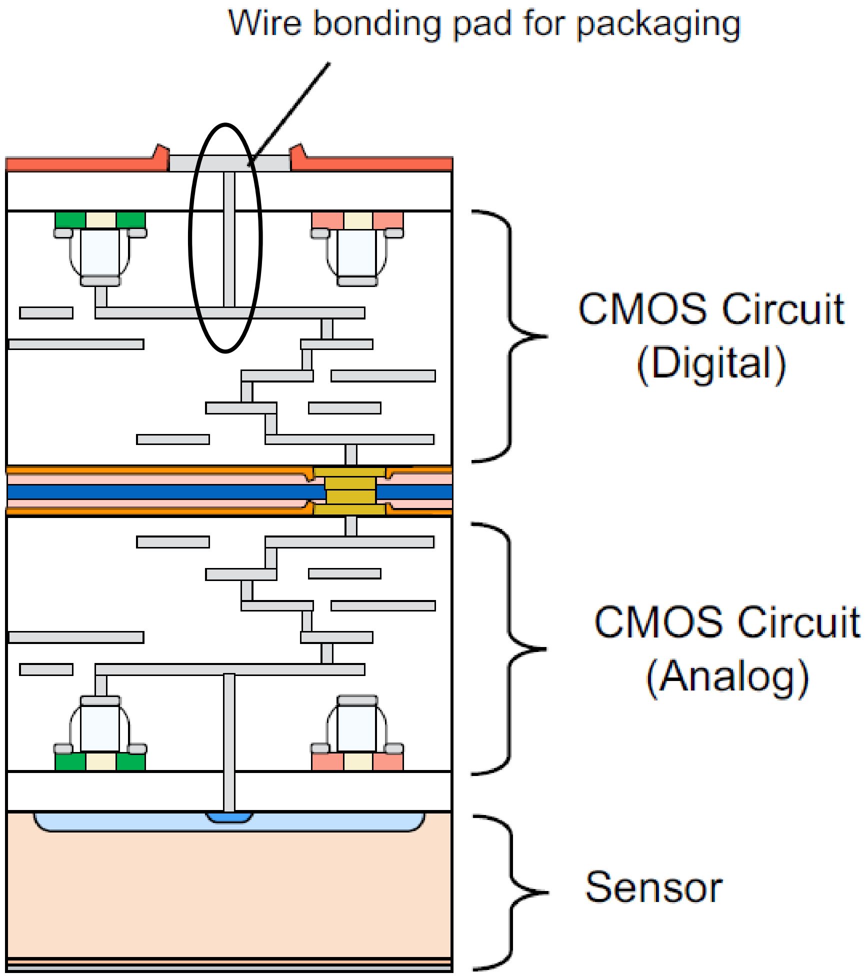


**Credit of the conceptual drawing: Miho Yamada*

- ◆ The bulk of upper tier is **removed by wet-etching**
  - Thickness of upper tier: 260 μm → ~10 μm
  - Wet-etching stopped by the box layer automatically, which makes SOI quite compatible with 3D integration
- ◆ Lower tier can be thinned as a conventional sensor
  - 75 μm in SOI case and 50 μm in CMOS case (lower tier not necessarily an SOI sensor)

** Currently SOI-3D demonstrated on a lower tier of 260 μm thick*

Introduction of SOI-3D: backside connections



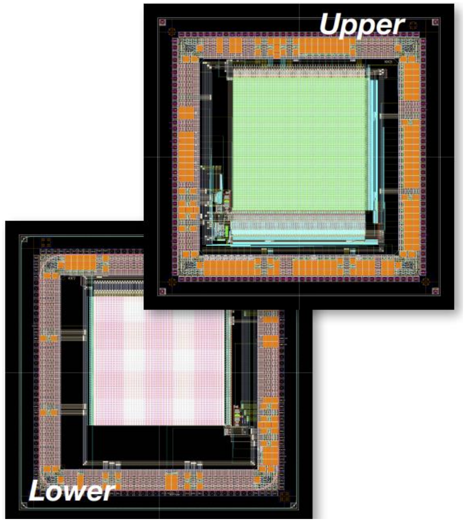
**Credit of the conceptual drawing: Miho Yamada*

- Backside connection is Through Box Via (TBV)
  - 0.32 μm hole which implemented already in the SOI process
  - Smaller than Through Silicon Via (TSV) hole by a factor of 10
  - Additional metal layer formed for the bonding pad

Introduction of SOI-3D: frontside connections

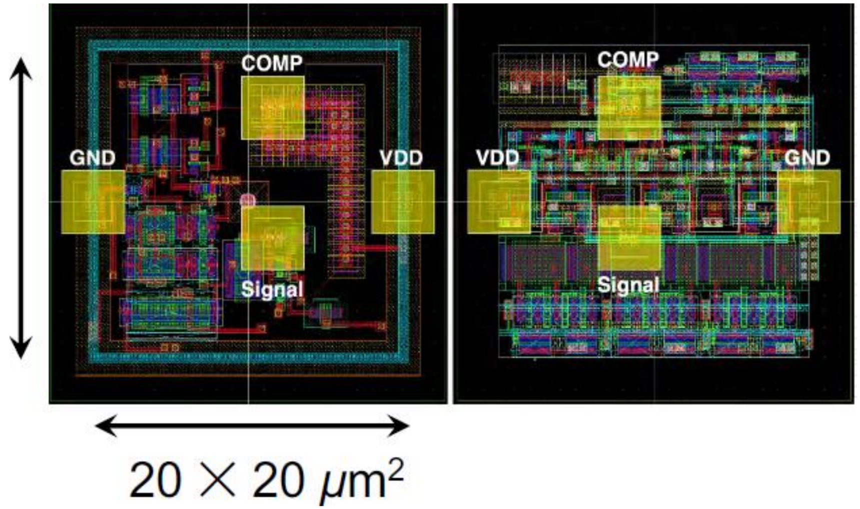
- 3 μm diameter cylindrical Au bump

  Multiple vertical connections per pixel, necessary and feasible

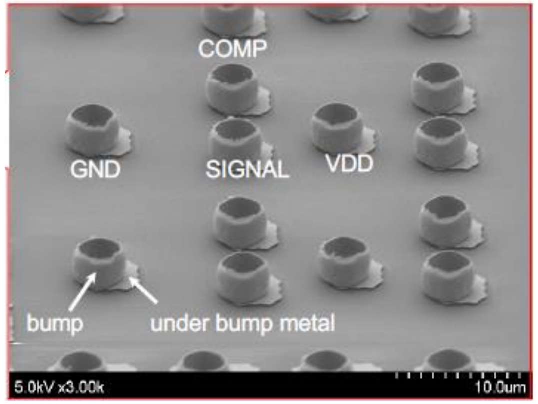


Layout of SOFIST4 designed by KEK for ILC. Evaluated at 2020

lower pixel upper pixel



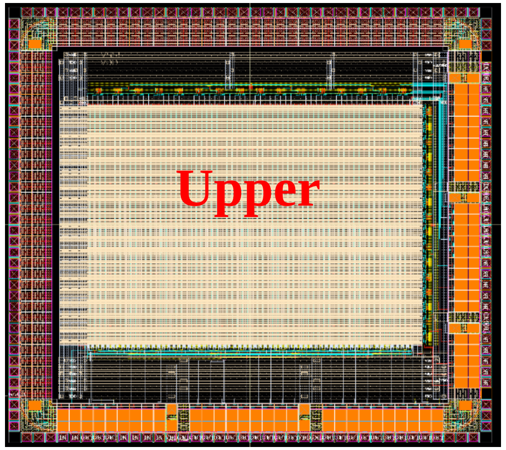
Au bumps

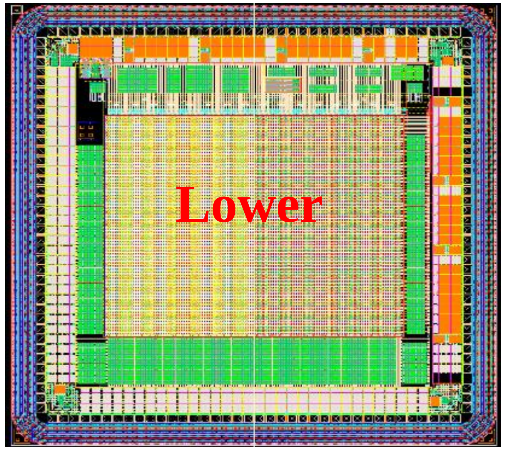


SEM image

4 connections per pixel: power/ground, analog signal and comparator output in the SOFIST4 by KEK, first demonstration of SOI-3D process.

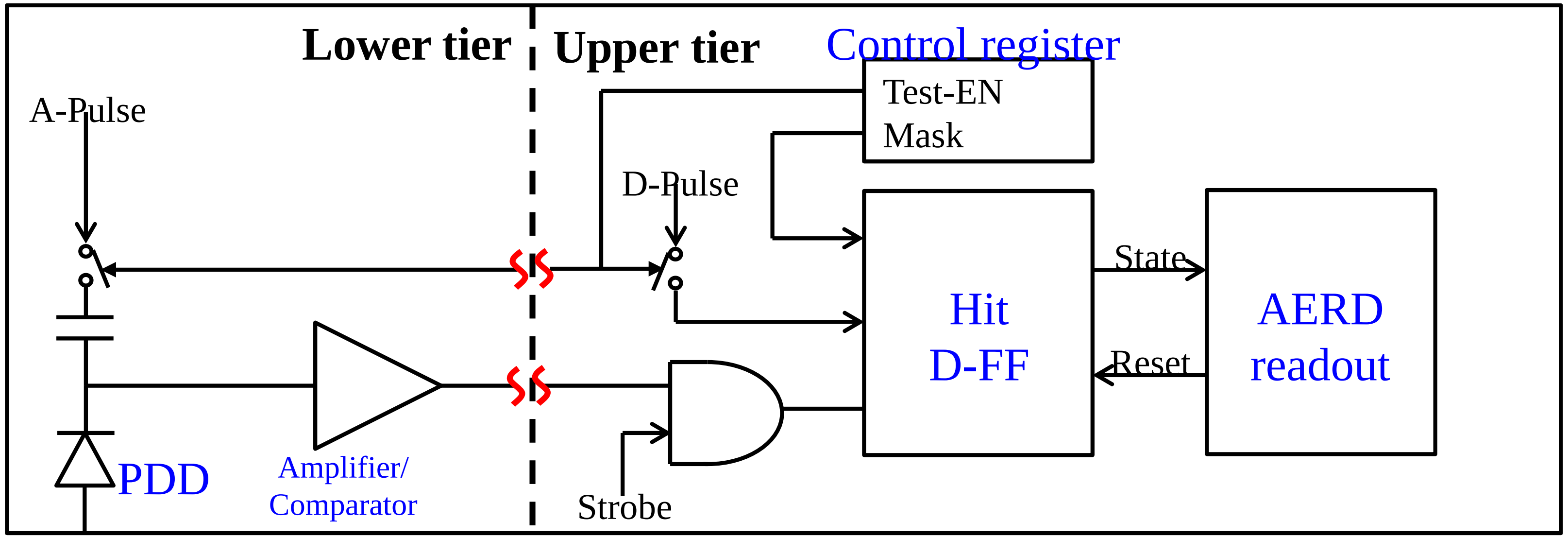
CPV4-3D: prototype sensor overview





Layout of CPV4-3D

Division of upper and lower functionalities

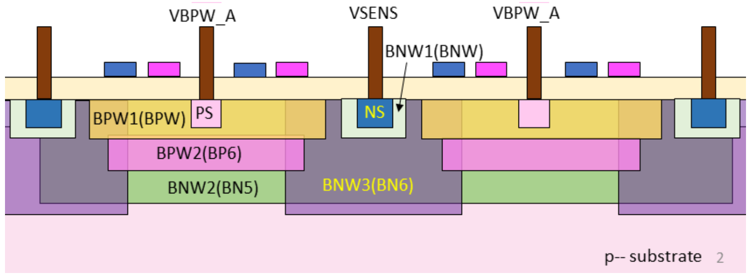


Pixel size	17.24×21.04 μm^2
Time resolution	~1 μs or ~3 μs in different operation mode
Pixel array	128×128
Chip size	4.5mm×4.5mm
Delivered	Nov. 2020

- Lower tier: PDD sensing diode + amplifier/comparator
- Upper tier: Hit D-Flipflop + Control register + AERD readout
- **2 vertical connections** in each pixel: comparator output and test switch;
- Analog and Digital power/ground are also separated

CPV4-3D: PDD sensing diode system

CPV4-3D employs the PDD (Pinned Depleted Diode) sensing diode system for charge collection



Schematic view of PDD diode structure.

Composed of several layers of doped structures with different depths interface:

- Sensing node (NS) and the buried n-well (BNW1) form a charge collector;
- BPW1:shielding layer between circuits and the charge collector;
- BNW2, BPW2, BNW3 form a lateral gradient electrical field, benefit to charge collection efficiency;
- High negative voltage is backside applied to obtain a fully depleted substrate.

◆ Not 3D-specific, but the most active part of study in SOI pixel **sensor** technology

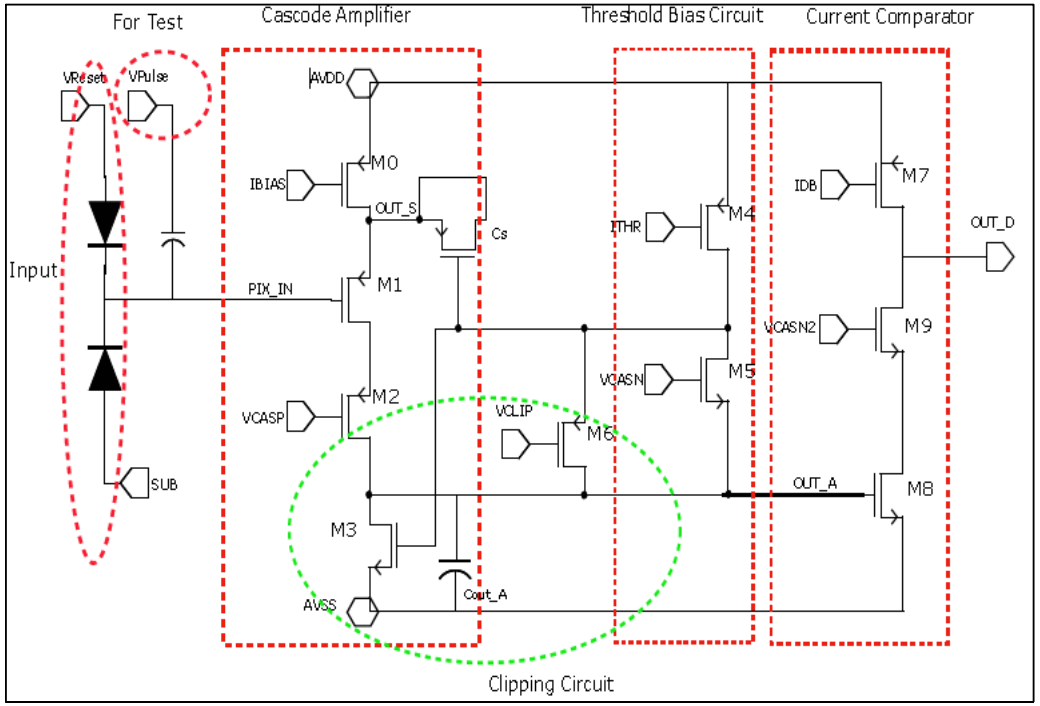
- Evolution of years' development: BPW, Nested-wells, Double SOI, and PDD (Pinned Depleted Diode)

◆ **All-in-one solution** in the sensor part:

- Control back-gate of transistors
- Maximize charge collection efficiency
- Suppress leakage current of Si-SiO_2 interface
- Minimize the capacitance of electrode (Cd)
- Shield the capacitive coupling between the sensor and pixel circuit

Detail of PDD structure characterization results shown by Dr. Jing Dong's talk today

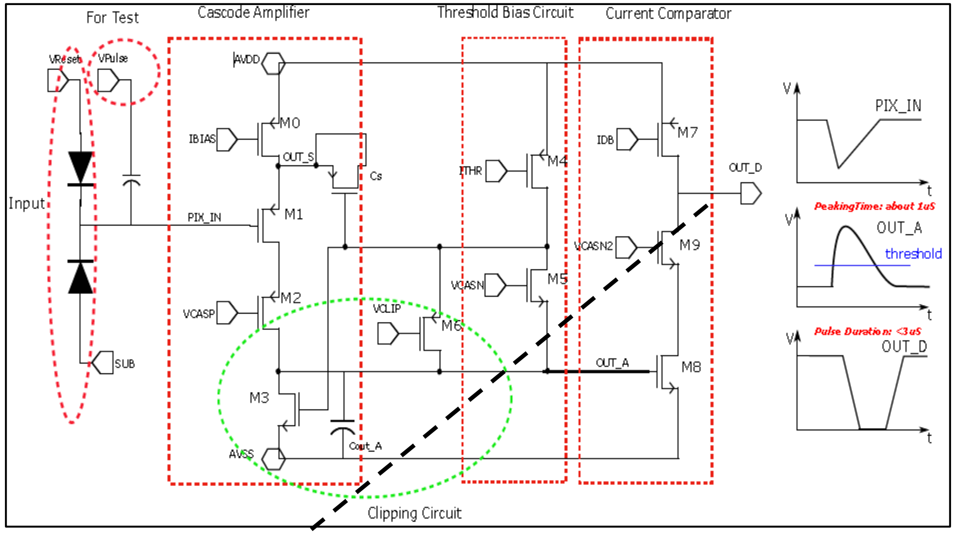
CPV4-3D: Lower tier pixel

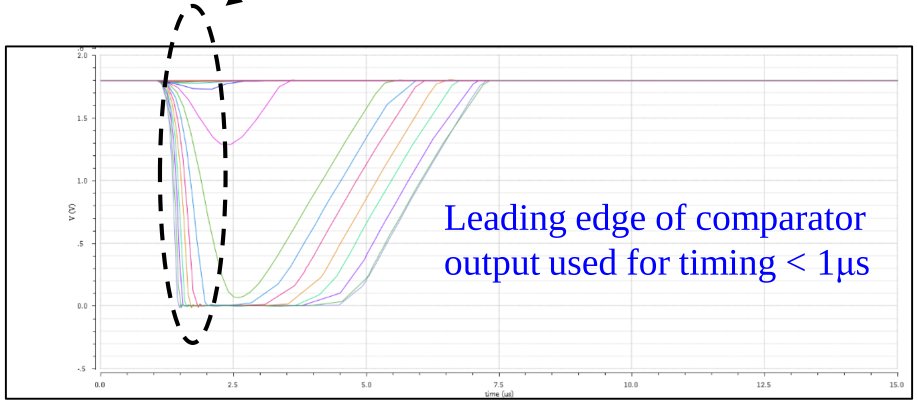


Pixel schematic of CPV4-3D lower tier. The *structure original from ALPIDE designed by CERN for ALICE*

- **Lower tier pixel integrate the functions of**
  - Charge collection;
  - Amplification;
  - Digitization;
  - Threshold tuning;
  - Structure for pulse inject test;
- -4V on the **back-gate** of MOS transistors required (BPW shown last page) in order to minimize electrode capacitance Cd.
  - Vth decreased 70 mV for PMOS and increased 50 mV for NMOS
  - Characterized and modeled in HSPICE by KEK
- Influence on the front-end assessed
  - Current mirror matched and placed in a -4V N-well (Counter-part branch of M0, M4, M7)
  - The other transistors compensated by proper offset on their bias voltage (VCASN e.g.)
  - **Confirmed by simulation**

CPV4-3D: Lower tier pixel





◆ **Transistor size** selected according to ALPIDE design* to minimize FPN as a first order approximation

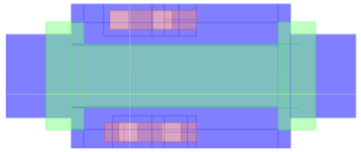
Transistor	M0	M1	M2	M3	M4	M5	M6	M7	M8	M9
W/L	1.8/8.5	1/0.4	1/0.4	1/5	2/8.05	0.63/4.94	0.63/3	1/5	1/0.4	1/1

◆ Simulation results of **threshold and noise**

	Threshold	Gain@Thr	Vnoise@Thr	ENC
Pre-layout	75 e^-	32mV/10e^-	4.33 mV	1.34 e^-
Post-layout	**125 e^-**	8.6mv/10e^-	2.92 mV	**4 e^-**

◆ TID radiation enhancement

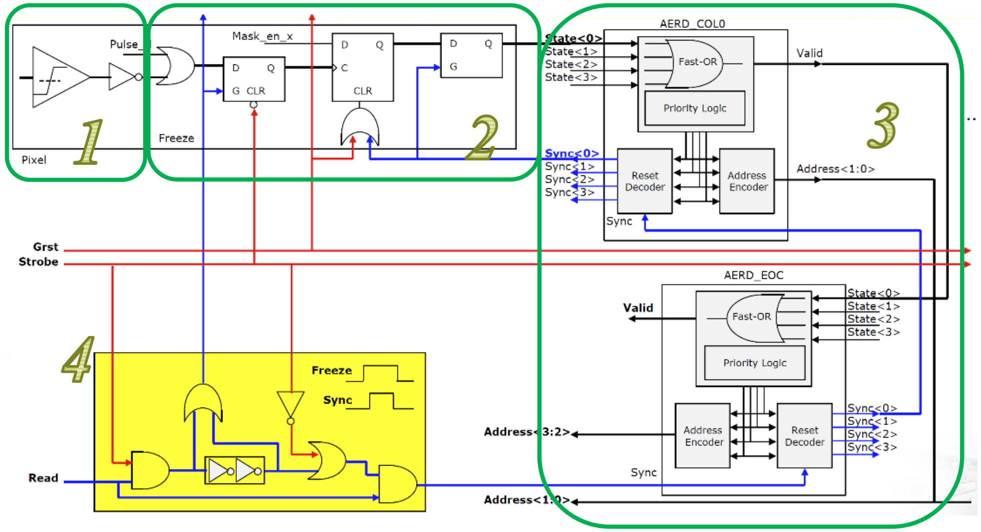
- Smallest working current path at M5 = 0.5nA, the same order of magnitudes with leakage after radiation (TID: ~1-10 Mrad)
- H-gate transistors used for M5 in test pixels for TID
- Compensation of TID-induced Vth shift to be applied on the BPW layer



H-gate NMOS layout used in this design

*Ref: D. Kim et al., 2016 JINST 11 C02042

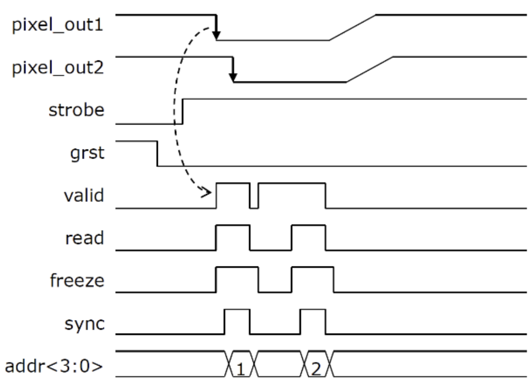
CPV4-3D: upper tier



Data readout structure (simplified) of CPV4-3D

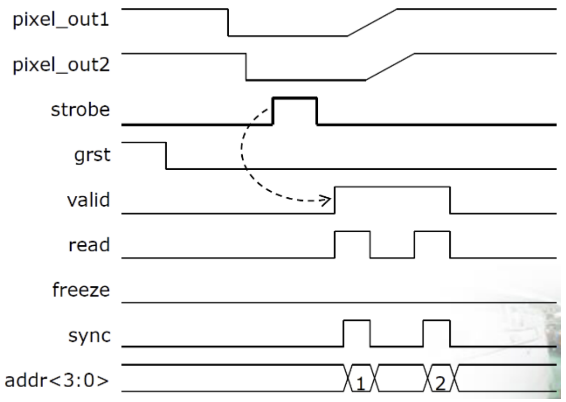
Continuous readout mode:

- Strobe == 1;
- Timing by falling edge ~ 1μs resolution
- New hits are freeze while reading



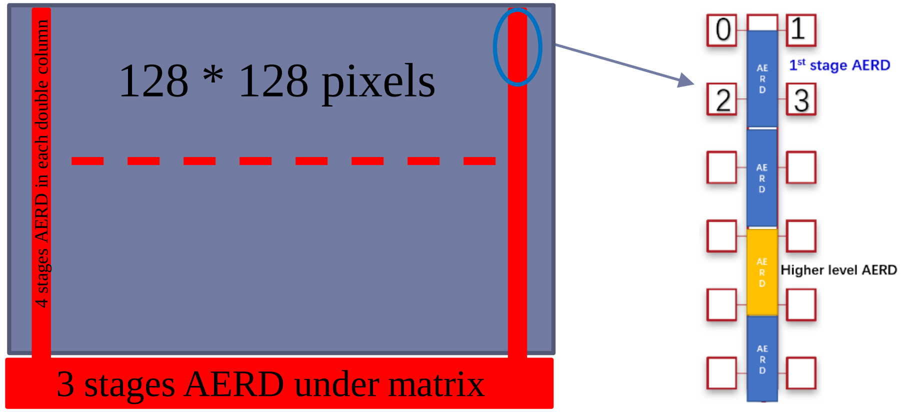
Triggered readout mode:

- Strobe as gate signal;
- Timing by trigger ~ 3μs resolution
- Read after trigger



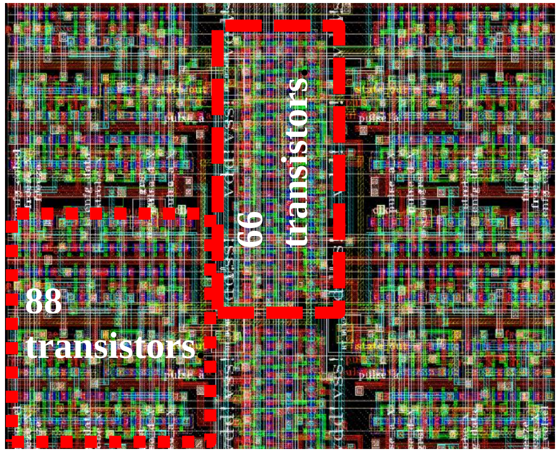
1. Lower tier pixel: convert hits information into digital signals
2. Upper tier pixel: Hit D-Flipflop + Control registers (Musk/D_test/A_test/hit_response)
3. Data-driven readout (Asynchronous Encode Reset Decode*)
   - 4 stages AERD in each double column for 128 rows
   - 3 stages AERD under matrix for 64 double columns
4. SYNC/FREEZE generation block: outside the matrix
   - Continuous readout mode
   - Triggered readout mode

*Ping Yang, NIMA 785 (2015) 61-69

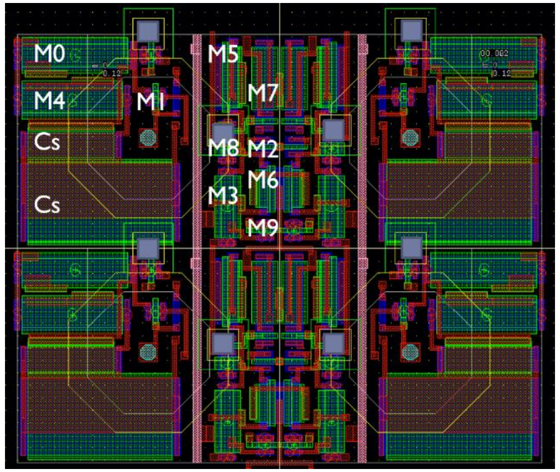


14-bit output for fired pixel address information

CPV4-3D: layout implementation

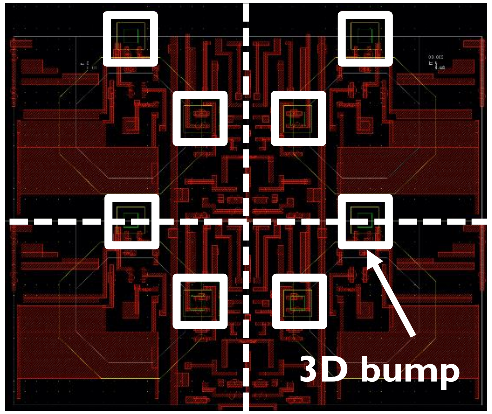


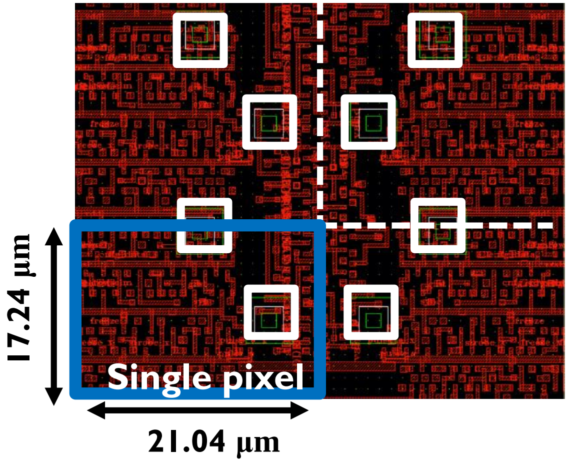
Layout of 2*2 pixels in upper tier



Layout of 2*2 pixels in lower tier

- A lot of efforts to minimize the layout size: 21.04 μm * 17.24 μm
  - Upper tier: 88 transistors for in-pixel control registers;
    66 transistors for a single stage of AERD;
  - Lower tier: Compromise between noise and transistor size;
    Y-axis mirrored, sensitive input node protected against the output node to minimize the crosstalk





3D bump positions in 2*2 pixels of upper and lower tier (Metal_1 only).
2 bumps for each pixel (Comparator output & test switch)

Summary and outlooks

Exploration of SOI-3D has started with the first prototype of CPV4-3D

- Targeting on the full specs of pixel sensors:
  - Spatial resolution: pixel size ~ 17×21 μm^2 *(~1/2 area of 26*28 μm^2)*
  - Time resolution: ~ 1μs;
  - Power dissipation: ~50mW/cm^2;
  - Material budget: could be thinned down to (75+10) μm; or possibly to (50+10) μm；
  - Radiation tolerance: TID tolerance enhanced design; initially less SEE benefits from SOI process.
- Sensors have just received; lower/upper tier separate test is preparing;
- To examine the scheme, implementation and yield of SOI-3D;
- 2 ~3 MPW run planned in 5 years

Acknowledgements

This work is supported by

- The National Natural Science Foundation of China (11935019);
- The State Key Laboratory of Particle Detection and Electronic (SKLPDE-ZZ-202010)

谢谢大家！

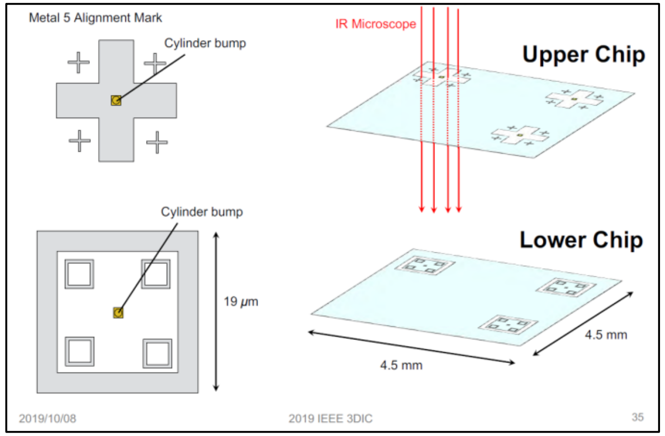
backups

Dummy 3D bumps

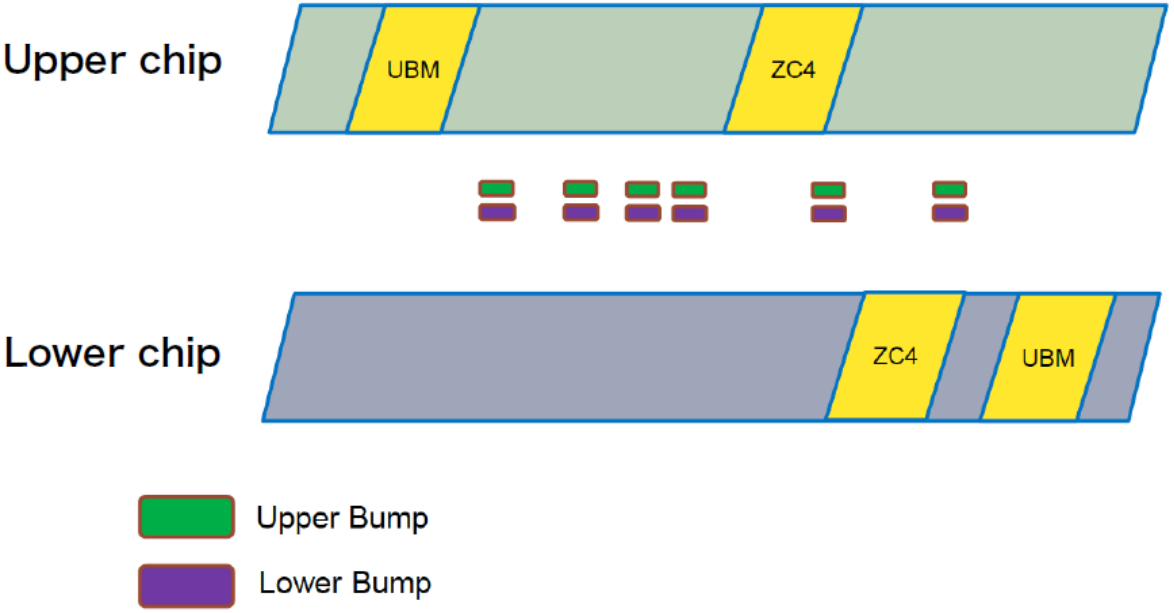
- Dummy 3D bumps, to **relieve the mechanical stress** of upper tier
- Generated automatically in the user-designated area

- Excluded area for the dummy 3D bumps
  - The pixel matrix
  - The p-stop of guard ring
  - The alignment marks

Alignment marks



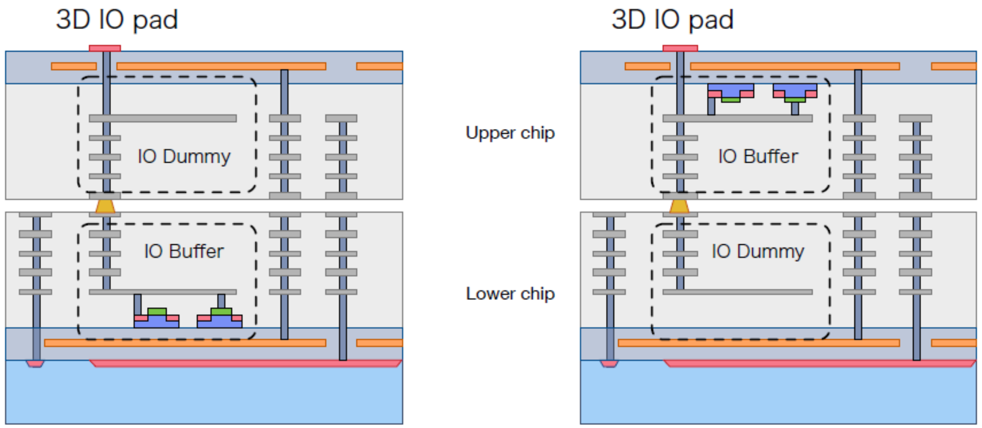
dummy 3D bumps avoids UBM and Masking ZC4



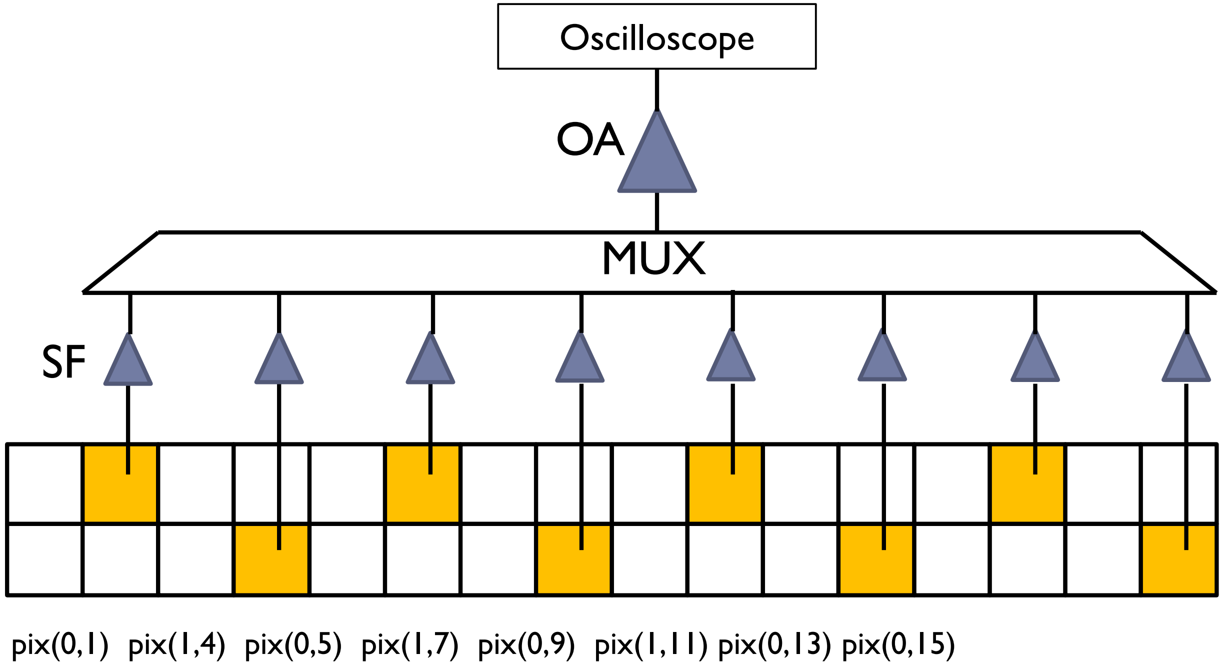
Design for test

- Signal and power access to the chips
  - Conventional IO pad equipped on both lower and upper chips, **accessible before 3D integration**
  - Functional IO always stacked up with dummy IO to avoid conflicts of buffers

Configuration for the signal of lower tier(left) and upper tier(right)



- Internal signal waveform are routed out of test pixels and buffered for oscilloscope observation
  - **Internal node** OUT_A and OUT_D
  - Two-stage buffers: Source-Follower and Operational Amplifier

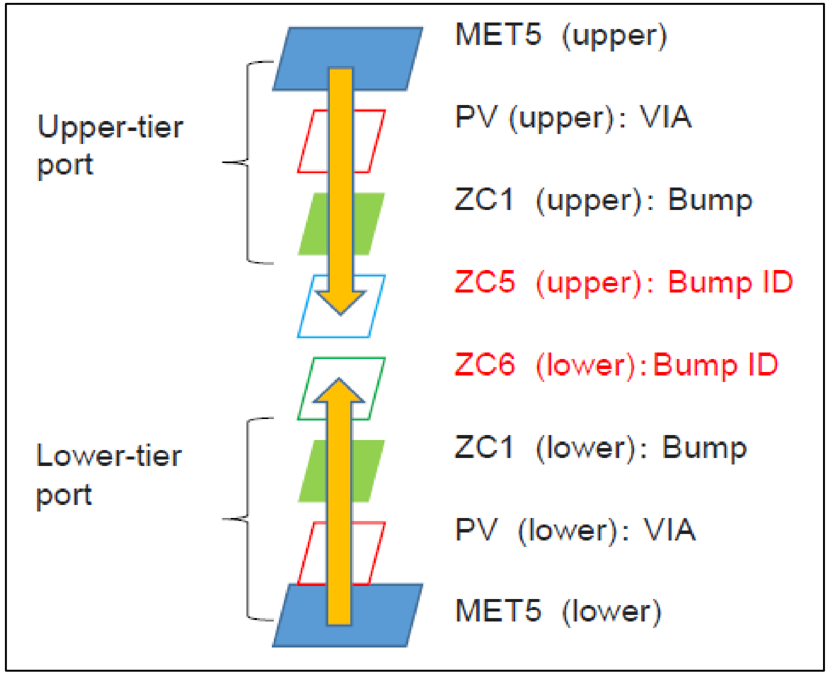


Design flow established

Conventional SOI tape-out plus a special 3D add-on process

- Upper and lower chips manufactured with the LAPIS 0.2um process
- Chip-to-chip 3D integration implemented by T-Micro originated in Tohoku-U.
- **Driven rules** of 3D design and verification integrated into the EDA tools

stack-up of 3D layers



flow chart of SOI-3D design