Characterization of SOI pixel sensor （CPV3） using pinned depleted diode structure for CEPC Vertex

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Outline

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2. Pinned Depleted Diode(PDD) sensor
3. CPV3
    - CPV3 PDD/chip
    - Method to test capacitance
    - Measurement setup
    - Characterization results
4 .Summary

1. Introduction

Compact Pixel detector for Vertex (CPV) series chips

- Using Lapis 200nm Silicon-On-Insulator(SOI) [1] process
- Significant efforts have been put to meet the unprecedented requirements on the vertex resolution.

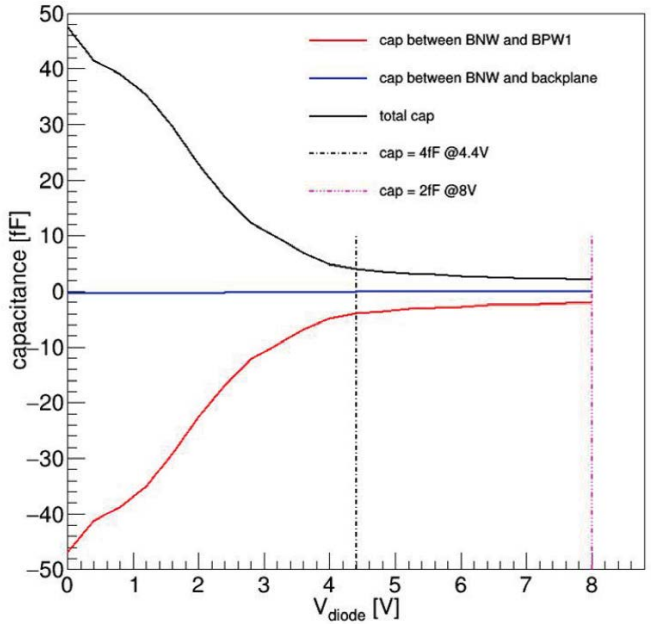
  - *The CPV2 prototype*， Double-SOI process， tested at 2017 autumn, achieve single point resolution below 3 μm with an infrared laser beam[2]. -*The first milestone*.

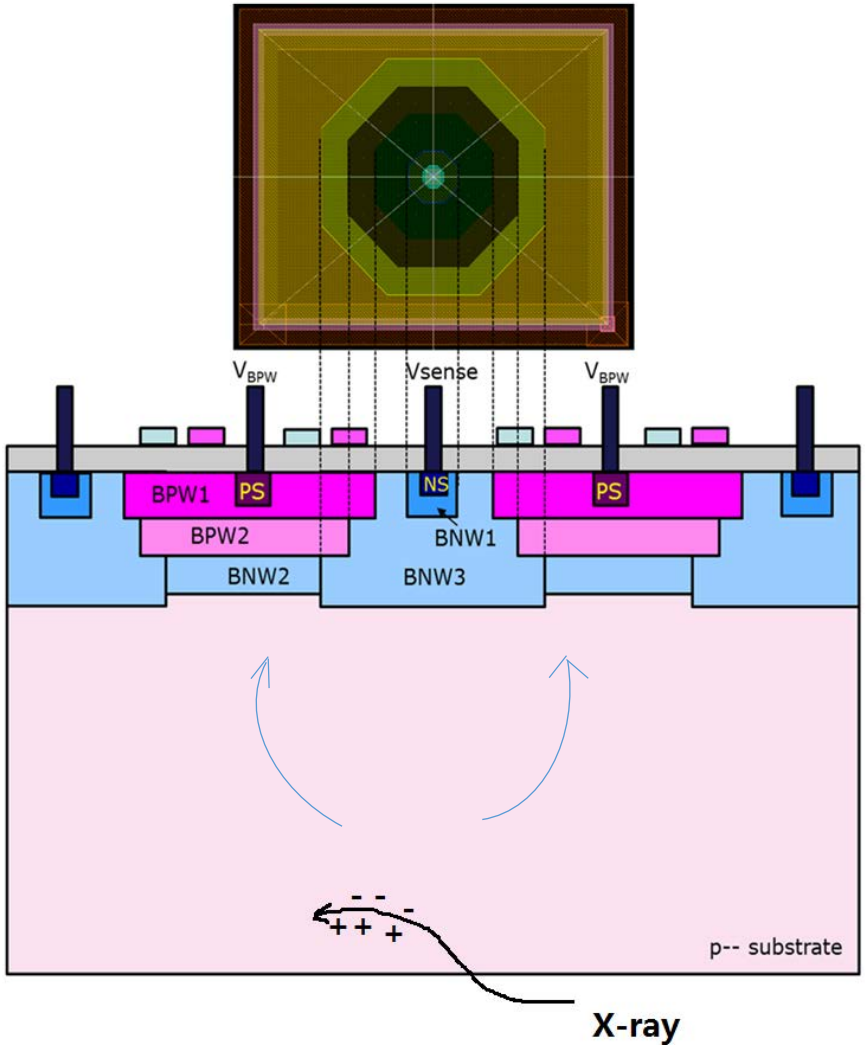
  - *The CPV3 prototype* ， *using a* new SOI-PDD process.
    - The equivalent input capacitance should be improved and studied in detail.
    - *This talk* is to present the characterization including Diode capacitance, parasitic capacitance.

  - *The CPV4 prototype, SOI-PDD,* the choice of PDD design in the CPV4 chip has been done based on results. -*Dr. Zhouyang's talk*.

2. Pinned Depleted Diode(PDD) sensor[3,4,5]

- **A new generation of sensor process developed in 2017**
  - **Blocks the contact with the Si-SiO2 interface, reducing the leakage current**
  - **A lateral gradient electrical field, which is beneficial to the charge collection efficiency.**
- **A reverse bias voltage of < -4V is necessary between the collection node and the shielding layer [Buried P-Well(BPW)]**

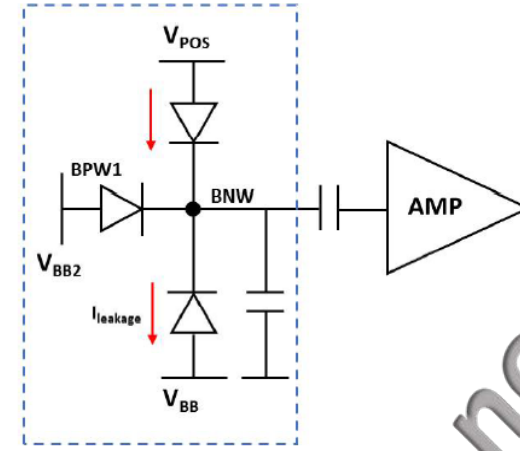


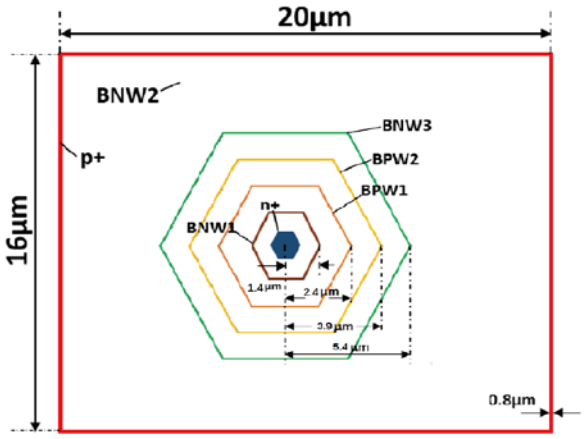


The schematic view of the PDD diode structure

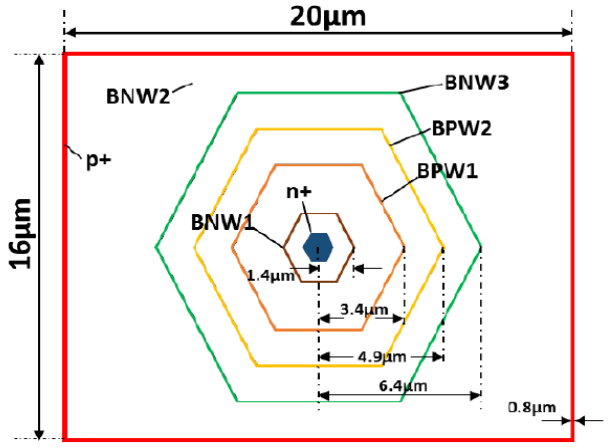
3. CPV3
CPV3-PDD structure

- *Three different sensor-structures have been designed.*
  - Potential of collection node set by Vpos
  - AC coupled to the AMP

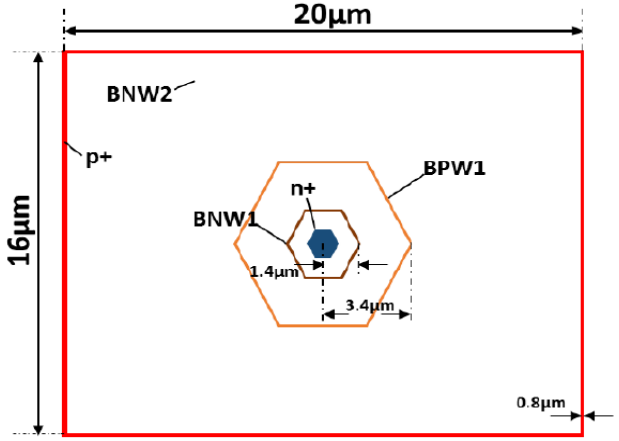




CPV3-PDD1: multi-layers structure



CPV3-PDD2: multi-layers structure



CPV3-PDD3: the simplified structure of CPV3-PDD2.

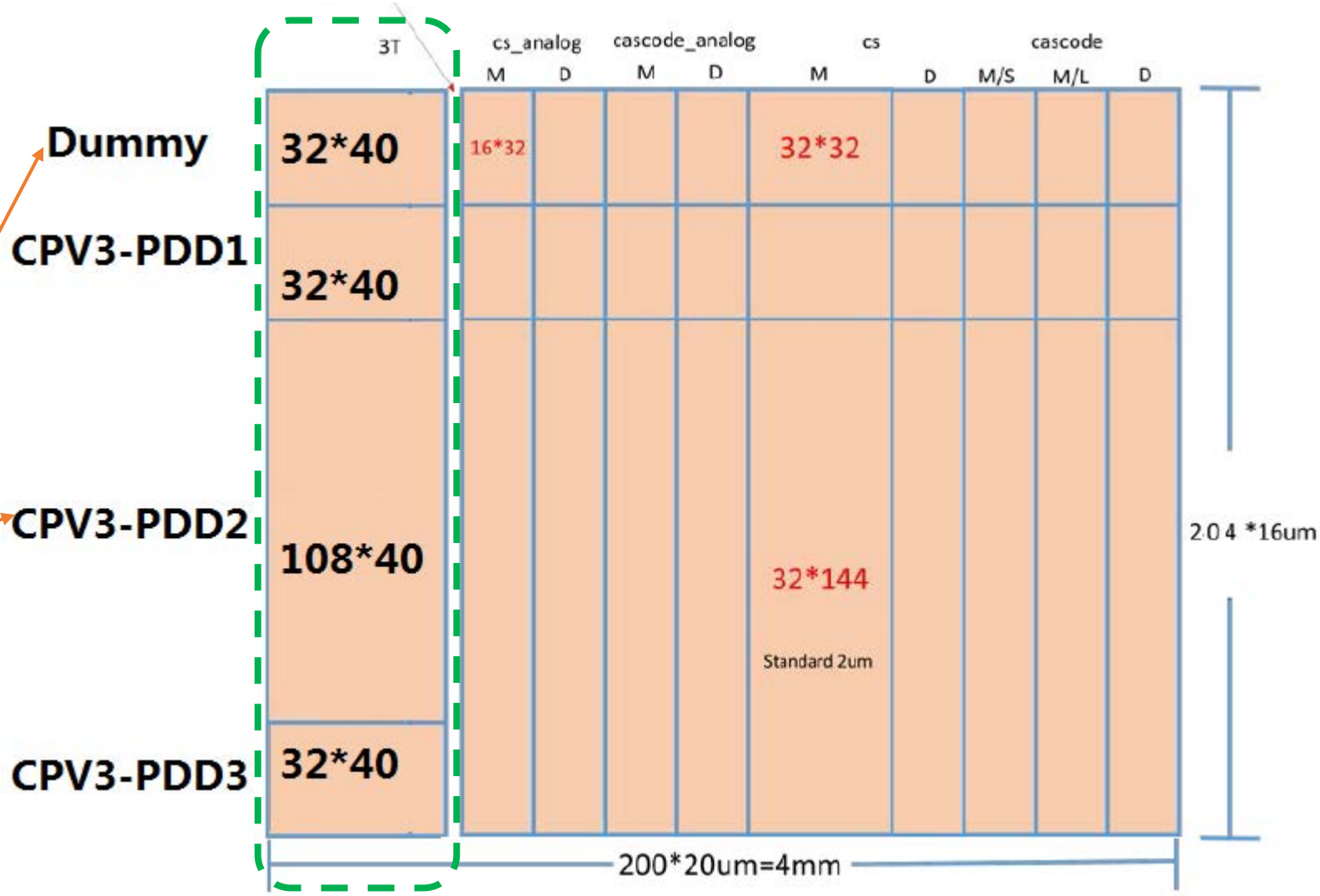
CPV3 chip

Active area: 4 × 4 mm²
310 μm thickness

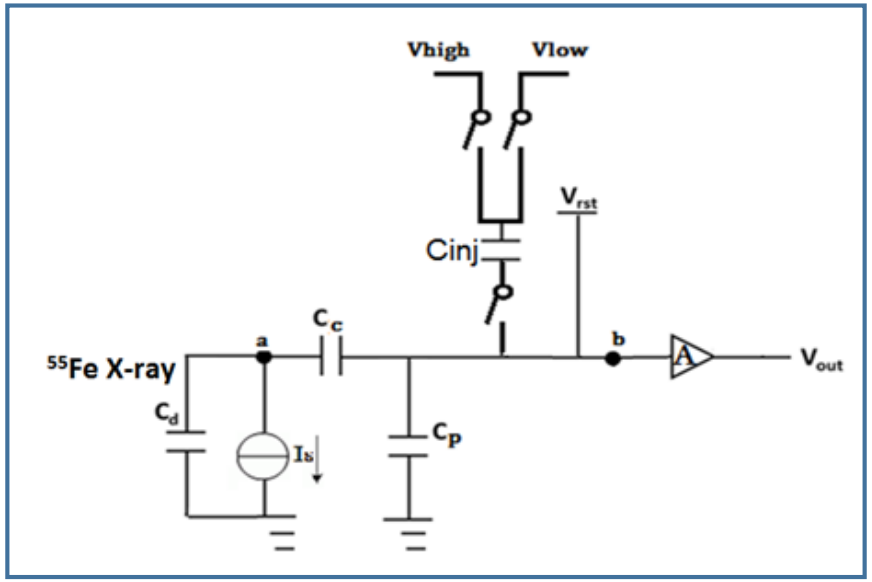
Dedicated test array of PDD sensor is placed consisting of 204 × 40 pixels.

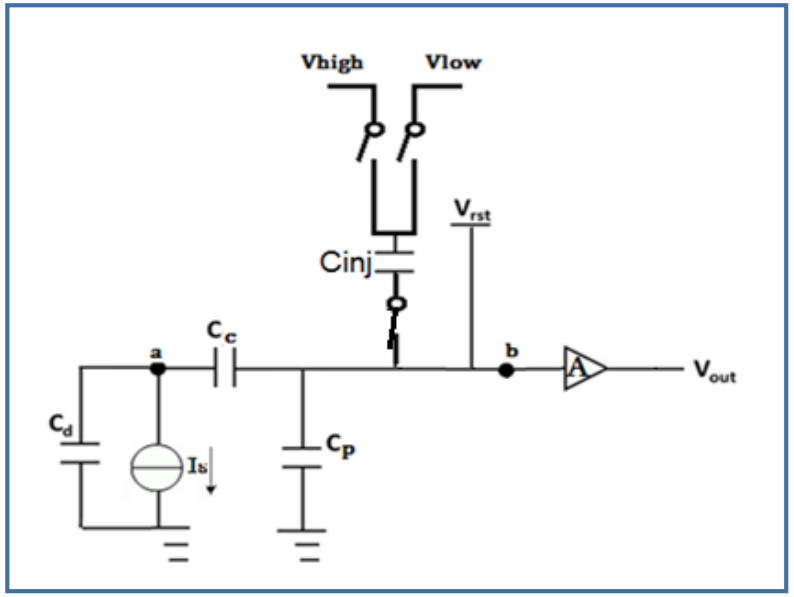
- A dummy' collection node broken off with its amplifier
- 1 submatrix baseline design
- 2 submatrix of variants

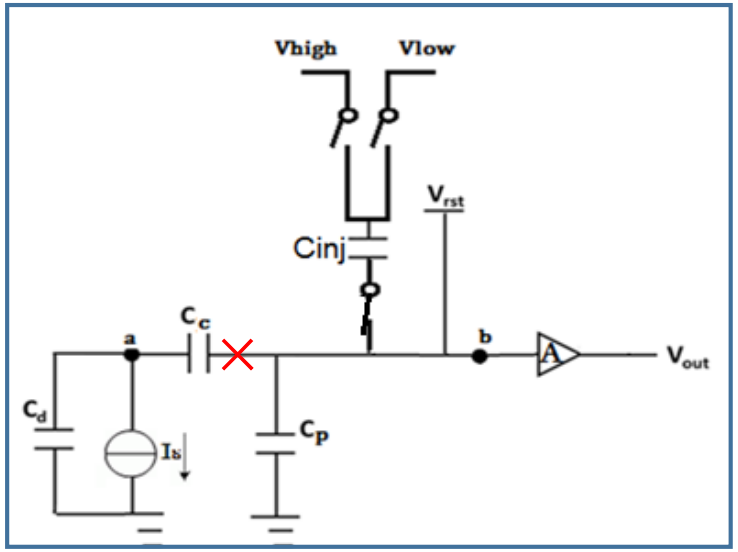
Simple amplifier (Source Follower) to readout



Method to test capacitance







① ^{55}Fe 5.9keV photon source is used for the calibration of Cinput.

② By injecting a controlled step-charge, electronic calibration was done->Cinj

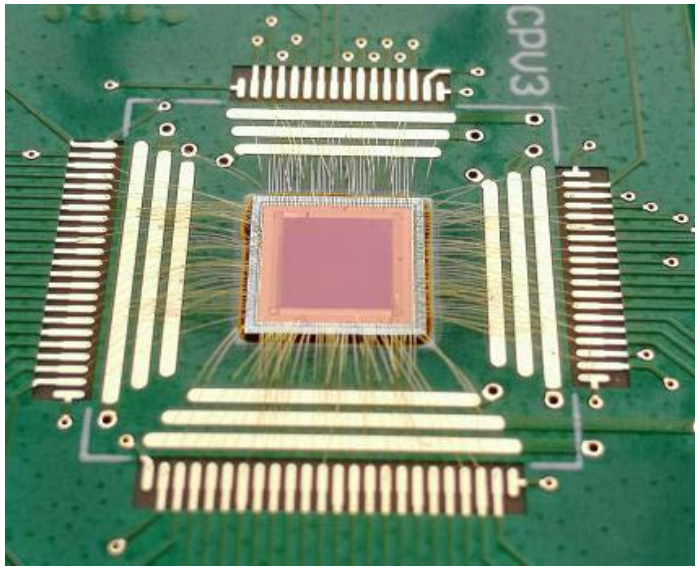
③ The parasitic capacitance Cp was tested by Dummy matrix

$$Cinj \approx A \cdot \frac{Vout}{(Vhigh - Vlow)} \cdot Cinput$$

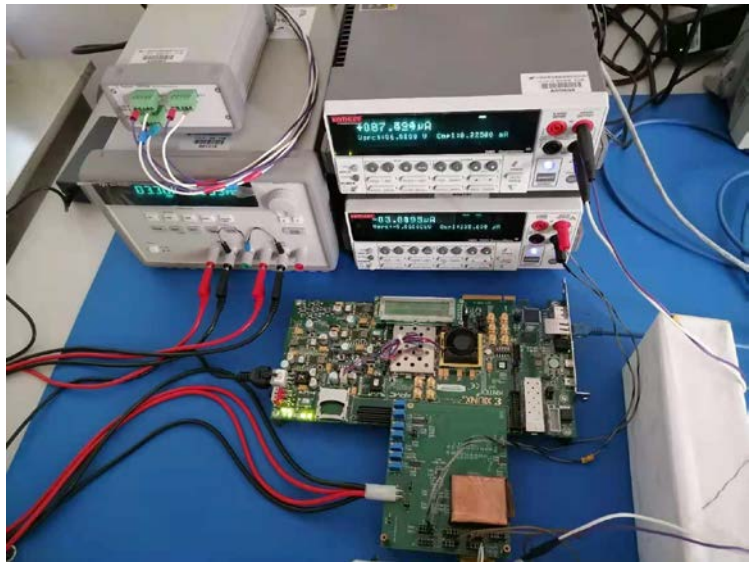
$$Cinput\ (DUT) \approx A' \frac{(Vhigh - Vlow)}{Vout} \cdot Cinj$$

Measurement setup

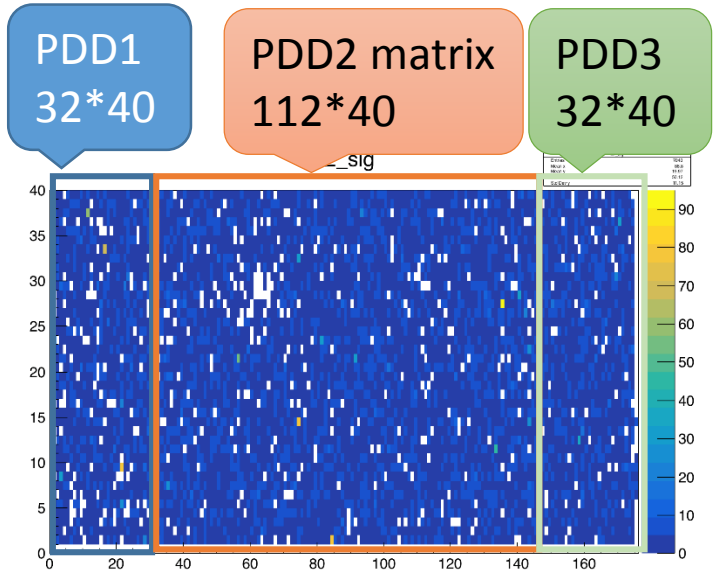
- The chip is wire-bonded on dedicated chip carrier PCB (custom designed)
- Mounted to the commercial FPGA KC705 board.
- The timing and reference voltages are controlled by the FPGA programming and the DAQ software on PC.
- The readout by a 12 bits ADC.



chip carrier PCB

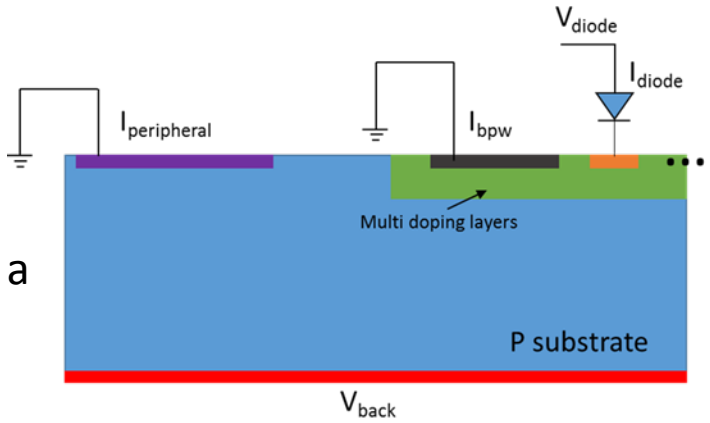


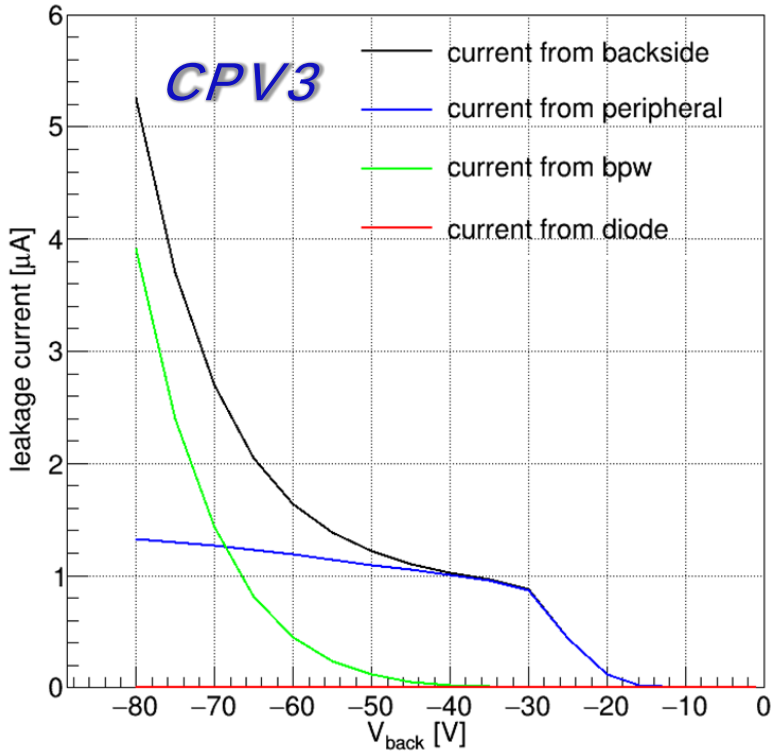
Setup

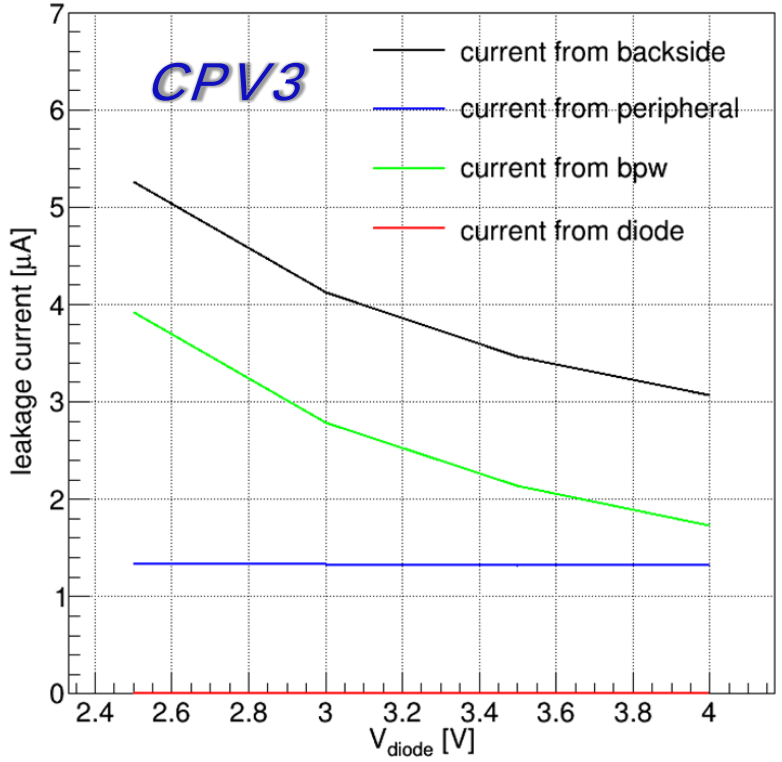


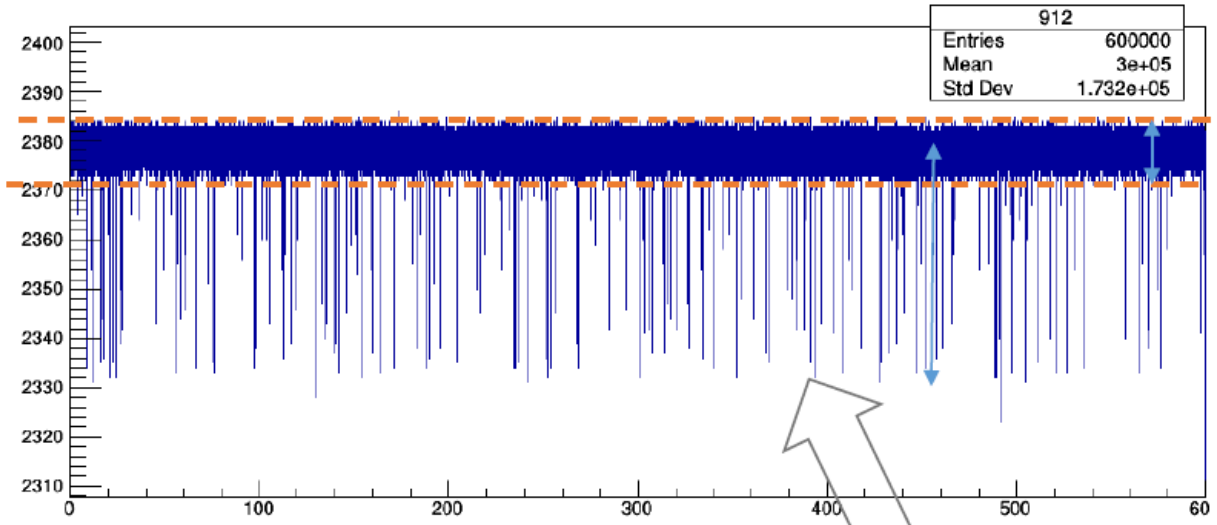
Characterization results-IV

- Measurements of each source have been performed.
- The total leakage currents increase as the bias voltages increase.
- The number from the PDD diode is quite low(<1nA) which has shown a quite good performance as expected.





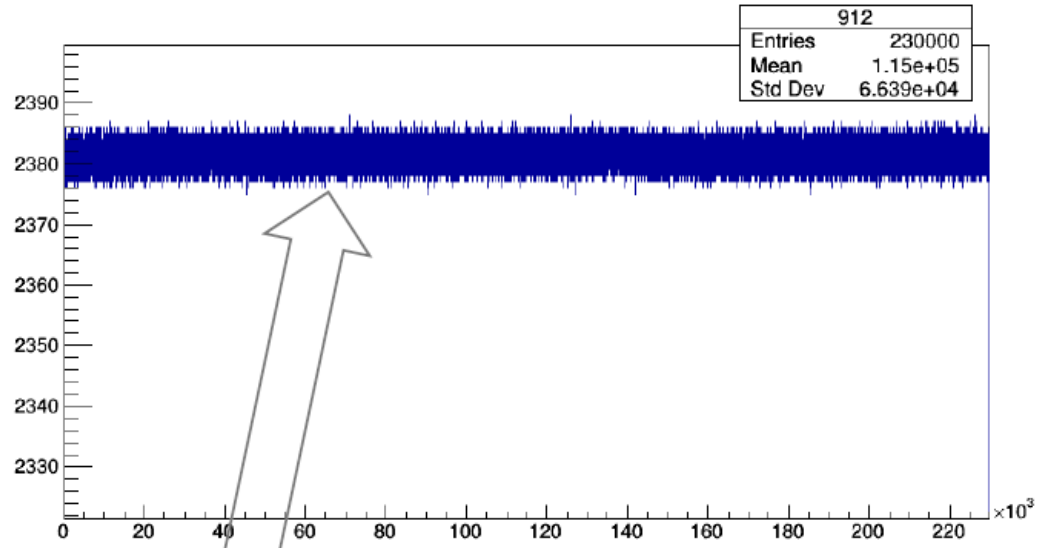




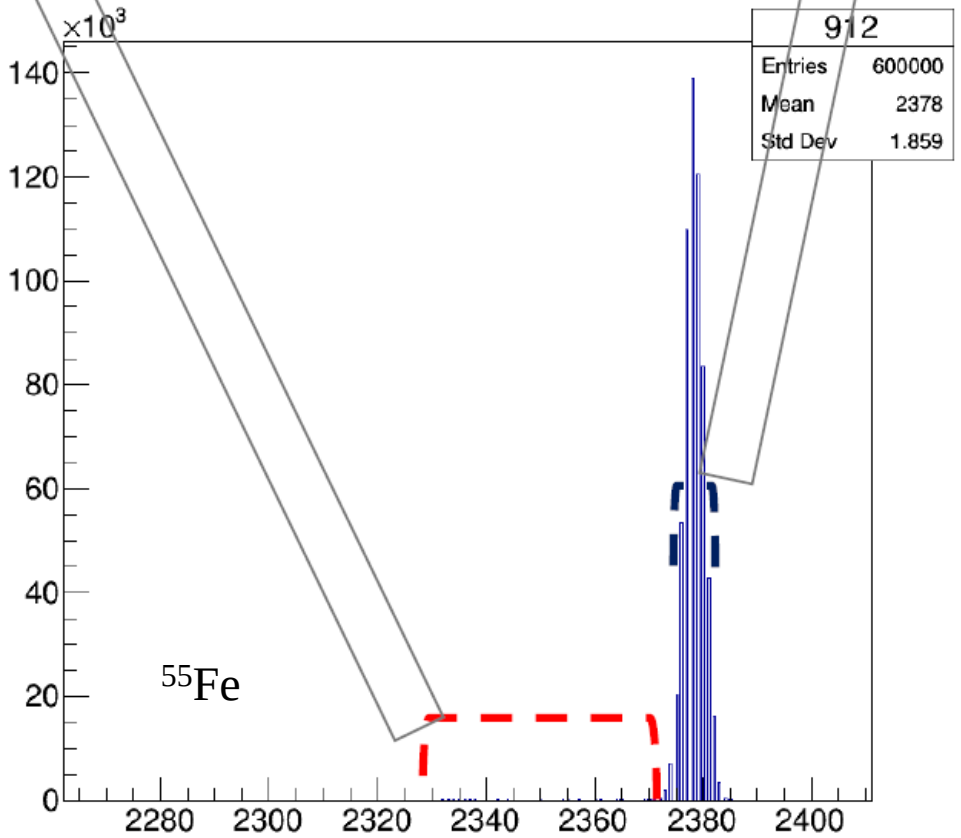
~10

(28,16)

(Nr,Nc)



SIGNAL

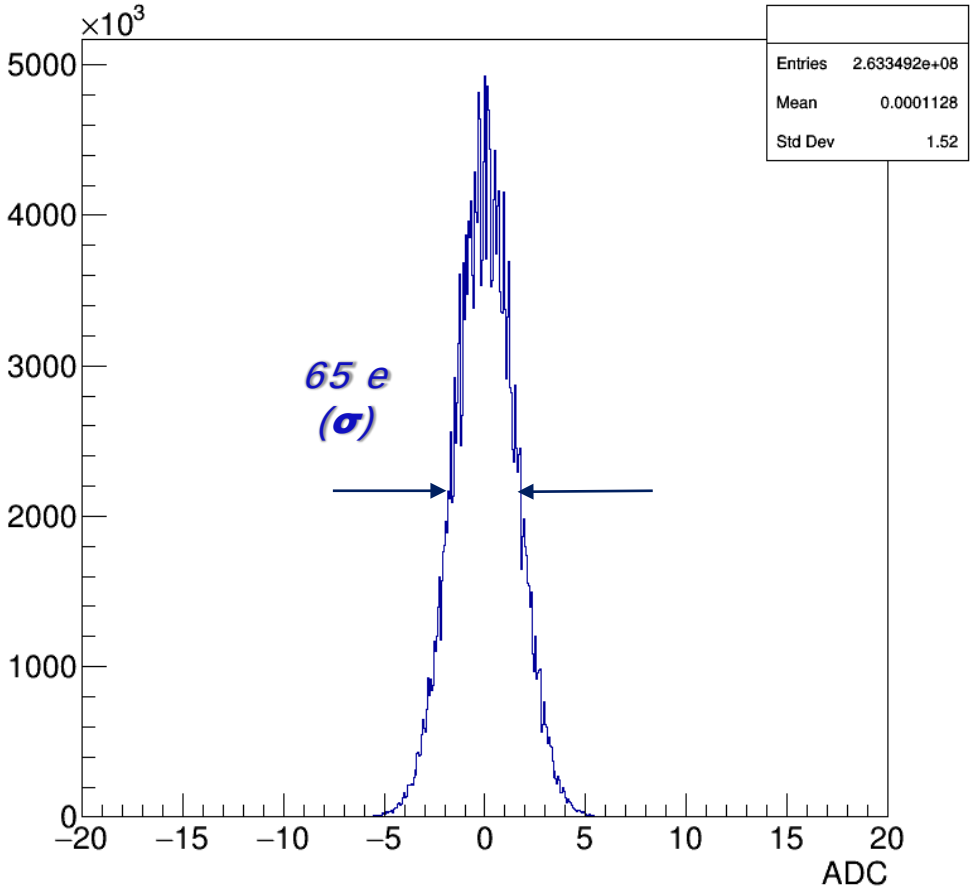


NOISE

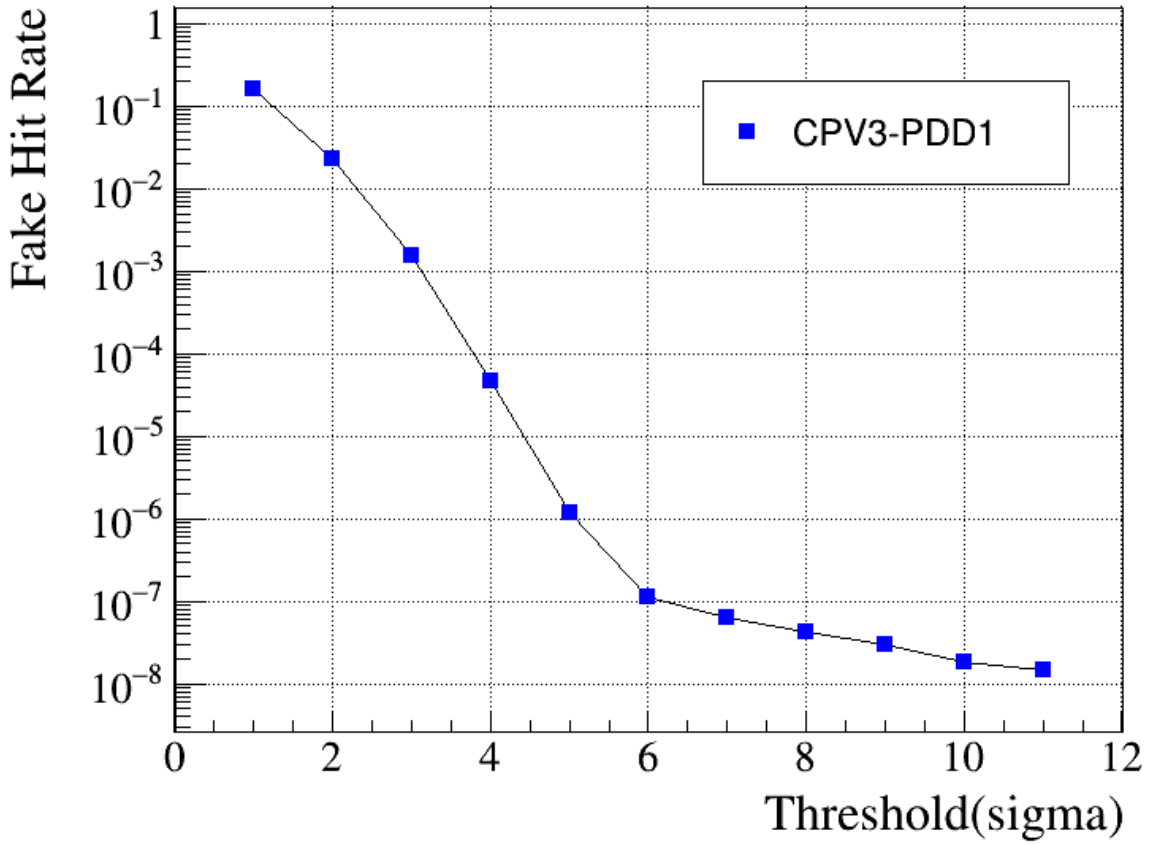
- ^{55}Fe signal observed
  - Signal =Output voltage - pedestal
  - sampled by ADC

The data of a single pixel in 600k frames

CPV3-noise

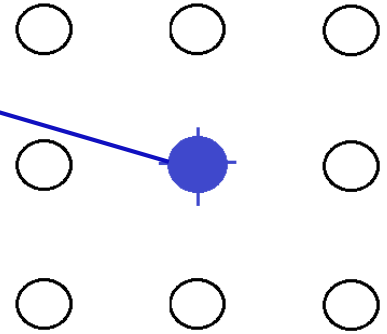


FHR as a function of Threshold



Calibration-Energy spectra of ^{55}Fe (I)

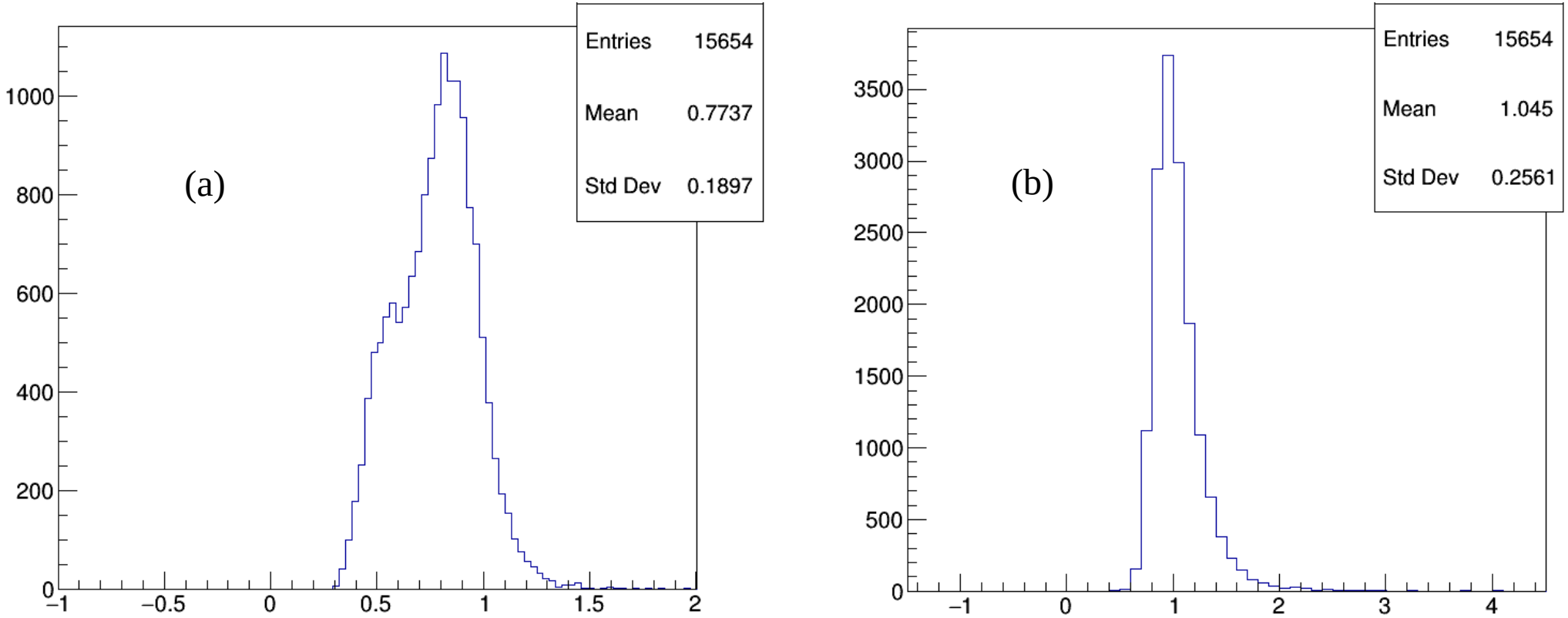
Matrix 3×3 signals



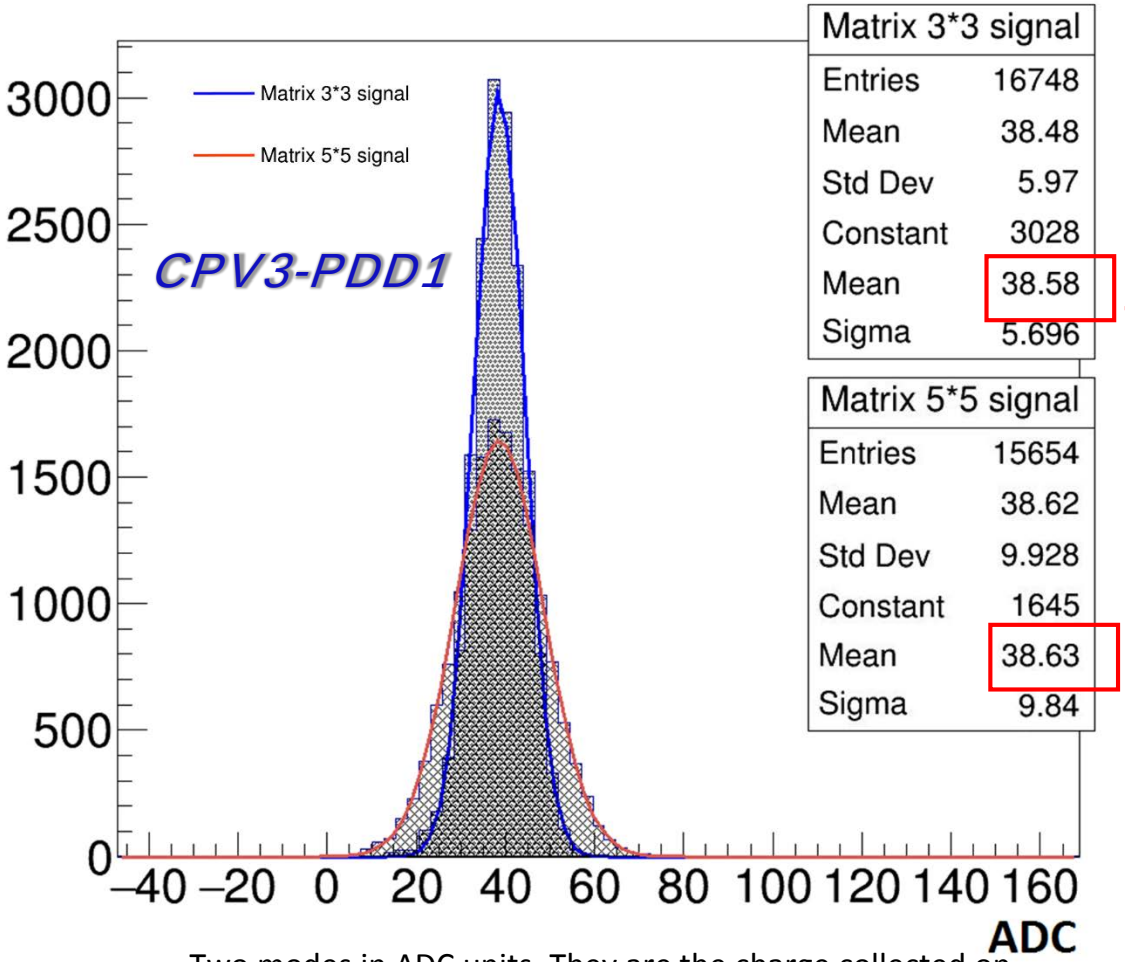
- Matrix signals: The sum of the signals of an n × n pixel matrix, centered around the seed pixel.
- Seed signal: The largest signal[6].
- Cluster signal: It is strongly dependent on the choice of the thresholds used for the assignment.

The histogram of the event-by-event values

(a) the seed pixel divided by Matrix 3 × 3 pixels signal. (b) Matrix 3 × 3 / Matrix 5 × 5 pixels signal



Calibration-Energy spectra of ^{55}Fe (II)



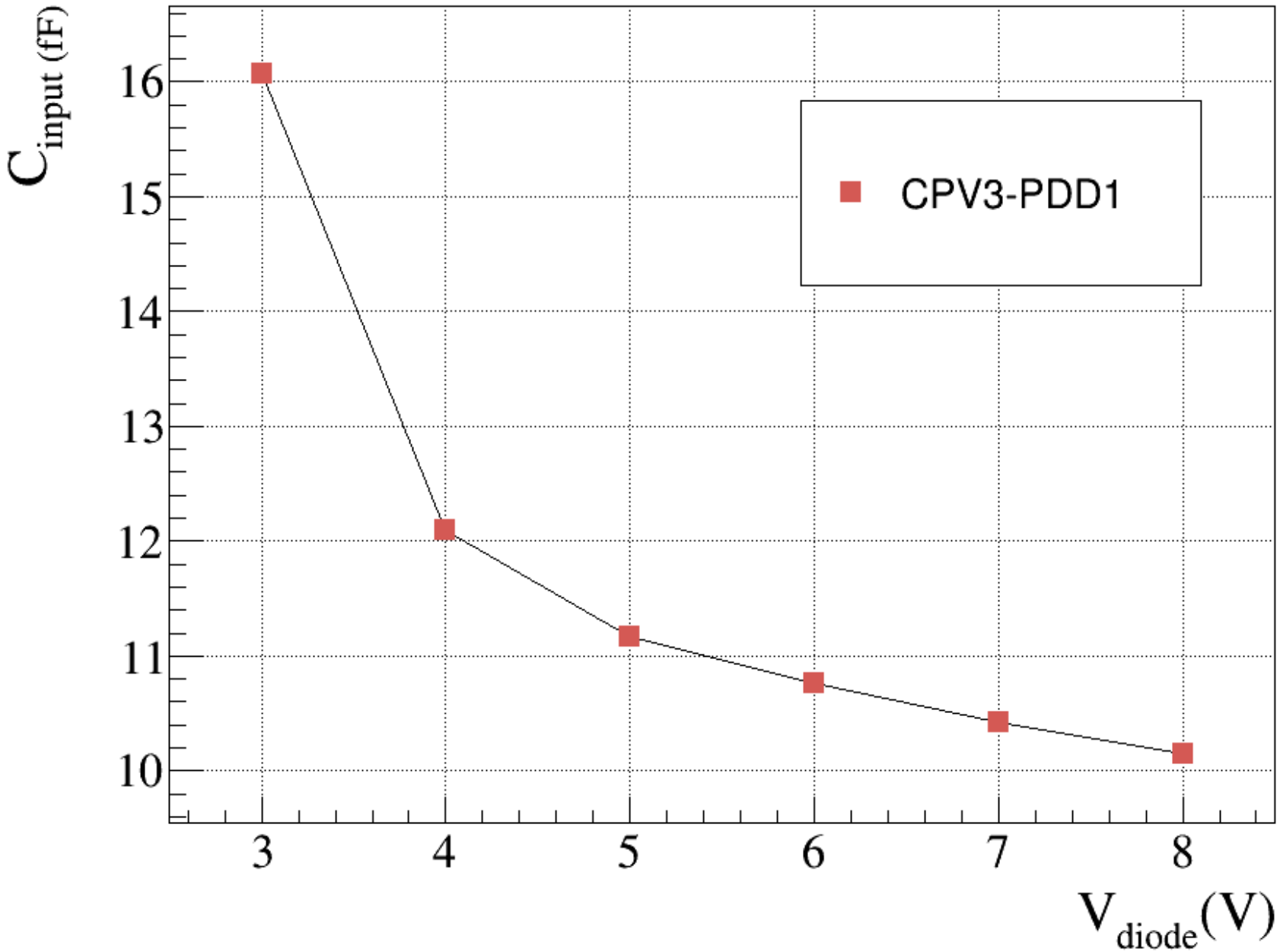
Two modes in ADC units. They are the charge collected on a **matrix** 3 × 3 pixels and 5 × 5 pixels **signal**

- The peak of two modes are quite uniform
  - **38.58 /38.63** ADC respectively.
  - Matrix 3 × 3 pixels signal is enough.
  - ~ 5.9 KeV. the charge voltage factor (CVF) and input capacitance can be calculated as:

$$CVF = \frac{V}{Nelectron} = \frac{38.6\times2/(4095\times0.87)}{5900/3.6} = 13\ \mu\ V/e-,$$

$$C_{input}(CPV\text{-}PDD1) = \frac{Q}{V} = \frac{\left(\frac{5900}{3.6}\right)\times1.6*10^{-19}}{38.6\times2/(4095\times0.87)} = 12fF$$

Here, Cinput = Cdiode + Cparasitic, when Vdiode = +4V,Vback = -60V.

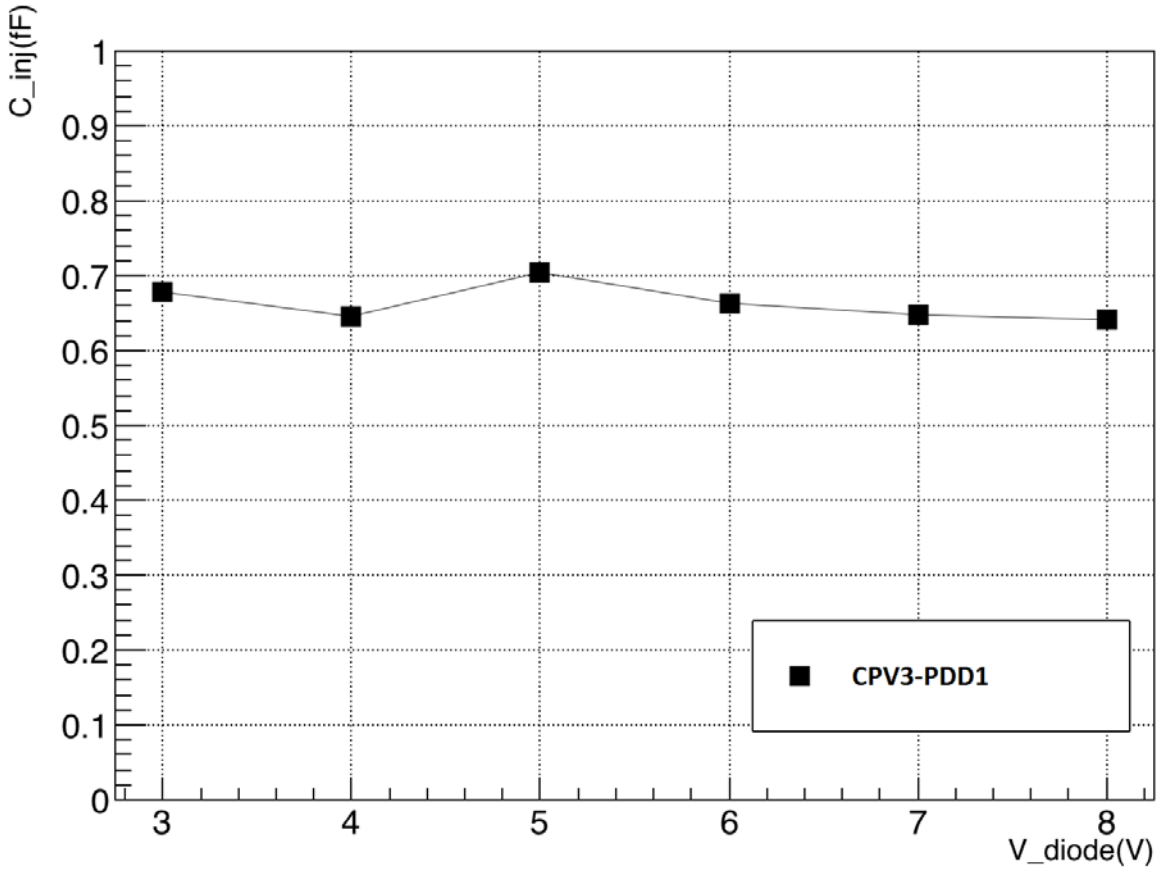

C_{input} (fF)
16
15
14
13
12
11
10
3
4
5
6
7
8
V_{diode}(V)
CPV3-PDD1

Cinj **:**

- as a function of Vdiode is performed

with each different *measured value of Cinput.*

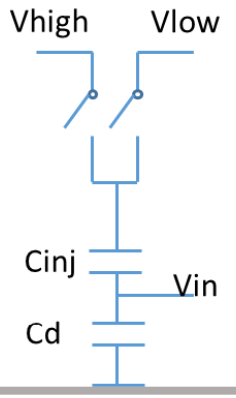
- an approximate consistency as expected (metal-metal capacitor).



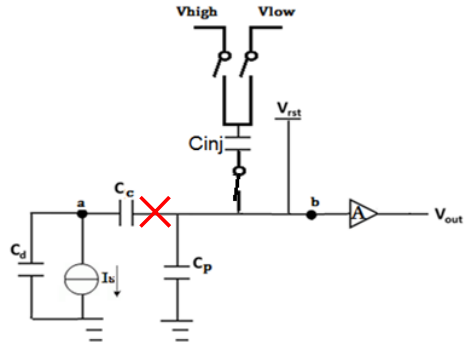
Using Cinput,pulse-test capacitance Cinj could be tested by

$$(Vhigh\text{-}Vlow\text{-}Vin)*Cinj = Vin* C_{input}$$

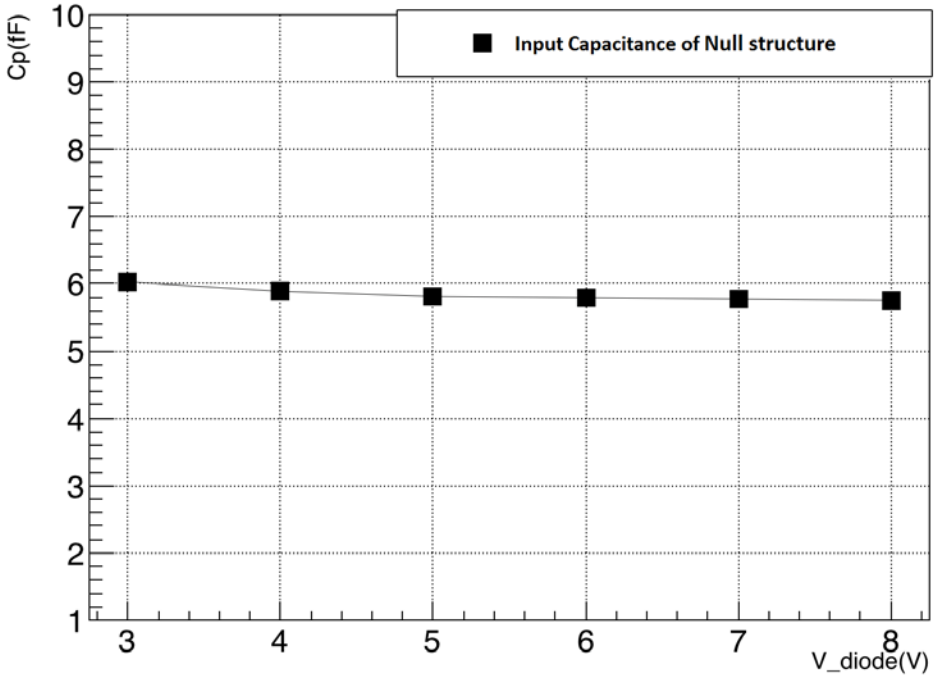
$$C_{inj} = \frac{C_{input}}{\left(\frac{Vhigh-Vlow}{Vin}\right)-1}$$

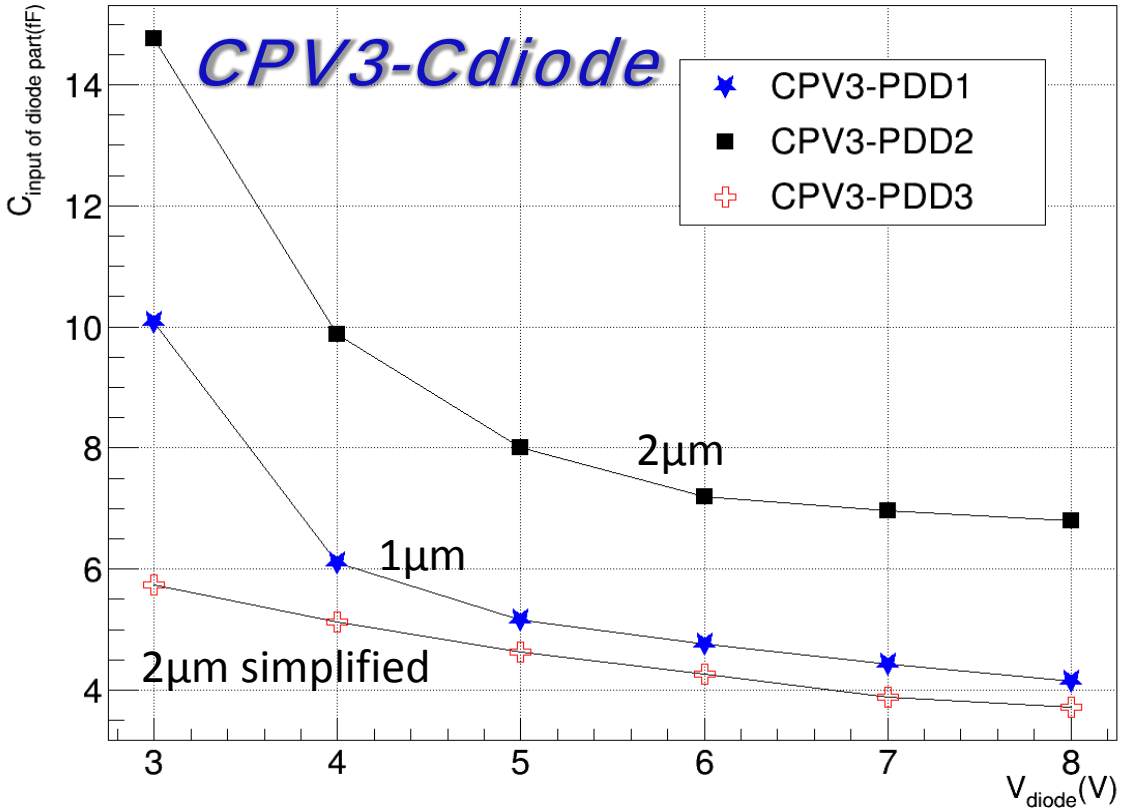


Cp :



- CP as a function of bias was tested by the dummy
  - Source of excessive cap
  - Partly confirmed by the post-layout extraction





- The diode capacitance of 3 CPV3-PDDs without Cp.
  - Minimum 3.7 fF.
  - PDD1 has smaller cap than the PDD2, which need to be understood further.

4.Summary

I. Three PDD sensor structures in the version CPV3 chip featuring 16 × 20 μm^2 pitch have been studied.

a) Cd can be decreased by applying reverse bias between the collection node and shielding layer (BPW).

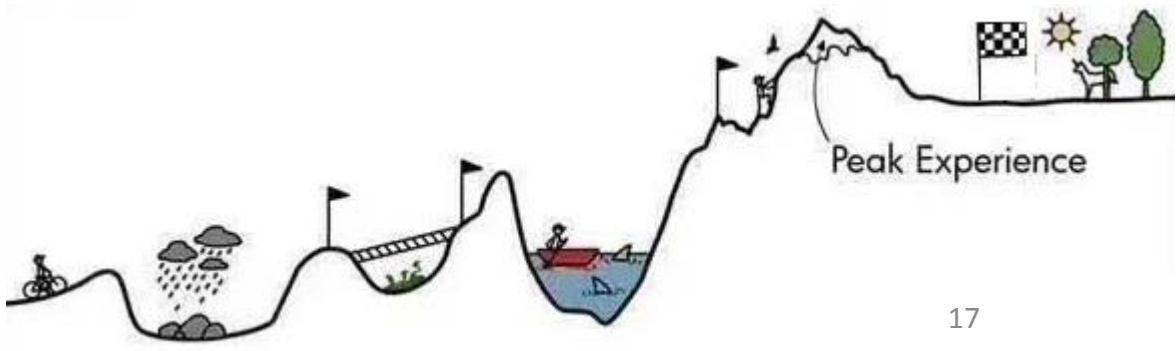
b) Excessive parasitic capacitance need to be reduced with reconsidered design.

c) The comparison of PDD1 and PDD2 is NOT expected, need to investigate further.

II. The choice of PDD design in the CPV4(3D) *[Dr. Yang Zhou's talk]* **chip has been done based on results.**

a) Chip has been delivered.

b) Bench work will start soonly.



References

[1] Y.ARAI et al., Developments of SOI monolithic pixel detectors, Nucl. Instr. and Meth. A 623 (2010), p. 186.

[2] Y.LU et al., A prototype SOI pixel sensor for CEPC vertex, Nucl. Instr. and Meth. A 924 (2019), p. 409.

[3] S.Kawahito et al., A low-Noise X-ray Astronomical Silicon-On-Insulator Pixel Detector Using a Pinned Depleted Diode Structure, Sensors, 18(1) (2018), p. 27.

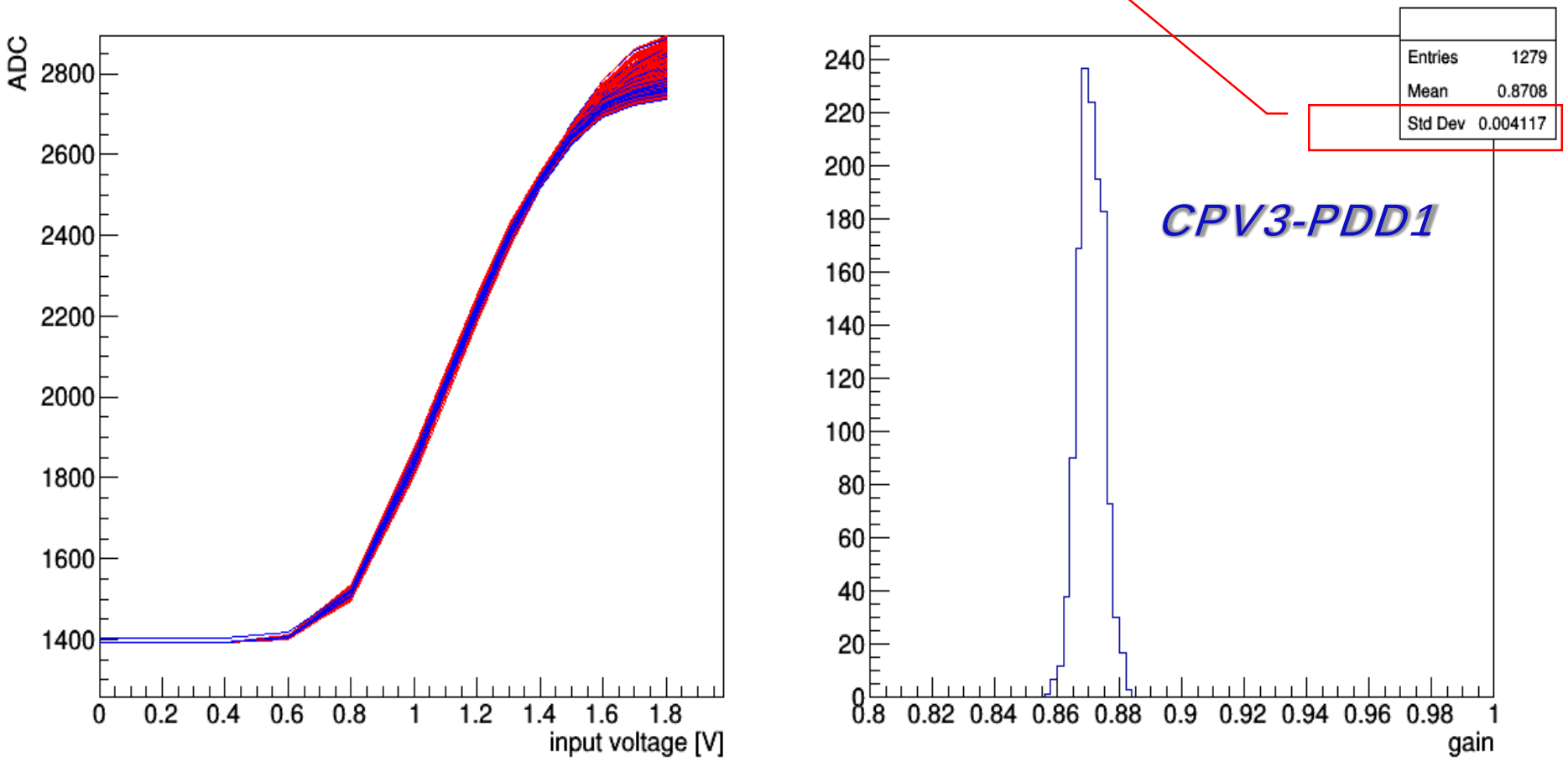
[4] S.Kawahito et al., A Silicon-on-Insulator-Based Dual-Gain Charge-Sensitive Pixel Detector for Low-Noise X-ray Imaging for Future Astronomical Satellite Missions, Sensors, 18(6) (2018), p. 1789.

[5] Y.ARAI et al., Silicon-on-insulator monolithic pixel technology for radiation image sensors. Japanese Journal of Applied Physics, 57(10) (2018), p. 1002.

[6] He M, PhD thesis,2008.

Characterization *results-Gain of circuit*

- The circuit gain's measurements of three PDD structures have been performed.
- CPV3-PDD1 Matrix 32×40 pixels: Average gain 0.87 with good consistency.



The analog readout as a function of the voltage Vrst for the whole pixel array of CPV3-PDD1.(left)The slope of the curve is the gain. (right) The distribution of the gain.