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Characterization of SOI pixel sensor using pinned depleted diode structure for CEPC vertex

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The experiment on the next generation of electron-positron collider as a Higgs factory should have to reach the unprecedented impact parameter resolution, for the purpose of efficient tagging of heavy flavor quarks and τ lepton. This sets stringent demands on silicon pixel sensors of the vertex system, which is around 3μm single point resolution for the inner most detector layer, with fast readout, and very low power-consumption density and material budget. The silicon-on-insulator (SOI) technology, featuring as a monolithic silicon pixel process with fully depleted substrate, has potential to meet those requirements. Since 2017, a new generation sensor process called pinned depleted diode (PDD) has been developed, which has shown its features such as high charge collection efficiency, suppressing the leakage current at the Si-SiO2 interface, minimizing the junction capacitance and so on. In order to take advantages of PDD in our compact pixel detector series chips for vertex (CPV) and study their performances such as diode capacitances, equivalent input capacitance, and charge sharing and so on, three different PDD sensor structures with the same test circuit, which has been fabricated in the LAPIS 200nm SOI process, were developed to learn the characterization of the different sensor structures. The description of the prototype chip including PDD sensor diode, CPV3-PDD structures，pixel schematic and test setup will be presented, followed by the characterization results of the sensors. Finally the conclusions will be drawn and future plans will be outlined.

Summary

Three PDD sensor structures in the version CPV3 chip featuring 16 x 20 ☒m2 pitch and 310 ☒m thickness have been studied. A complete overview of the characterization performed on three PDD sensors including capacitance- , current-voltage characteristics and cluster multiplicity was reported by measuring the energy spectrum of 55☒e 5.9keV x-ray as well as pulse injected charge. The measured result shows that the designed PDD structure has very low leakage current, the equivalent input capacitance decreases as the forward bias voltage increases and around 3.5fF of equivalent in-pixel capacitance. From the comparison, we get the conclusion that one of the three structure shows lower junction capacitance and better charge sharing. The evaluation was carefully taken into account and chosen in the design of the next generation CPV4 chip with SOI-3D technology.

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