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# HEPS-BPIX2: the Hybrid Pixel Detector with TSV Processing for High Energy Photon Source

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HEPS-BPIX2 is the second prototype of single-photon counting pixel detector with 1.4 million pixels developed for applications of synchrotron light sources. It follows the first prototype, HEPS-BPIX, with a pixel size of 150 μm x 150 μm and frame rate up to 1.2 kHz at 20-bit dynamic range. This paper contains a detailed description of HEPS-BPIX2 upgrade with a recently launched Through Silicon Via (TSV) processing to reduce the insensitive gap between modules. From the 60k-pixel single-module detector to large-area multi-modules systems, the transmission control protocol (TCP) hardware stack on 10 Gigabit Ethernet (10GbE) is adopted for high speed data transfer to DAQ. The calibration and images are taken at X-ray and synchrotron light, and the performance is also presented.

## Summary

High Energy Photon Source-Test Facility (HEPS-TF) is a project to study and verify the feasibility of the key technologies which will be applied to the building and running of HEPS during the 13th Five-Year Plan in China. The hybrid pixel detector is one of the most important components of synchrotron light detection, but the research in this area is almost blank in China. The anticipated technical target is an effective area larger than 8 cm x 8 cm, a spatial resolution better than 200 μm, a detectable energy range from 8 keV to 20 keV, a maximum count rate bigger than 10^6, and a frame rate higher than 100 Hz. To meet this requirements, we developed the first prototype, HEPS-BPIX, with 6 modules featuring a pixel size of 150 μm x 150 μm and frame rate up to 1.2 kHz at 20-bit dynamic range in 2016. Along with the increasing area/modules, the data-transfer requirement goes up to 10 Gbps. We start to upgrade to HEPS-BPIX2 with TSV processing, 10GbE TCP/IP hardware stack and 8GB DDR3 DIMM memory in 2017. In this paper, the complete design and verification processes of the readout electronics system including hardware design, FPGA firmware design and system testing are introduced in details.

The HEPS-BPIX2 detector (figure 1) we designed comprises:

1. Front-end module, connected in daisy chain
2. Fast control board, generating clock and trigger and forwarding data
3. DAQ server (Lenovo System x3850 with four 10Gbit/s Ethernet NICs)

On the top, the sensor consisting of p+ pixelized implants on a 300 μm n-silicon substrate is bump-bonded with 8 readout chips. The X-ray or synchrotron radiation light crossing the sensor component creates electron–hole pairs. The electrons and holes are separated by an applied reverse bias voltage, allowing the charge carriers to be collected by the appropriate pixels of the read-out chip. The readout chip can be divided into the analog part and digital part. The charge is first amplified with a low noise amplifier, shaped through a shaper and then discriminated with an adjustable threshold.

Through Silicon Vias are processed to make the connection between the front and back sides of the read-out chip. The Redistribution Layer (RDL) and Bump bonding are performed at the bottom of read-out chip to replace the wire bonding. The control, readout signals and power supplies are provided through flexible PCBs to the backing board at the backside. By using this so-called three-dimensional (3D) integration techniques, the insensitive area of the module is reduced from 26.3% to 11.8%.

Each front-end module contains one readout board. The main components in readout board are a Field Programmable Gate Array (FPGA, Xilinx Inc. XC7K325T), one optical transceiver and LEMO connector for single module mode, and Molex Nano-Pitch I/O ™ for multi module cascading. The digitized data are stored in a ring buffer of DDR3, and sent to the network processor block when the frame signal is received. A hardware based network processor (Intilop 10G TCP Offload Engine) is employed to FPGA for high speed data transfer over 10GbE. So the front-end module can connect to the data server or network switch directly.

The fast control board fans out the 40MHz clock and frame signal, monitor the buffer status of the front-end modules and forward packets between front-end module and data server.

The assembled modules have been tested with X-ray and synchrotron light source, and the results show that the readout chips work well through the TSV process without any measurable performance degradation.

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