CEPC MOST2 DAQ Plan

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CEPC MOST2 Meeting

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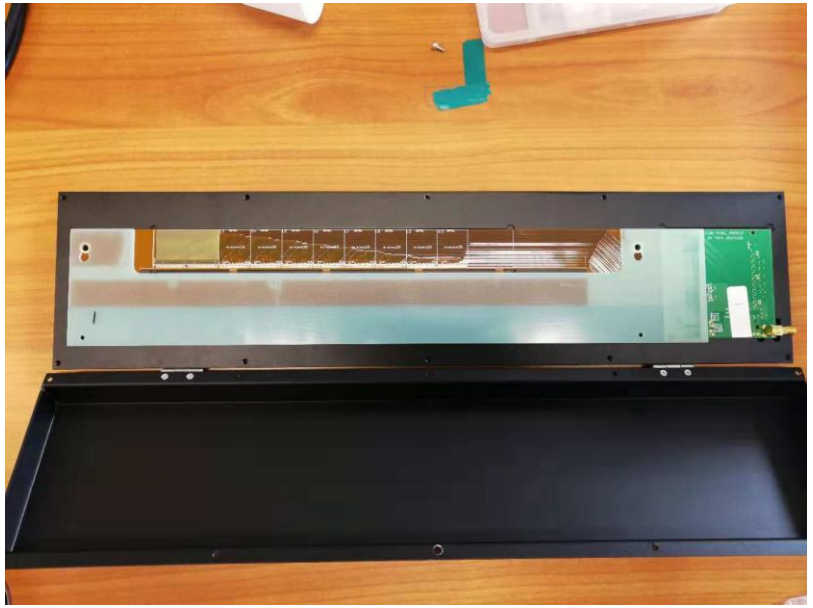
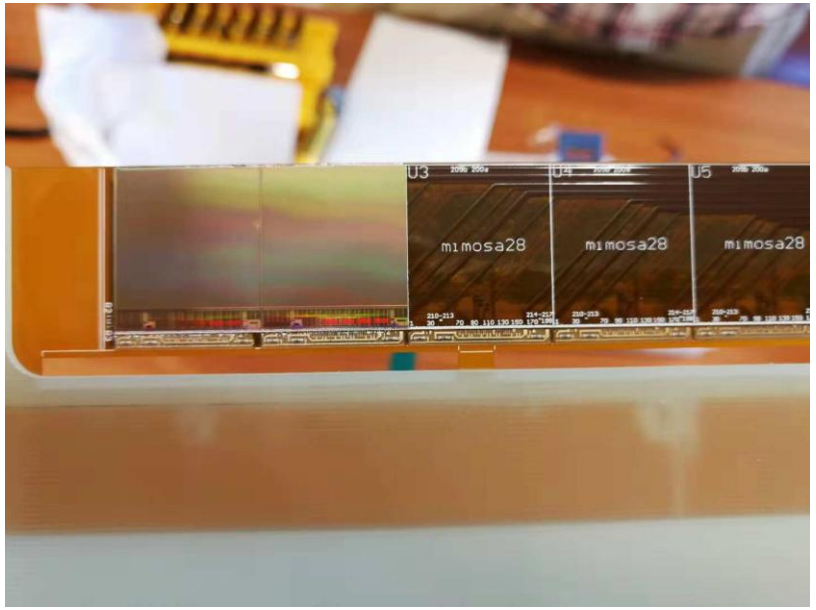
Outline

- Some experience on MAPS DAQ and Beam Test
- CEPC MOST2 requirements for DAQ
- CEPC Vertex Detector requirements for DAQ

MAPS Ladders (By DONG Mingyi)



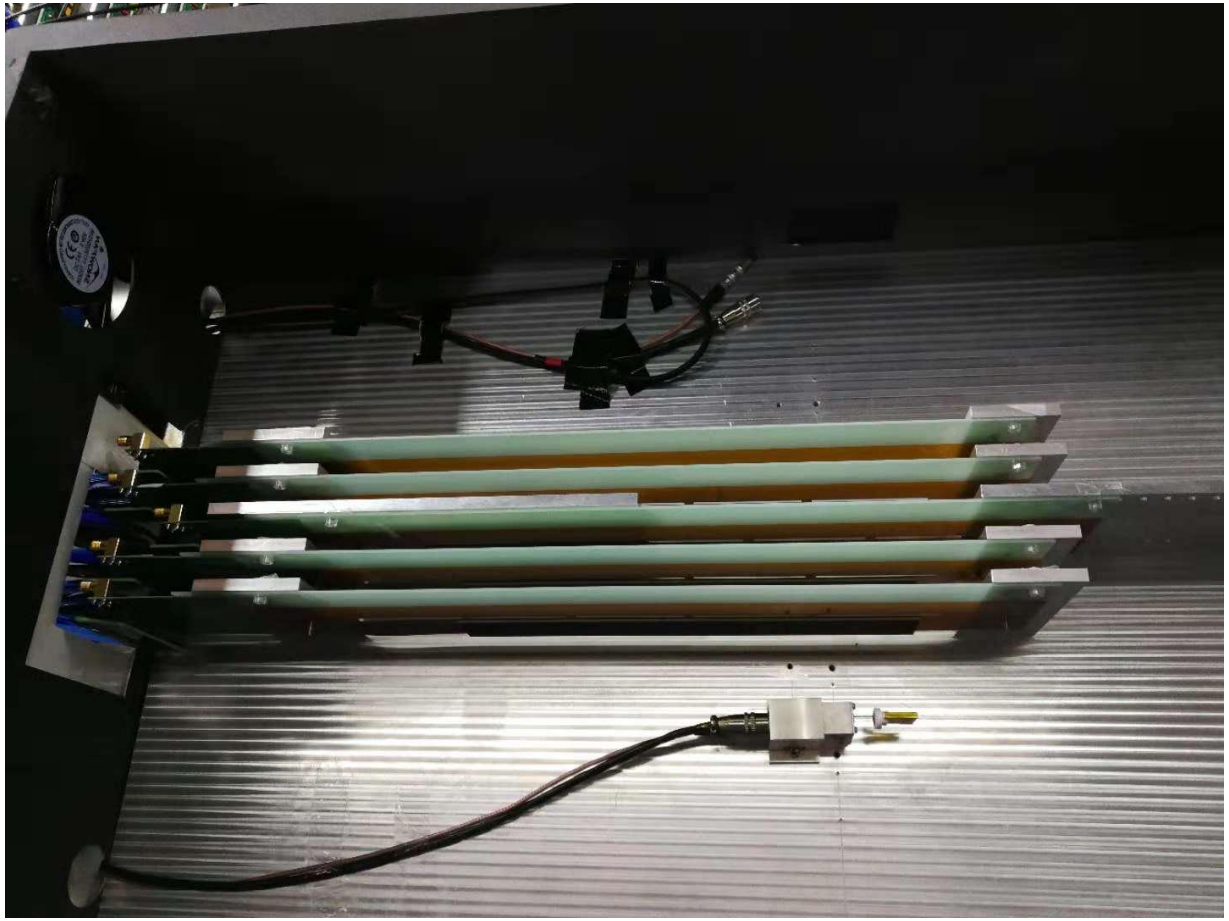
Ladder



Ladder with 2 Mimosa chips mounted

5 Ladders:
1 for test and 4 acting as for telescope

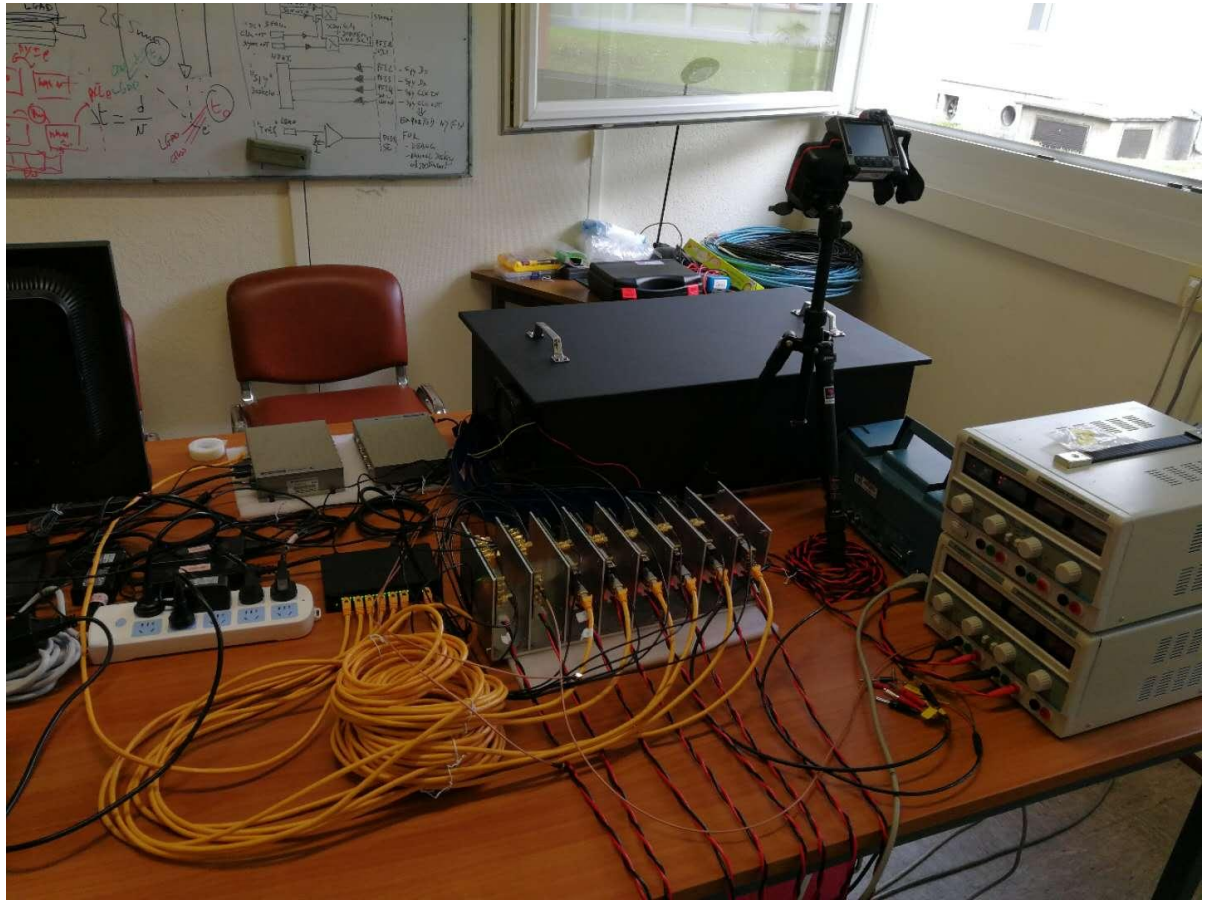
Ladders and Electronics



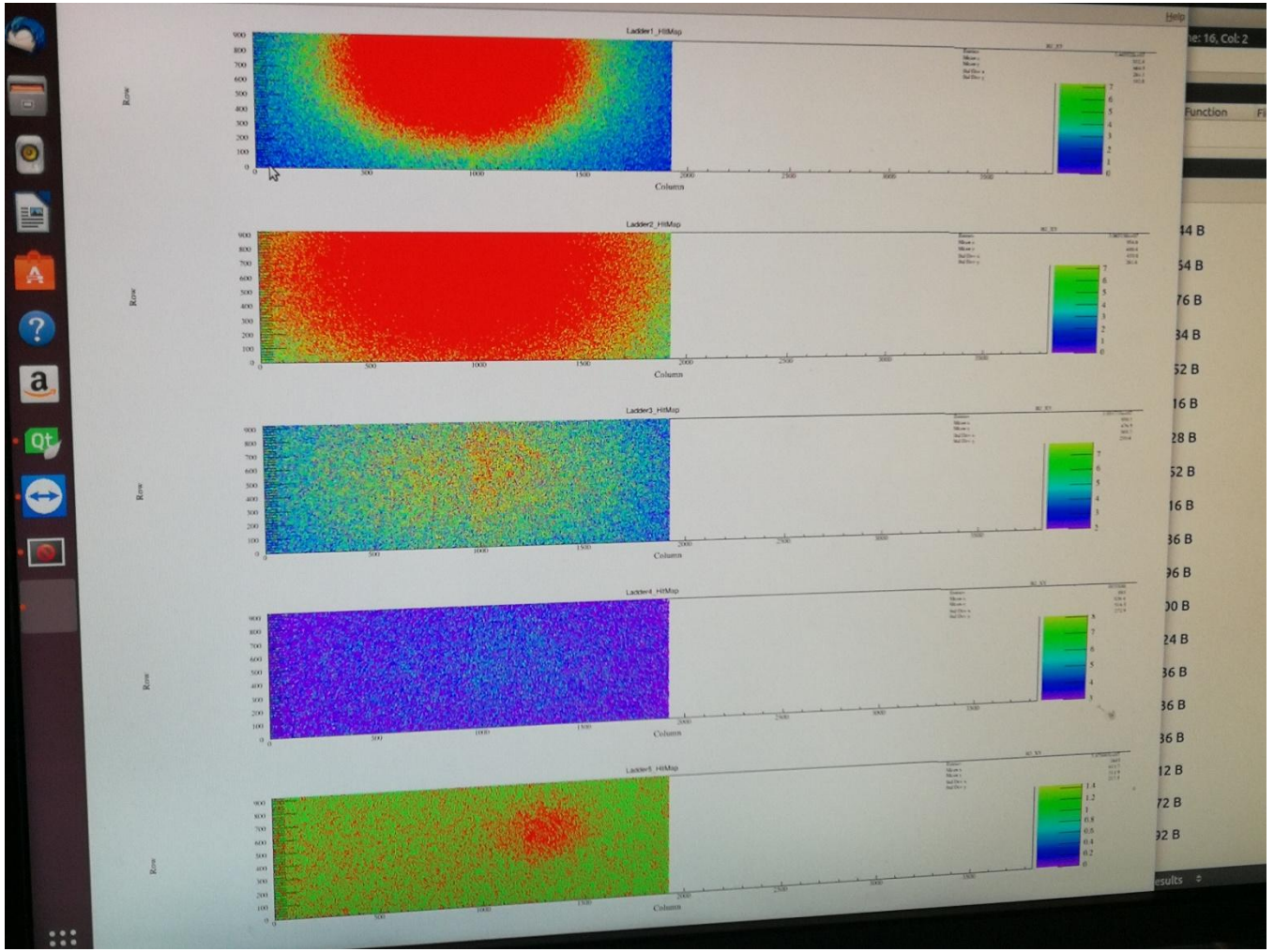
Ladders designed by DONG Mingyi

Electronics Designed by TIAN Xingcheng

MAPS Ladders & Electronics & DAQ



Result of Radioactive Source Test



MAPS Prototype Beam Test at DESY

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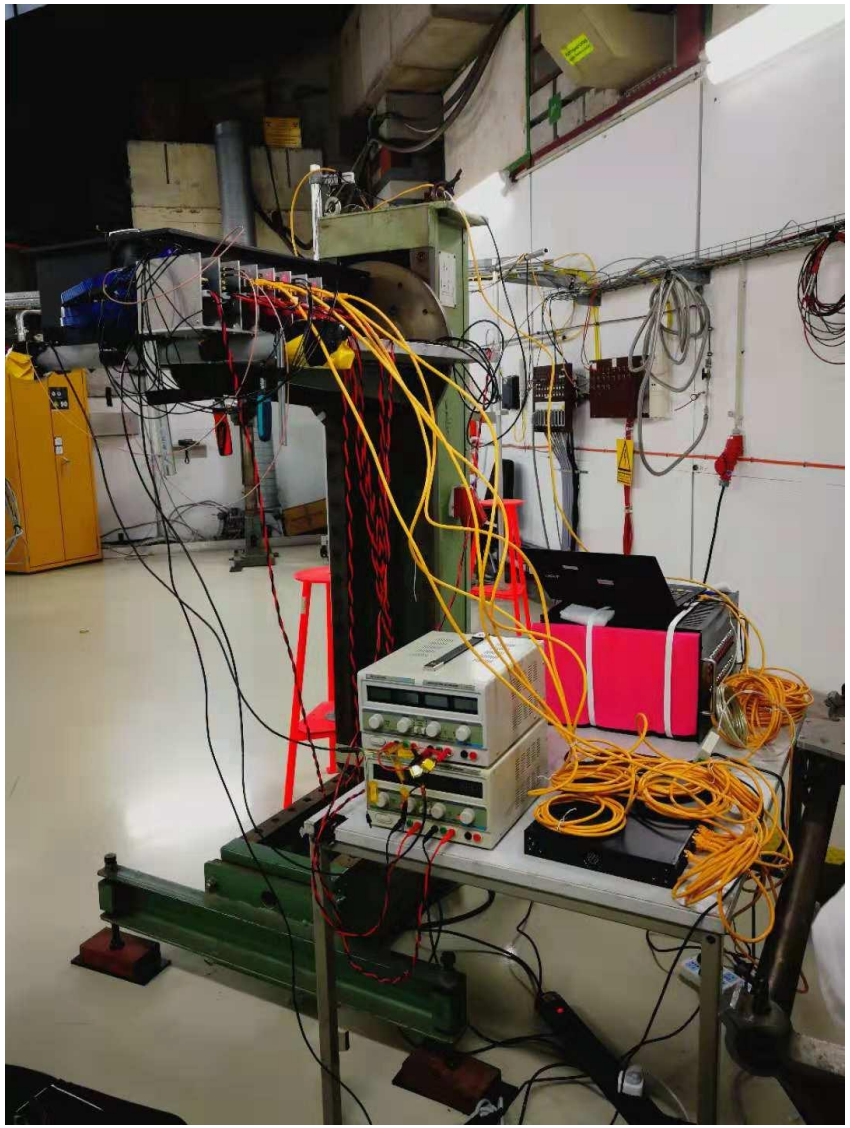
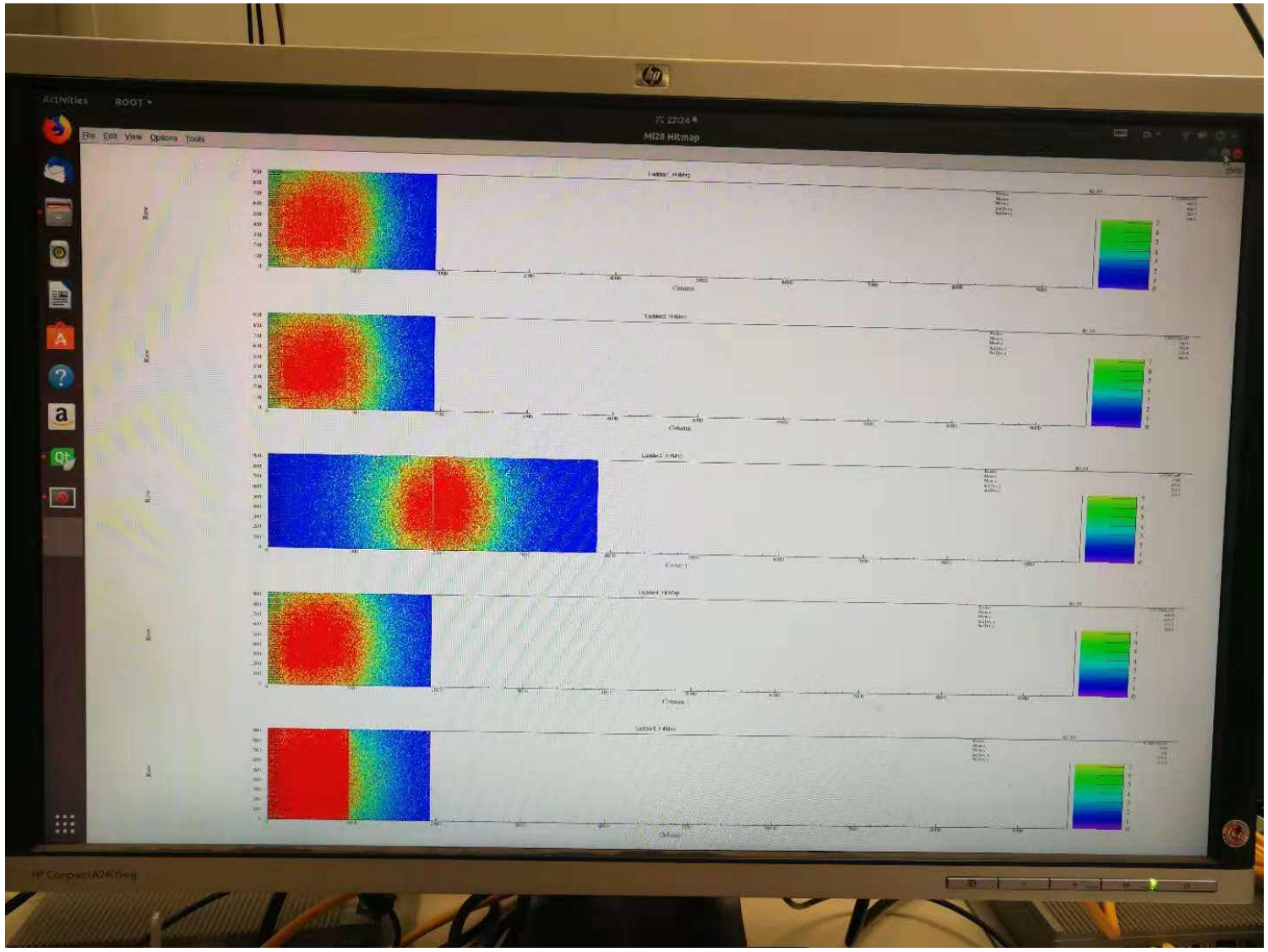
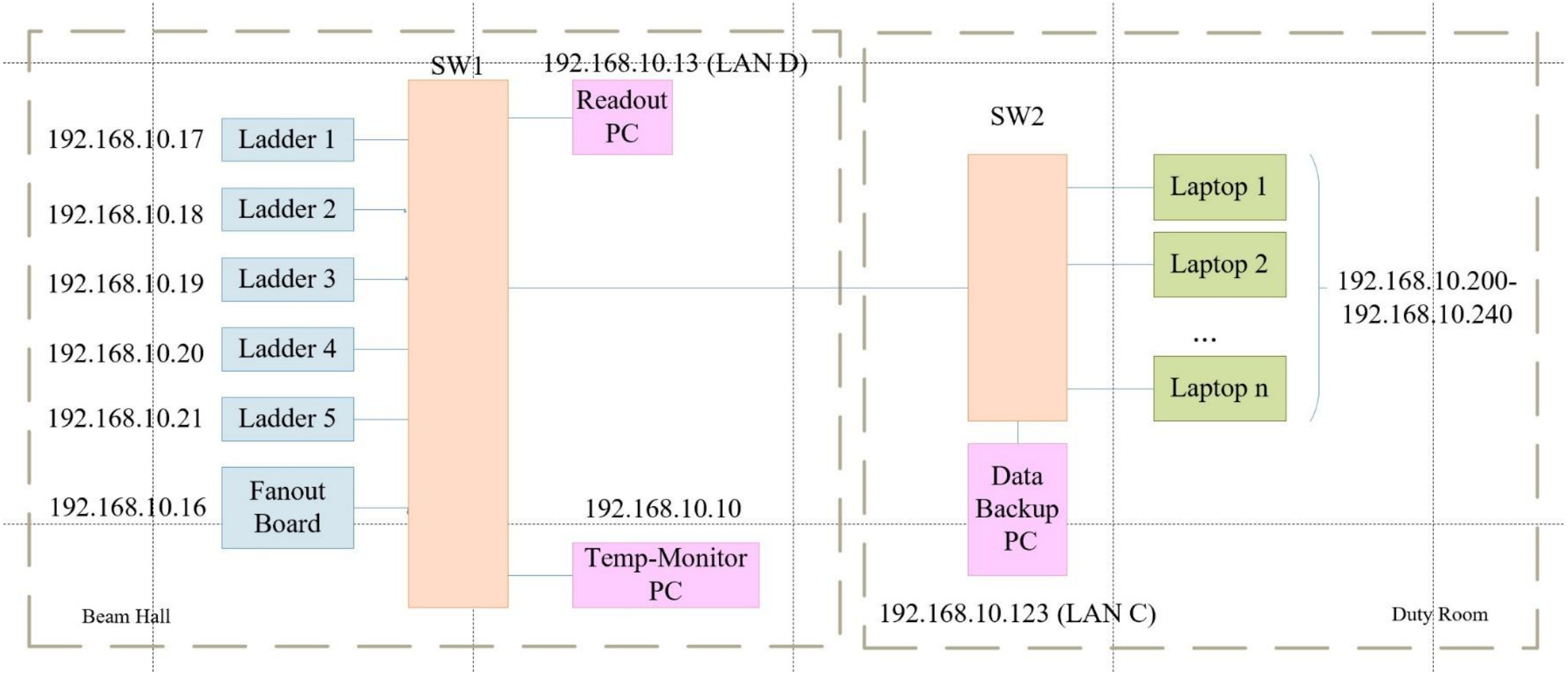




Layout of MAPS DAQ at DESY



MAPS DAQ

- Interface with FEE boards – 1Gb Ethernet port (SiTCP)
- Configure FEE boards via UDP
- Read out FEE data via TCP/IP (1GbE)

MAPS Data Readout & Data Format

- Data zero compression on chip
  - Special coding method to reduce the frame data
- Frame data could be continuously read out
- But in our case, we use trigger mode , read out 2 Frames of data per Trigger
- Build full events according to Trigger Numbers
- Thresholds of each sensor should be carefully scanned before the beam test and should be set properly to reduce occupancy & data rate of the ladders
  - Sometimes we have to disable some sensors (when too much data generated from the 10-sensor ladder)

- Readout bandwidth of each ladder is a big issue for Silicon detector

What we know about CEPC Vertex Detector

- We assume a 10 μs readout window to calculate vertex and silicon tracker occupancy. The estimated rates for Bhabha events in the LumiCal detector are within the nominal event rate, however, a dedicated high-rate LumiCal data stream is envisioned to study the beam backgrounds and deliver the required luminosity uncertainty. With the level-1 trigger operating at 100 kHz, the total raw data rate is about 2 TBytes/s.（CEPC Conceptual Design Report Volume II - Physics & Detector----8.3.1 READOUT DATA RATE ESTIMATION）

Vertex Data Rate Estimation

- Total channel numbers: 690M
- Occupancy: 0.3%
- Number of bit per channel: 32bit (4bytes)
- Channel number to be readout per event: 690M*0.3% = 2070K
- Data volume per event: 4Bytes*2070K ≈ 8.3Mbytes
- Data rate at 100KHz (10μs readout window): 8.3MBytes*100KHz = 830Gbytes/s

- Maybe more than 830Gbytes/s if considering the background of beam?

	Total # channels [M(10^6)]	Occupancy [%]	Nbit /channel	# Channels readout/evt [k(10^3)]	Volume /evt [MBytes]	Data rate @100 kHz [GBytes/s]
Vertex	690	0.3	32	2070	8.3	830
Silicon Tracker						
Barrel	3238	0.01 ~ 1.6	32	1508	3.15	315
Endcap	1238	0.01 ~ 0.8	32	232	0.4	40
TPC	2	0.1-8	30	1375	5	500
Drift Chamber	0.056	5-10	480		3	300
ECAL						
Barrel	17/7.7	0.17	32	28.8/13.1	0.117/0.053	11.7/5.3
Endcap	7.3/3.3	0.31	32	22.4/10.2	0.090/0.041	9.0/4.1
AHCAL						
Barrel	3.6	0.02	32	0.72	0.0029	0.3
Endcap	3.1	0.12	32	3.72	0.015	1.5
DHCAL						
Barrel	32	0.004	8	1.28	0.00128	0.13
Endcap	32	0.01	8	3.2	0.0032	0.32
Dual Readout						
Calorimeter	22	0.4-1.6	64	88-352	0.704-2.8	70-280
Muon						
Barrel	4.9	0.0002	24	0.01	< 0.0001	< 0.01
Endcap	4.6	0.0002	24	0.01	< 0.0001	< 0.01
LumiCal	0.5	0.2	12	0.5	0.0007	0.07

- CEPC MOST2 requirements for DAQ
  - If triggerless (4Gbits/s/sensor) is not an option, only Trigger mode (160Mbits/s/sensor) will be used:
    - Both 1 sensor and 5 sensors on a ladder, even double sided ladder (10 sensors) is OK for DAQ by using 1GbE or 10GbE TCP/IP readout
    - There is no much challenge for DAQ
    - Reuse MAPS DAQ software
  - What kind of online data processing need to do ?
    - Event building? According to Trigger Number or Time Stamp? Event sorting?
    - Event filter / soft trigger algorithm?

- CEPC Vertex Detector requirements for DAQ
  - reasonable total data rate?
  - New architecture of CEPC DAQ could be a big Challenge

Further Plan

- DAQ for Double sided MAPS Ladder
  - Ready for use or need only minor modification

- DAQ for TaichuPix Ladder
  - Need to know more details of the data format
  - How to configure the test electronics
  - Reuse part of the MAPS DAQ software