Ladder Design

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Ladder

- Ladder: basic building and functional block of the detector, key issue for the prototype and detector
 - Material budget
 - Rigidness, low deformation under gravity and force from air cooling
 - High precision of sensor position



Double-sided ladder concepts



	R (mm)	z (mm)	$ \cos \theta $	$\sigma(\mu{\rm m})$
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4

- Double sided ladder (CEPC vertex R&D)
- Double-sided has features attractive
 - low material budget (two layers share one support)
 - high rigidness
 - high resolution

- PLUME developed the first double-sided ladder
- One option of ILD vertex



Double-sided ladder design



- Material budget: 0.48% X_0 (flex cable with copper traces)
- Reduce to 0.29% X_0 if using aluminum traces

Ladder assembly procedure

- Step 1
 - Positioning, aligning and holding the sensors by using jigs
 - Aligning and gluing flex cable to sensors
 - Get single-sided ladder with sensor, flex cable
 - Repeat above procedure and get another single-sided ladder with sensor, flex cable
- Step 2
 - Wire bonding between chips and flex cable on individual flex cable
 - Get 2 individual single-sided ladders
- Step 3
 - Gluing 2 single-sided ladders on both sides of a CF fiber support
 - Operating manually with a dedicated jigs, should avoid damaging the wire bonding, especially the operation of gluing the second ladder on the CF support

Ladder assembly



















Mechanical support





- Sandwich structure : CF(150μm) + PMI Foam (1.5mm) + CF (150μm)
- Foam fill factor: about 8%
- New design with thinner CF (100 µm, high elasticity modulus)
 - Equivalent thickness: 350 μm CF

Plan

- Double-sided ladder design and jigs design
- Before May 2020, Verify the double-sided ladder design, assemble prototypes with MIMOSA chips
- Next year, Double-sided ladder system test with beam at IHEP E3 if it is available
- Jul.-Dec. 2020, Modify the jigs, and move to the ladder development of CEPC vertex prototype with dummy chips
- Develop ladders of CEPC vertex prototype with functional chips
- CEPC vertex prototype assembly
- CEPC vertex prototype test

Thanks for your attention

BES Ladder Assembly







Material budget tested with beam







- The material budget was tested
- About 0.35% X₀
- Be consistent with the calculation value (0.37 % X₀)

Gap between two chips





- D1≈D2 ≈ 340µm
- Average gap between neighboring chips is 340 µm
- Take into account the row sequencer on the chip, chip location accuracy is better than 10µm

Spatial Resolution

Resolution VS Threshold @ 5GeV Resolution VS Threshold @ 5GeV 6 U Resolution U Resolution 4.6 V Resolution 5.8 V Resolution 4.4 5.6 Resolution [um] Resolution [um] 5.2 5 3.8 4.8 3.6 4.6 2 2.5 3.5 4.5 5 5.5 2 2.5 3.5 4.5 5 5.5 3 3 4 System average resolution Threshold [Sigma]

Spatial Resolution VS Energy @ 2.5o

