Full Size Sensor Designs for the CEPC Vertex Detector

Wei Wei & Yunpeng Lu

On behalf of the CEPC Vertex detector design team

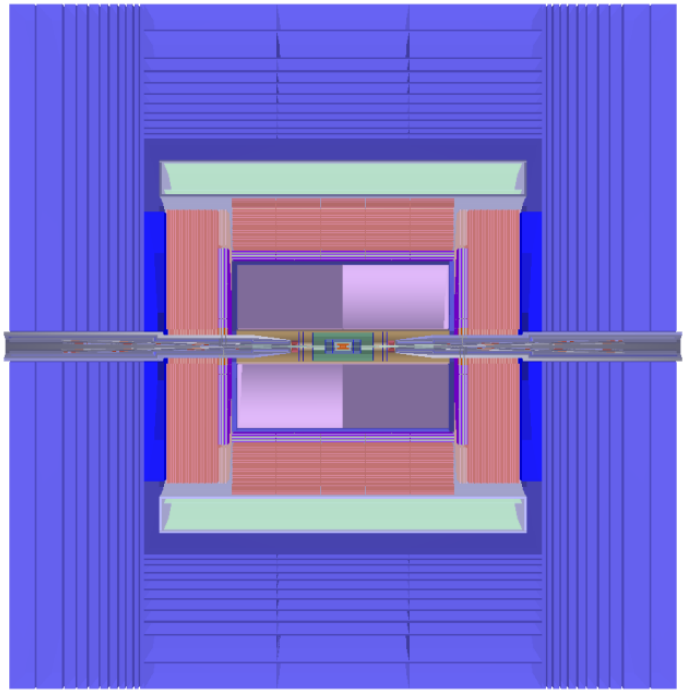
2019-12-30

Outline

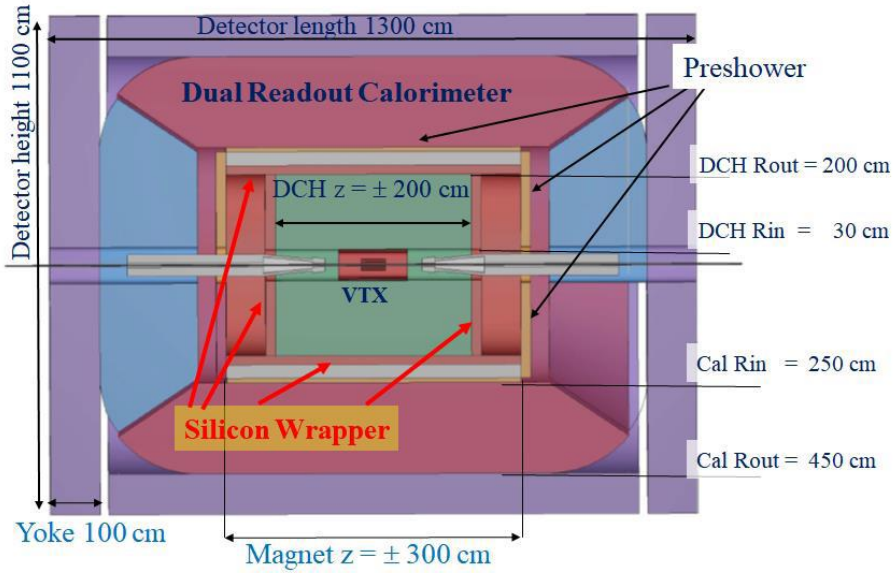
- **CEPC Vertex Detector Concept**
- **Design activities for the full size sensor**
  - **Fine pitch low power approach**
  - **Fast readout approach**
- **Recent Status of the sensor designs**
  - **Jadepix3**
  - **TaichuPix1**
  - **Test & plans**

CEPC Detector Concepts

- **Baseline detector concept**
  - either Silicon tracker + TPC or full Silicon Tracker
  - High granular calorimetry system
  - 3 Tesla solenoid
  - Muon detector



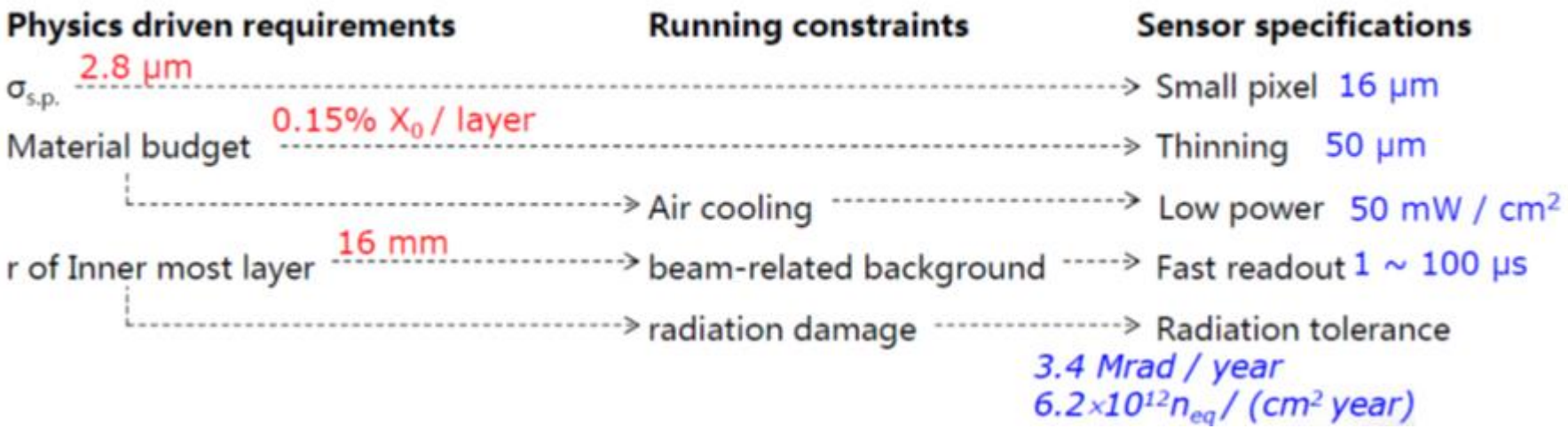
- **Alternative detector concept, IDEA**
  - Silicon pixel + Drift Chamber
  - 2 Tesla solenoid
  - Dual readout calorimeter
  - Muon chamber



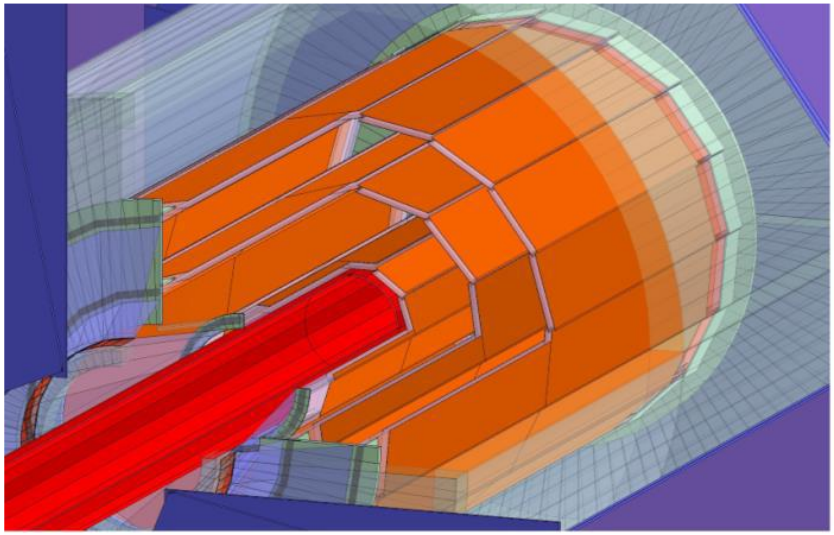
Pixel Sensor Specifications

- **Efficient tagging of heavy quarks (b/c) and τ leptons**
  - **impact parameter resolution**

$$\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\sin^{3/2}\theta} (\mu m)$$

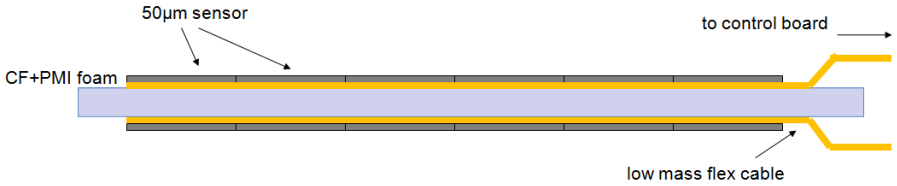


CEPC Vertex Detector Concept

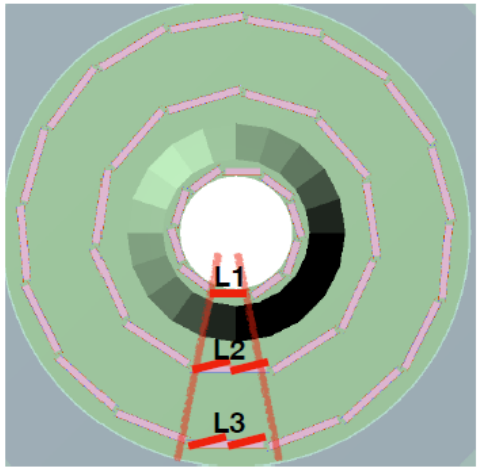


3-layers of double-sided pixel sensors

		R(mm)	|z|(mm)	σ(μm)
Ladder1	Layer1	16	62.5	2.8
	Layer2	18	62.5	6
Ladder2	Layer3	37	125	4
	Layer4	39	125	4
Ladder3	Layer5	58	125	4
	Layer6	60	125	4



A ladder module conceptual design



ATLAS/CMS upgrade
(15 μm)

Alice upgrade
(8 ~ 10 μm)

CEPC vertex
(3 ~ 5 μm)

Resolution

Ref: Pixel Vertex Detector Prototype MOST 2018-2023 (MOST2), Joao Costa, 2019.11

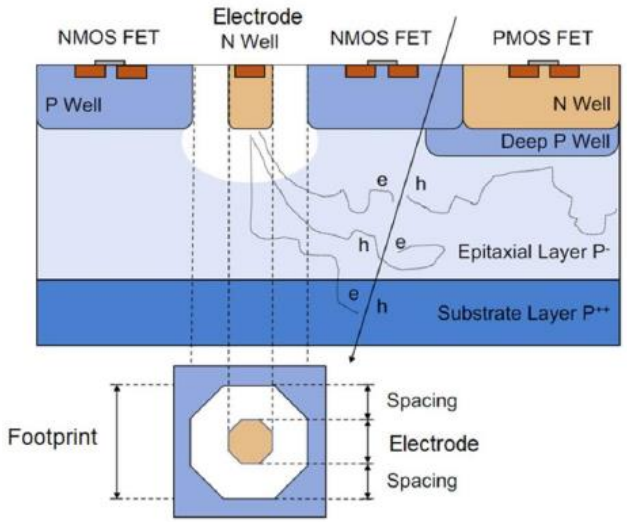
Challenges and R&D activities on pixel sensors

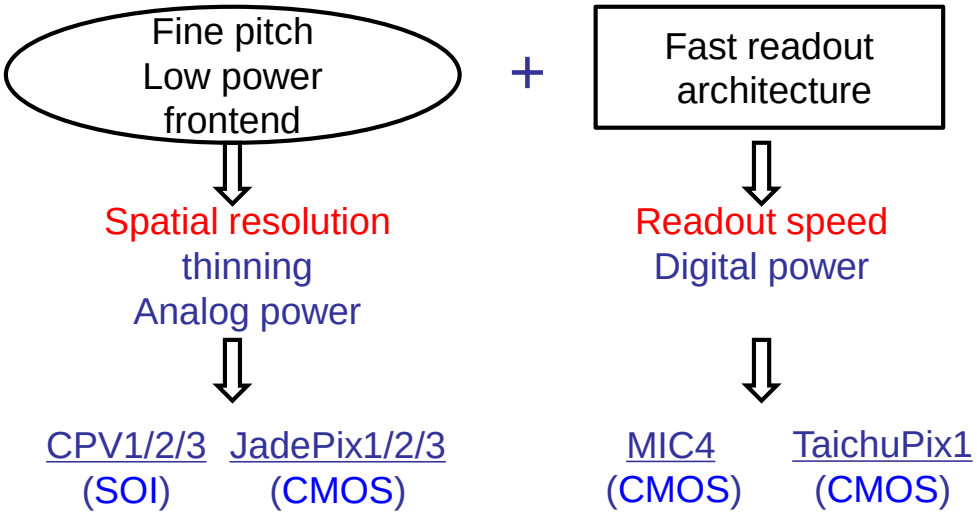
- **Bunch spacing**
  - **Higgs: 680ns; W: 210ns; Z: 25ns**
  - **Meaning 40M/s bunches (same as the ATLAS Vertex)**
- **Hit density**
  - **2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z**
- **Cluster size: 3pixels/hit**
  - **Epi- layer thickness：~18μm**
  - **Pixel size： 25μm×25μm**
- **Hit rate: 120MHz/chip @W**

- **Two major constraints for the CMOS sensor**
  - **Pixel size: < 25μm* 25μm (σ~5μm)**
    - **aiming for 16μm*16μm (σ~3μm)**
  - **Readout speed: bunch crossing @ 40MHz**
- **None of the existing CMOS sensors can fully satisfy the requirement of high-rate CEPC Vertex Detector**
- **TID is also a constraint, 1~2.5Mrad/year is achievable**

	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✔	X	✔
Readout Speed	X	✔	X
TID	X (?)	✔	✔

Challenges and R&D activities on pixel sensors



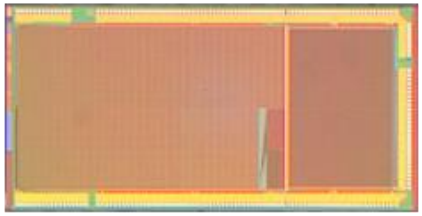


- **TowerJazz CIS 0.18 µm process**
  - **R & D on SOI in parallel**
- **Quadruple well process**
- **Thick (~20 µm) epitaxial layer**
- **with high resistivity (≥1 kΩ•cm)**
- **Very small C_{diode} ~ a few fF**

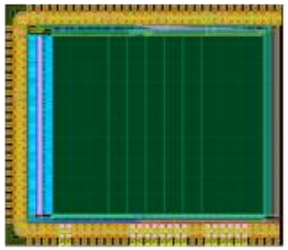
- **Step 1: optimized separately either for spatial resolution or for readout speed**
  - **CPV1/2/3 and JadePix1/2/3**
  - **MIC4 and TaichuPix1**
- **Step 2: combine the two parts**
  - **with advanced technologies**
    - **3D-SOI is being pursuing**
  - **or on different layers**

Previous CMOS pixel sensor prototypes

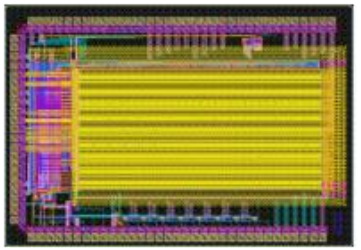
Prototype	Pixel pitch (μm^2)	Collection diode bias (V)	In-pixel circuit	Matrix size	R/O architecture	Status
JadePix1	33 × 33 16 × 16	< 1.8	SF/amplifer	96 × 160 192 × 128	Rolling shutter	In measurement
JadePix2	22 × 22	< 10 V	amp., discriminator	128 × 64	Rolling shutter	In measurement
MIC4	25 × 25	reverse bias	amp., discriminator	112 × 96	Asynchronous	In measurement



JadePix1 (IHEP)
3.9 × 7.9 mm^2



JadePix2 (IHEP)
3 × 3.3 mm^2



MIC4 (CCNU & IHEP)
3.2 × 3.7 mm^2

All prototypes in TowerJazz 180 nm process

- **Slides from Y. Zhang: "IHEP CMOS pixel sensor activities for CEPC", 2018.3**
- **Y.P. Lu, "Pixel design and prototype characterization in China", The 2018 International Workshop on the High Energy Circular Electron Positron Collider**

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- **Design activities for the full size sensor**
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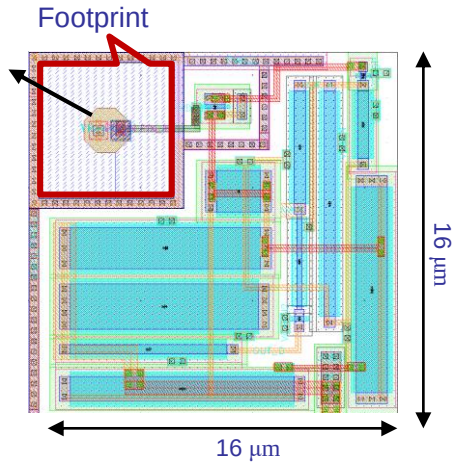
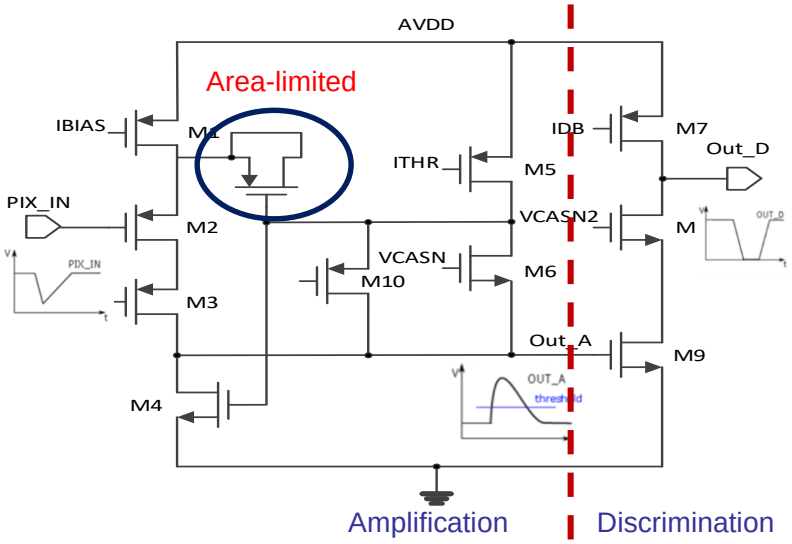
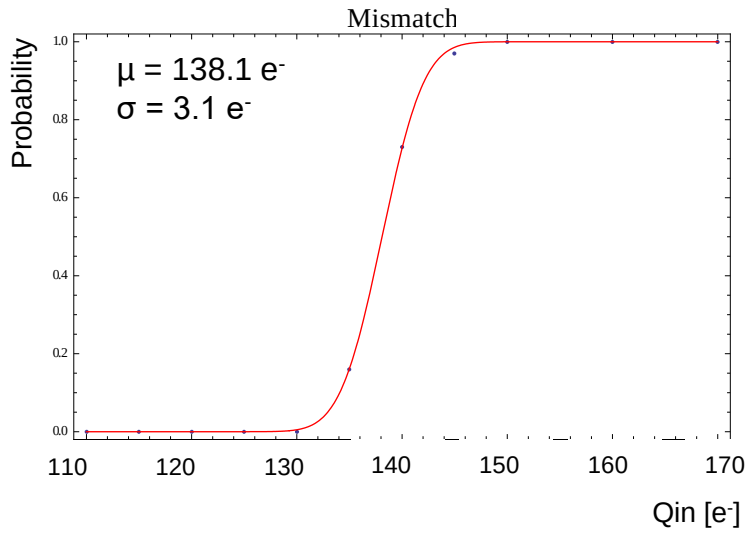
- **Recent Status of the sensor designs**
  - **Jadepix3**
  - **TaichuPix1**
  - **Test & plans**

JadePix3: Diode & Front-end design

- **Design goals: small pixel size and low power consumption**
- **Sensing diode: negatively biased for high Q/C**
  - **Electrode size 4 µm², with a small footprint 36 µm²**
- **Frontend: tradeoff between FPN and layout area**
  - **Improvement on the FPN = 3.1e⁻ (simulation)**
  - **Reduction on the layout area, ~200 µm²**
  - **A low power version (20nA), equivalent to 9 mW/cm²**

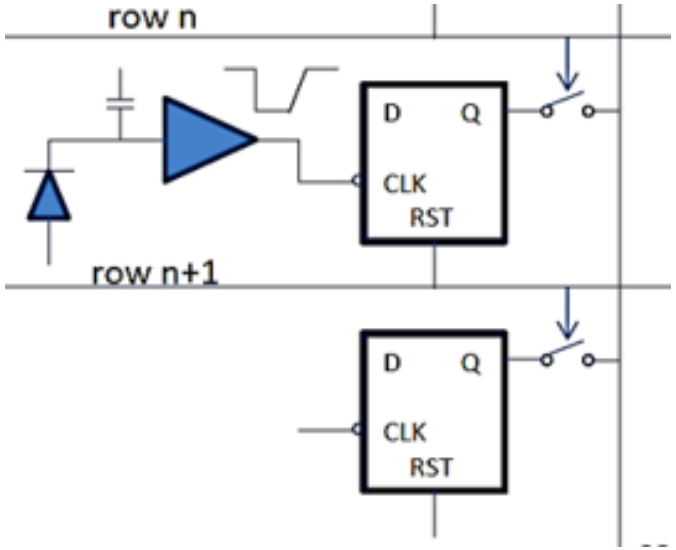


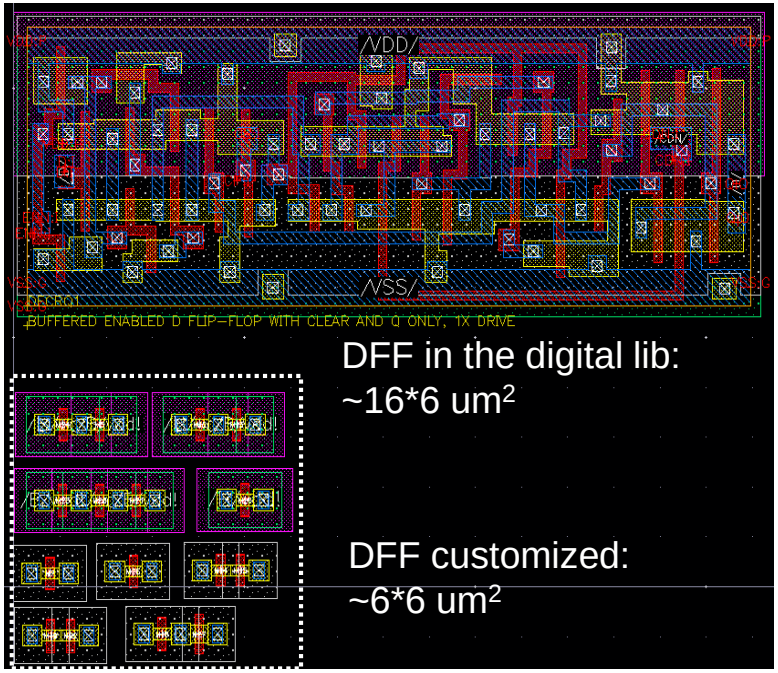




JadePix3: Customized D-FlipFlop

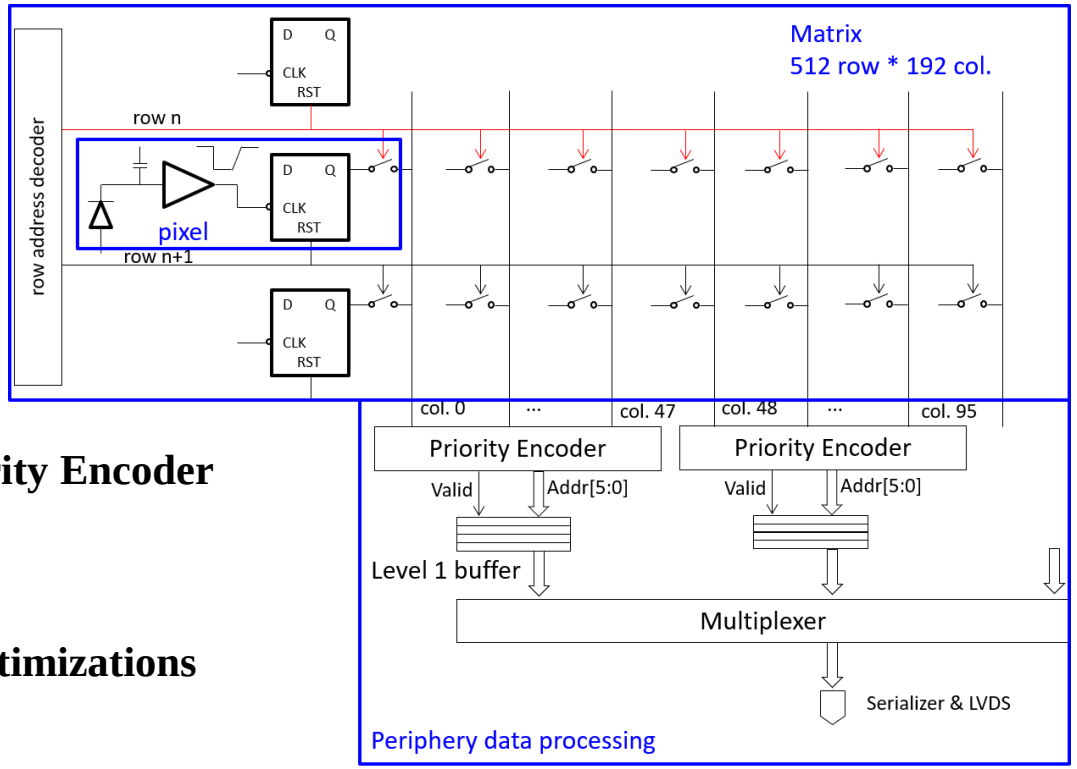
- **D-FlipFlop (DFF) used to register the 'Hit' from the discriminator**
  - **Set to 1 by the leading (falling) edge of discriminated pulse**
  - **Reset to 0 by the shared row line**
  - **Enhanced to drive the column line (capacitive)**
  - **Customized design to reduce the layout area**



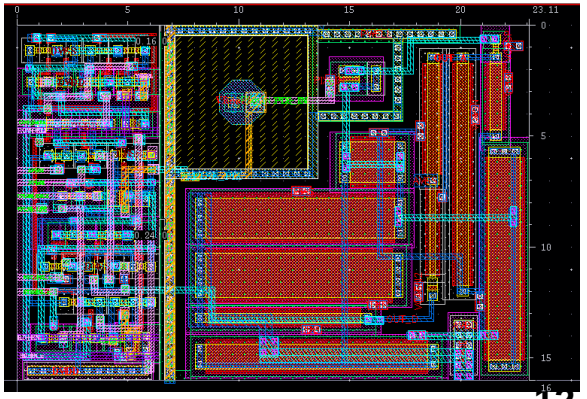


JadePix3: Rolling shutter readout of matrix

- **In-pixel circuit**
  - **Low power binary front-end**
  - **Optimized DFF**
- **Rolling shutter readout**
  - **512 row * 192 col.**
  - **One row selected at a time**
  - **102 us to finish 512 rows**
  - **Every 48 columns fed into the Priority Encoder at the end of columns.**
- **Minimum pixel size 16× 23.11 μm²**
  - **4 variants to investigate possible optimizations**



Sector	Diode	Front-end	Pixel digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	16×26 μm²
1	2 + 2 μm	FE_V0	DGT_V1	16× 26 μm²
2	2 + 2 μm	FE_V0	DGT_V2	16× 23.11 μm²
3	2 + 2 μm	FE_V1	DGT_V0	16×26 μm²

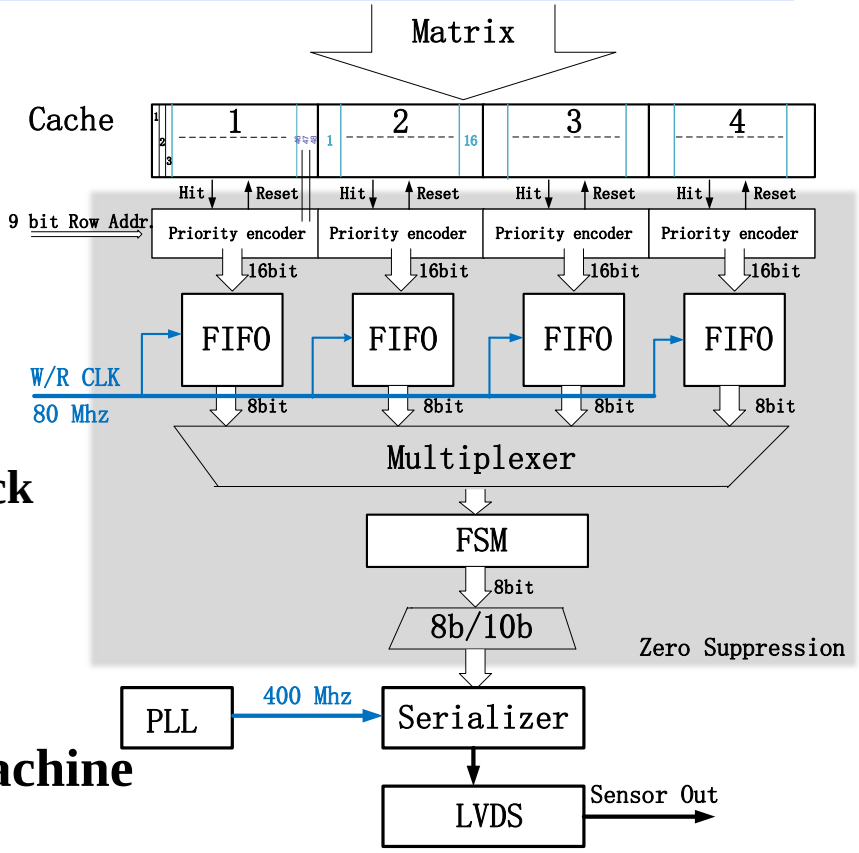


JadePix3: Periphery data processing

- **Zero suppression at the end of column**
  - **Each 48 columns divided into 16 blocks**
  - **'Fired' blocks identified sequentially by a 4-bit priority encoder**
  - **12.5 ns * 16 blocks = 200 ns/row**
- **Only hit information fed into FIFO**

Row #	Block #	hits in block
9-bit	4-bit	3-bit

  - **FIFO R/W clk: 80 MHz**
  - **FIFO depth: 48**
- **Data stream steered by a Finite State Machine**
- **Data after 8b/10b: 800 Mbit/s**
- **Estimated Power consumption 60mW**
  - **15mW (Zero suppression), 25mW (Serializer), 20mW (PLL)**

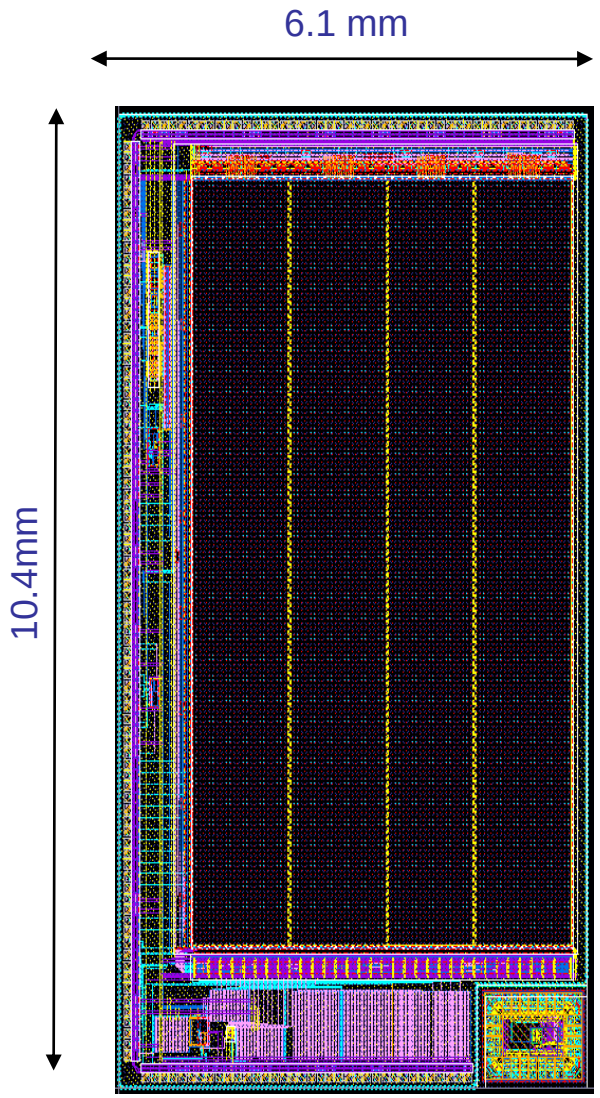


JadePix3: Status

- **Submitted in Oct. 2019**
  - **10.4mm * 6.1 mm**
- **Minimum pixel size 16× 23.11 μm^2**
  - **Rolling shutter readout 102 us/frame**
- **Estimated power consumption ~ 51 mW/cm^2**
  - **9mW/cm^2 (Pixel)**
  - **30mW/cm^2 (Zero suppression)**
  - **6.25mW/cm^2 (Serializer)**
  - **5mW/cm^2 (PLL)**

  } If shared by 1 * 2 cm^2 chip

- **Design team**
  - **IHEP: Yunpeng Lu, Ying Zhang, Yang Zhou, Zhigang Wu, Qun OuYang**
  - **CCNU: Yang Ping, Weiping Ren, Le Xiao, Di Guo, Chenxing Meng, Anyang Xu, Xiangming Sun**
  - **Dalian Minzu Unv: Zhan Shi**
  - **SDU: Liang Zhang**



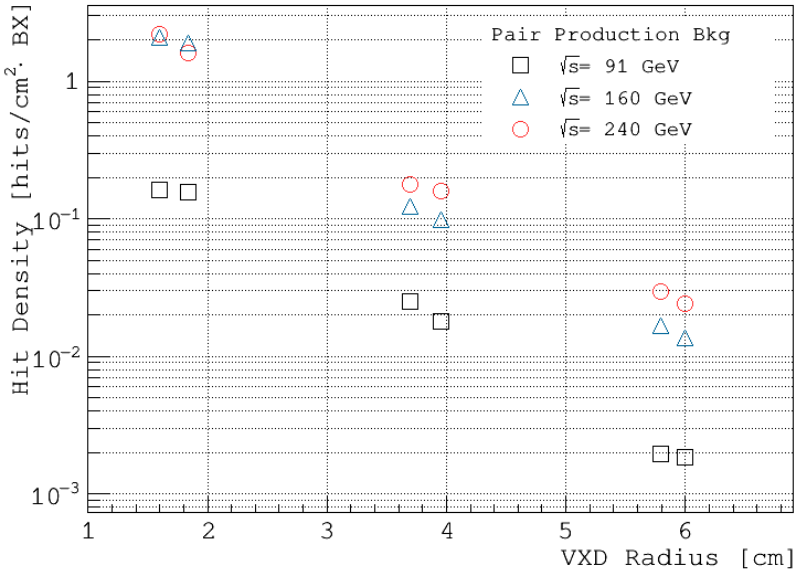
Outline

- CEPC Vertex Detector Concept
- Design activities for the full size sensor
  - Fine pitch low power approach
  - Fast readout approach
- Recent Status of the sensor designs
  - Jadepix3
  - TaichuPix1
  - Test & plans

Main specs of the full size chip for high rate vertex detector

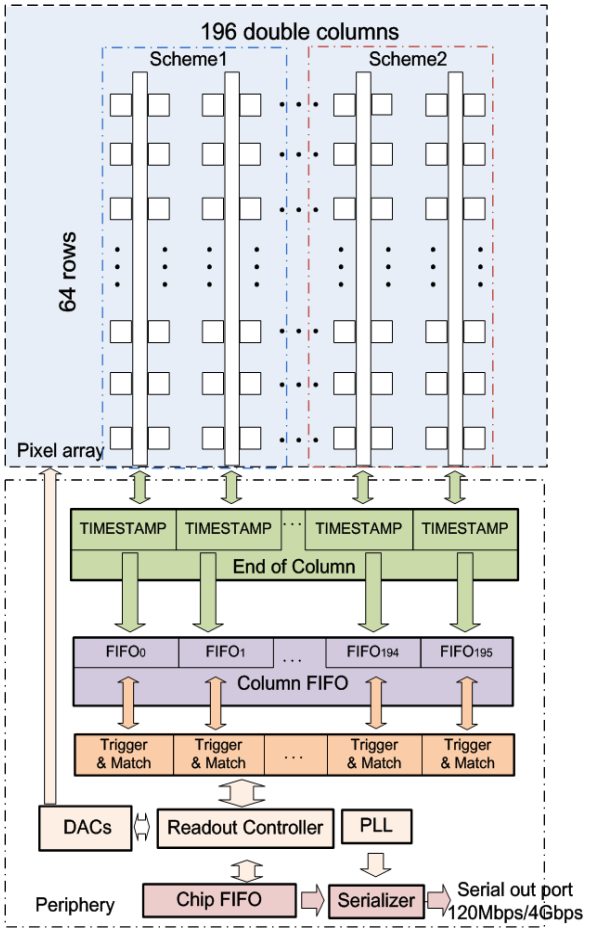
- **Bunch spacing**
  - **Higgs: 680ns; W: 210ns; Z: 25ns**
  - **Meaning 40M/s bunches (same as the ATLAS Vertex)**
- **Hit density**
  - **2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z**
- **Cluster size: 3pixels/hit**
  - **Epi- layer thickness：~18μm**
  - **Pixel size：25μm×25μm**

From the CDR of CEPC

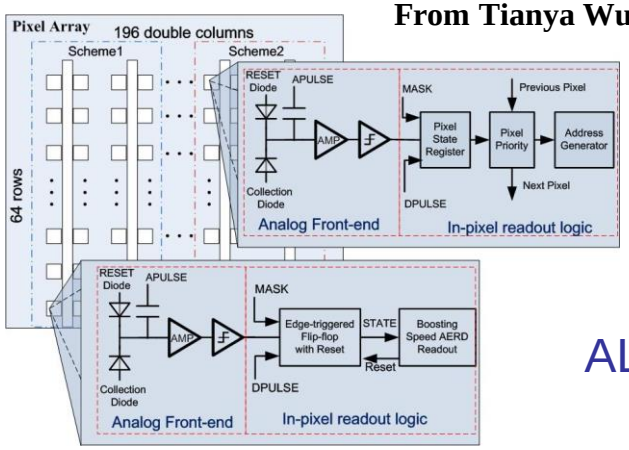


For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm^2 (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm

New proposed architecture by TaichuPix



From Tianya Wu in User Manual



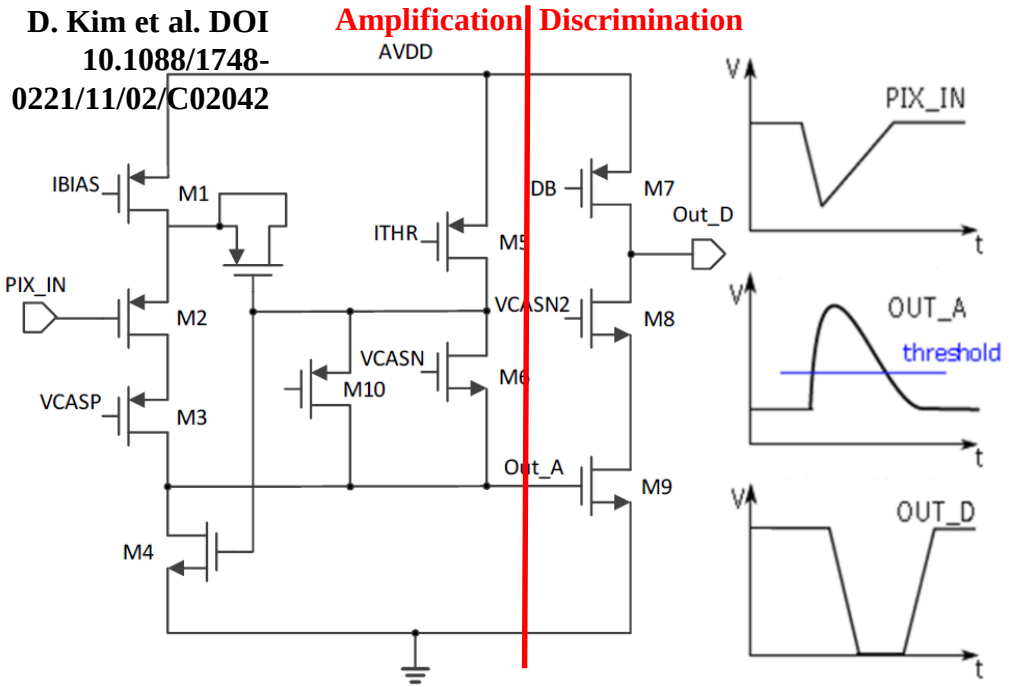
FE-I3-like Pixel

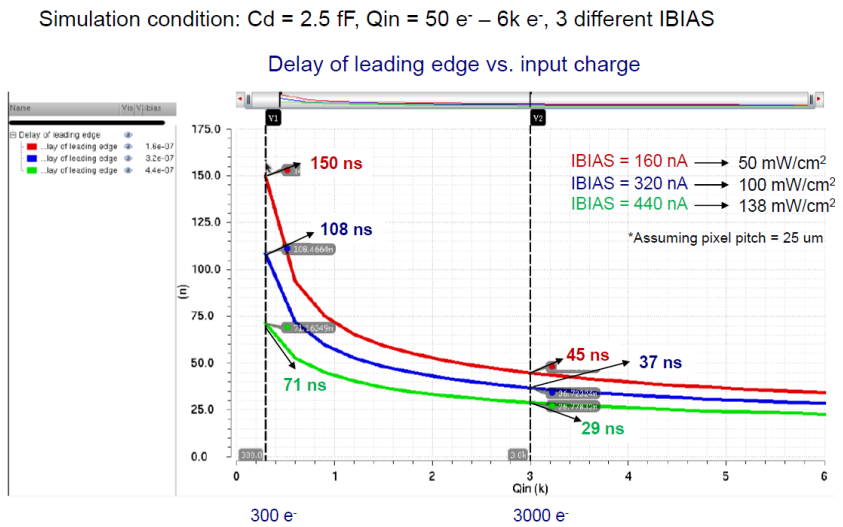
ALPIDE-like Pixel

- **Similar to the ATLAS ITK readout architecture: "column-drain" readout**
  - **Priority based data driven readout**
  - **Modification: time stamp is added at EOC whenever a new fast-or busy signal is received**
  - **Dead time: 2 clk for each pixel (50ns @40MHz clk), negligible compared to the average hit rate**
- **2-level FIFO architecture**
  - **L1 FIFO: In column level, to de-randomize the injecting charge**
  - **L2 FIFO: Chip level, to match the in/out data rate between the core and interface**
- **Trigger readout**
  - **Make the data rate in a reasonable range**
  - **Data coincidence by time stamp, only matched event will be readout**

Pixel architecture – Analog

D. Kim et al. DOI 10.1088/1748-0221/11/02/C02042



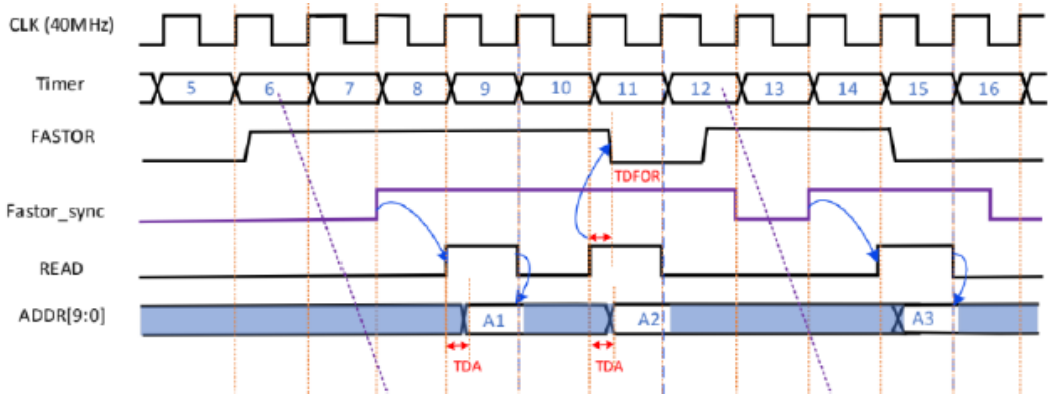


Y. Zhang for the CEPC Vertex MOST2 group meeting

- **Digital-in-Pixel scheme: in pixel discrimination & register**
- **Pixel analog is derived from ALPIDE (and benefit from MIC4 for MOST1)**
  - **As most of ATLAS-MAPS sensors' scheme**
- **Biasing current has to be increased, for a peaking time of ~25ns**
  - **Now in MOST1 ~2us peaking time was designed, too slow for 40MHz BX**
- **Consequence:**
  - **Power dissipation increased**
  - **Modified TJ process for ATLAS has to be used**
    - **With faster charge collection time, otherwise only fast electronics is of no meaning**

Design effort aiming for 40MHz BX on digital

- **ALPIDE-like scheme：**
  - **Fast-Or bus added to record the column hit time stamp**
  - **Boosting speed of the AERD (Address-Encoder & Reset-Decoder）**
    - **To shift the Fast-Or by a half of the clock cycle**
      - **More margin in the timing constraint of the periphery circuit**



Normal AERD

SS ; 1.6V ; 50°C	
Signal	Delay
FASTOR	14. 3ns
READ	14. 3ns
TDA	28ns
TDFOR	1. 3ns

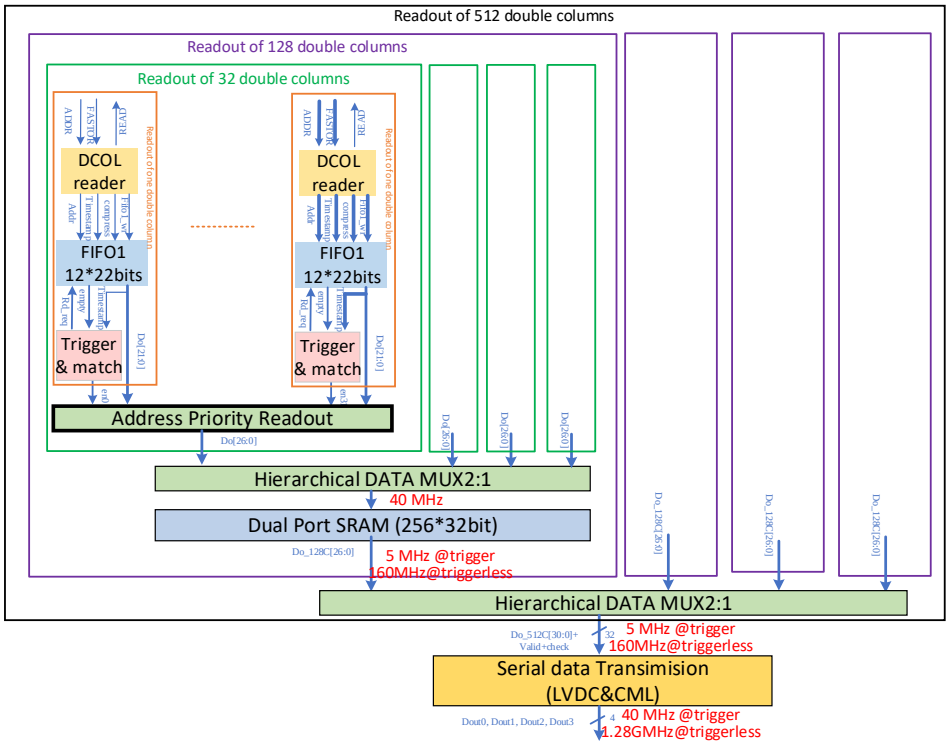
Boost AERD

SS ; 1.6V ; 50°C	
Signal	Delay
FASTOR	14. 3ns
READ	14. 3ns
TDA	25. 5ns
TDFOR	1. 3ns

TY. Wu for the CEPC Vertex MOST2 group meeting

- **FE-I3-like scheme：**
  - **Simplify the pixel cell logic**
  - **All the logic gates were re-designed with fully customized layout**
    - **For smaller pixel size**

Full chip periphery logic design

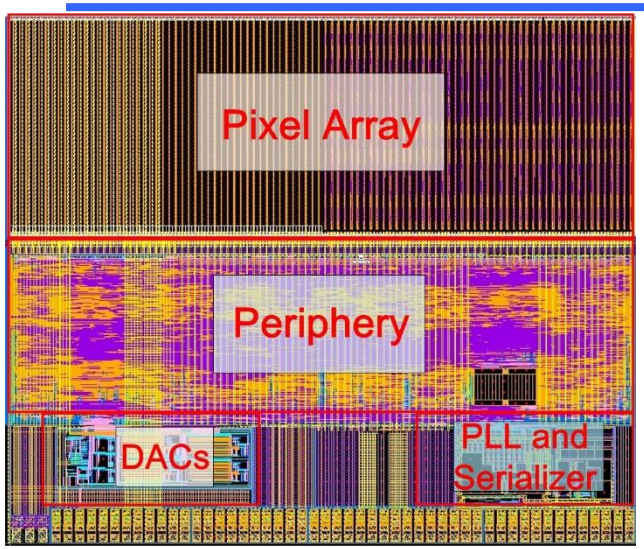


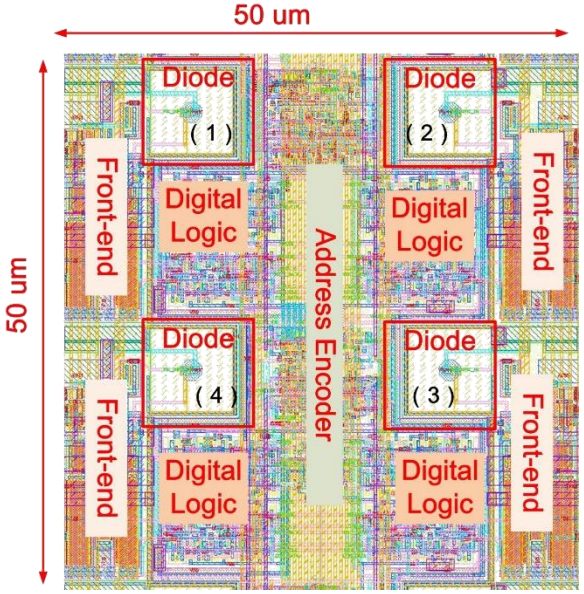
- **Main Functionality:**
  - **Trigger/Triggerless readout mode compatible**
    - **Data coincidence and trigger window logic**
  - **Two level FIFOs for hit derandomization**
  - **High speed serialization for data readout**
    - **4Gbps data rate capability**

From X.M. Wei for the CEPC Vertex MOST2 group meeting

- **Other necessary blocks**
  - **Slow control of the pixel array and full chip via SPI interface**
  - **Bias generation by current- and voltage- DACs**
  - **Clock management: Phase Lock Loop and serializer**
  - **Power management: LDOs for on-chip low ripple power supply**
  - **High speed interface: CML & LVDS Drivers**

TaichuPix Chip Status





Chip size：5mm×5mm
Pixel size：25μm×25μm

- First MPW tapeout of TaichuPix was submitted in June
- Chip received in Nov.
  - With 60 chips, 40 chips delivered to China
- One block area of 5mm×5mm was fully occupied
  - A full functional pixel array (small scale)
    - 85% of the block area
    - A 64×192 Pixel array + Periphery + PLL + Serializer
    - Bias generation included
    - I/O arranged in one edge, as the final chip
  - other independent test blocks (less critical)
    - LDO + PLL

Team organization

- **Design team:**
  - **IHEP, SDU, NWPU, IFAE & CCNU**
  - **Biweekly/weekly video design meeting on chip design (convened by IHEP)**

Institutes	Tasks	Designers
IHEP	Full chip modeling & simulation Pixel Analog, TCAD simulation High speed interface: PLL + Serializer	Wei Wei, Ying Zhang Xiaoting Li, Weiguo Lu, Mei Zhao
CCNU/IFAE	Pixel Digital	Tianya Wu, Raimon Casanova
NWPU	Periphery Logic, LDO	Xiaomin Wei, Jia Wang
SDU	Bias generation	Liang Zhang

- **Chip characterization**
  - **Test daughter boards: SDU & IFAE (Jianing Dong, IFAE)**
  - **FPGA Firmware: IHEP (Jun Hu, Wei Wei)**
  - **Electrical test: all designers + other interested parties**
  - **Irradiation test: X-ray irradiator + beam line**

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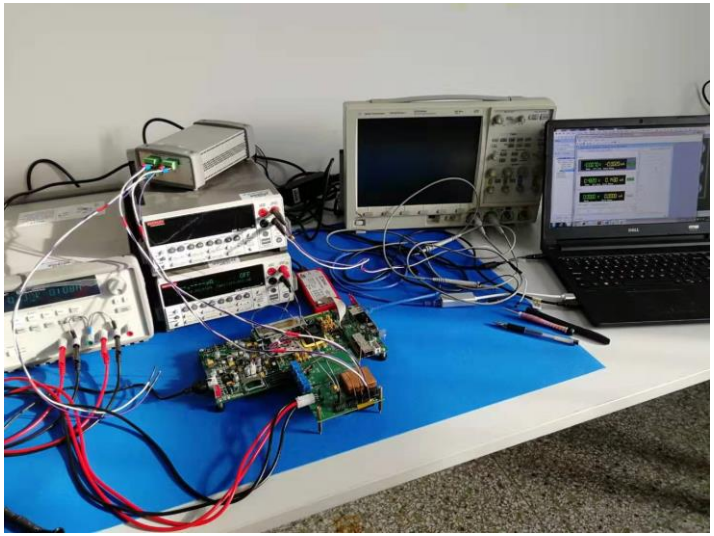
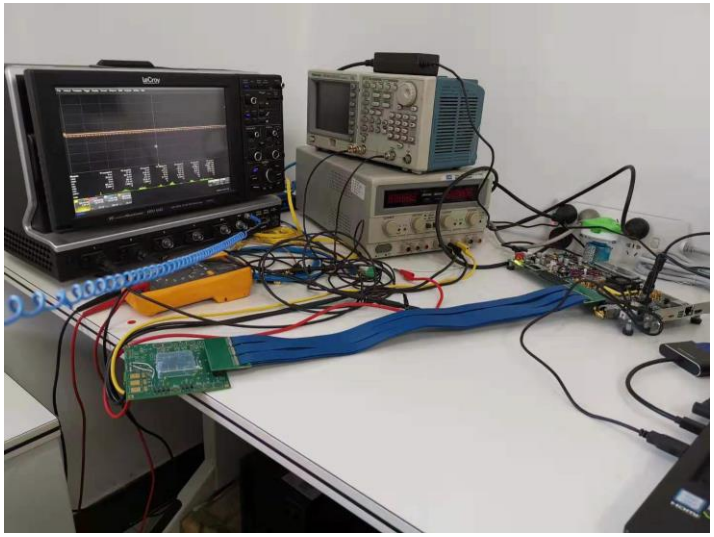
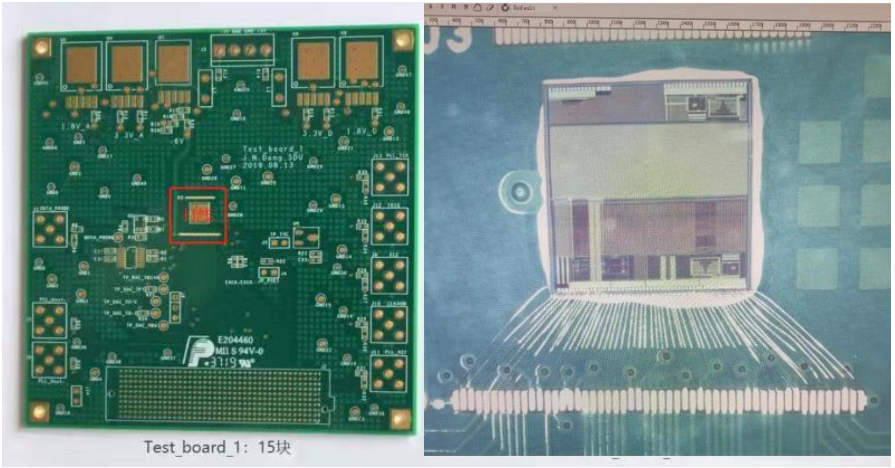
Test system



Jadepix3 test system

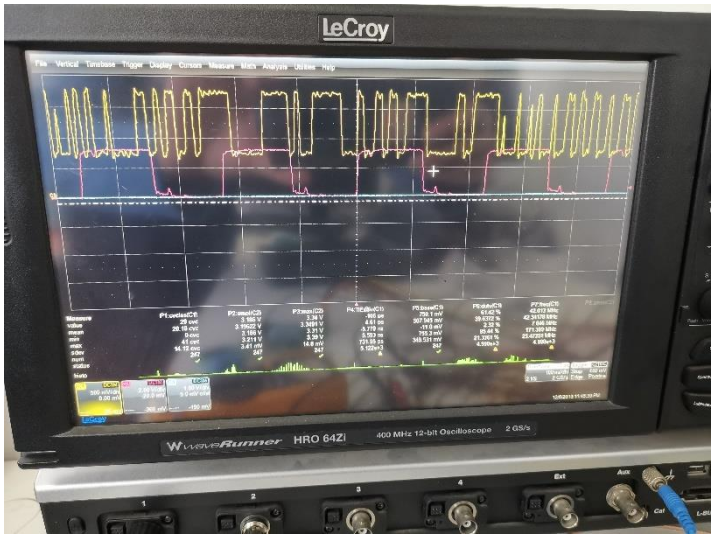


TaichuPix1 test system

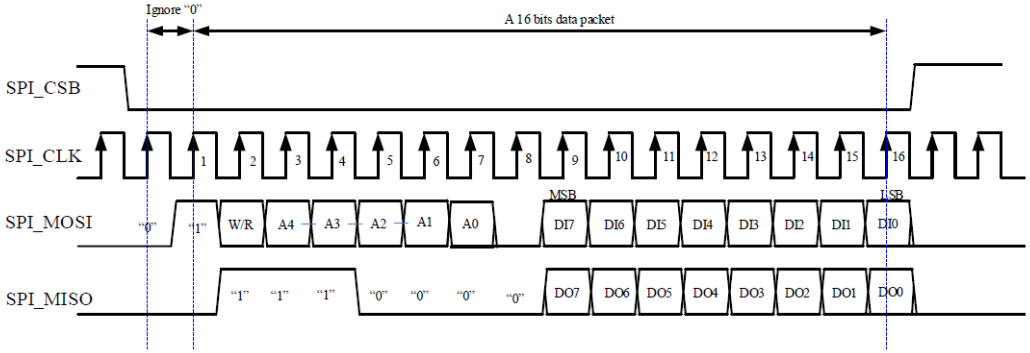


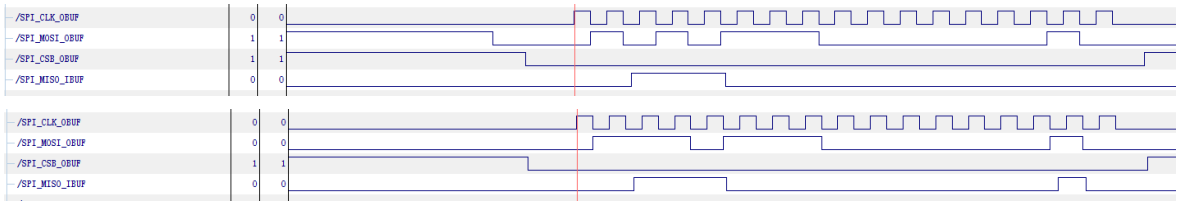
- **Test setup based on KC705 Xilinx FPGA Eva board**
  - **For Jadepix3：**
    - **FPGA firmware to be adapted to the JadePix3 interface**
    - **DAQ Software can be reused**
  - **For TaichuPix1**
    - **Communication interface with PC: SiTCP IP core & TCP/IP protocol**
    - **Downstream: TCPIP@MATLAB → SPI package@ FPGA → TaichuPix Periphery**
    - **Upstream : TaichuPix Serializer → FIFO@FPGA → TCPIP@MATLAB**

TaichuPix1 preliminary test status



Serializer PRBS test stream @160Mbps





SPI incoming & outcoming stream by ChipScope

- **Chip in test only for two weeks…**
- **Signs for the chip functionality:**
  - **PLL evaluated: locked@40MHz -> central freq. 2.24GHz**
    - **First condition of Triggerless capability satisfied**
  - **Serializer PRBS test @160Mbps stream observed**
  - **SPI control & output stream succeed**
  - **Periphery + Serializer combined test verified**
  - **…**
- **Analog part to be tested**

Recent plans

- **Jadepix3 is going to be tested in June 2020**
- **The potential of the SOI-3D process will be explored by IHEP group**
  - **may bring about new design space in terms of shrinking the pixel size**
- **TaichuPix2 is about to be submitted in Feb. 2020**
  - **A fully functional chip was proposed with all the blocks integrated as in the full size chip**
    - **Pixel Matrix 64*192 + Periphery + DACs + PLL + Serializer + LDOs**
  - **New features will be studied in TaichuPix2**
    - **With chip-to-chip interconnection buses**
    - **More testability added**

Summary

- **Two recent CMOS pixel sensor designs were discussed**
- **Jadepix3 for low power fine pitch objective**
  - **Minimum pixel size 16× 23.11 μm^2**
  - **Estimated power consumption ~ 55 mW/cm^2**
  - **Rolling shutter readout 102 us/frame**
- **TaichuPix1 for fast readout full functional objective**
  - **New scheme proposed based on column-drain architecture**
    - **Event driven and time stamp, 2-level FIFOs,**
  - **Triggerless compatibility**
    - **Possible to run @ 40MHz BX with high efficiency**
- **Test is progressing well for the system design and chip verification**

Thank you !