New structure of digital pixel evaluation

Tianya Wu

CEPC MOST2 Chips Meeting

twu@ifae.es

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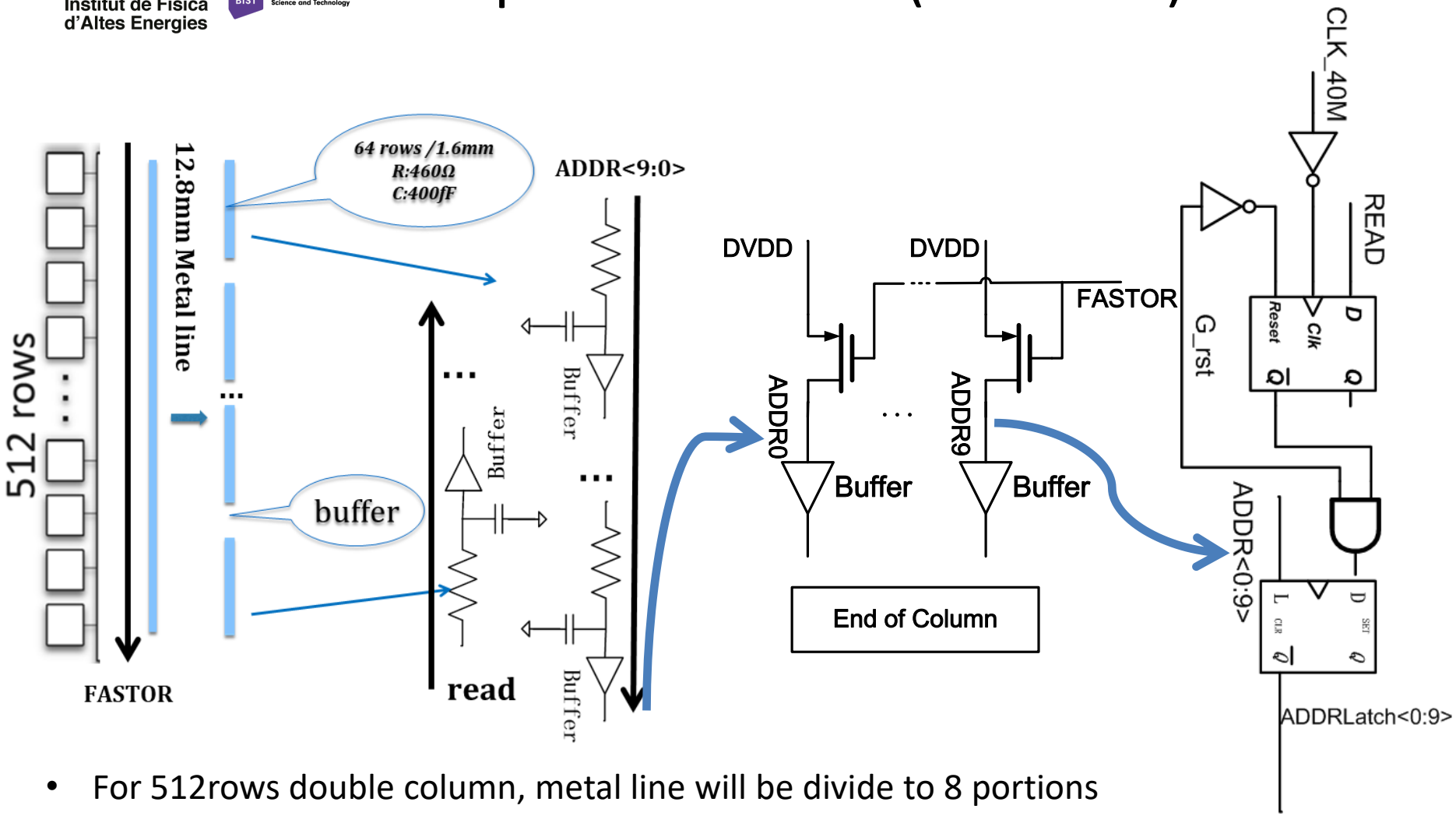
華中師範大學
CENTRAL CHINA NORMAL UNIVERSITY

OUTLINE

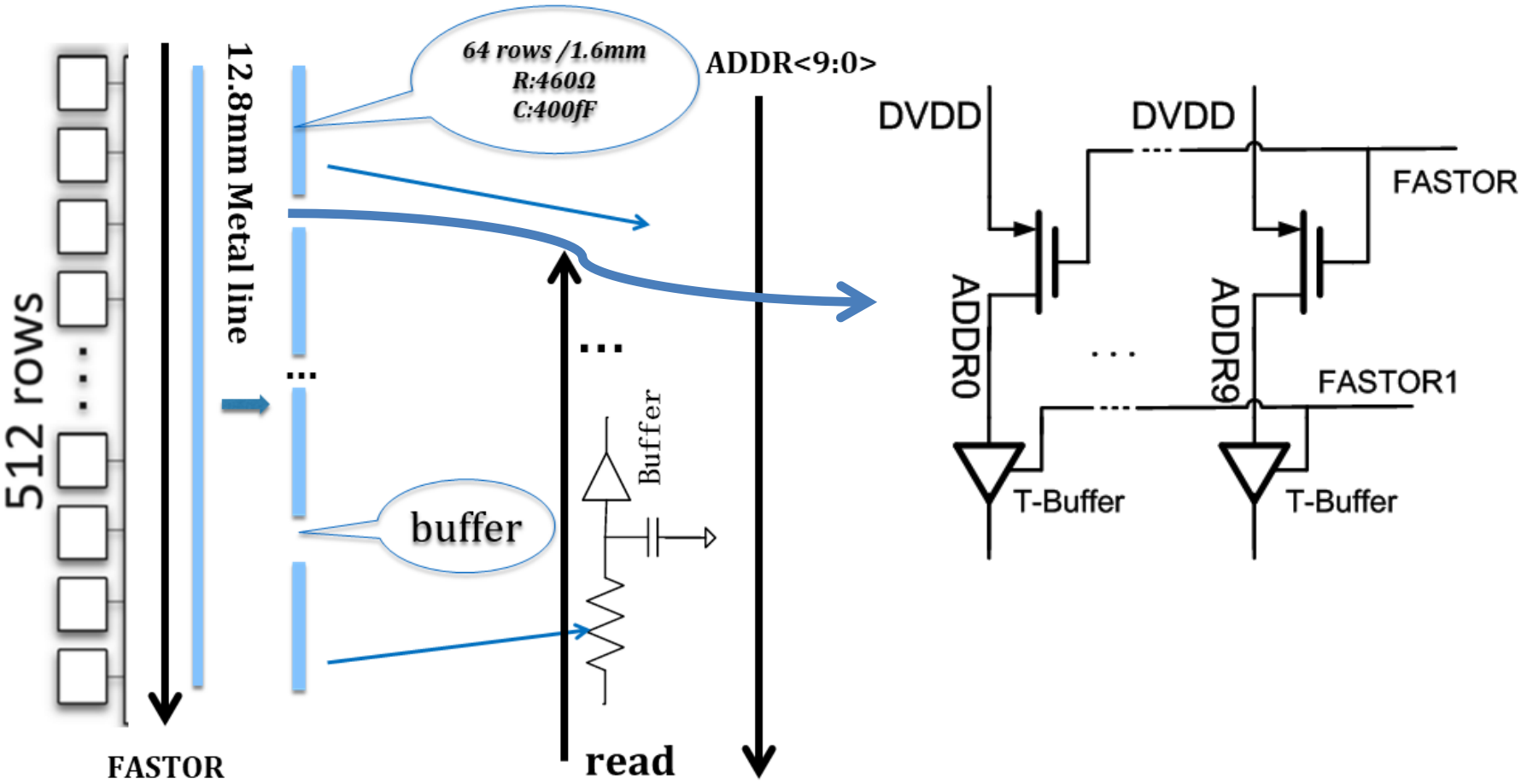
- Principle of scheme1(FE-I3 like)
- Principle of scheme2(ALPIDE like)
- Simulation results
- A possible solution for SuperPixel
- Summary

Principle of scheme1(FE-I3 like)



- For 512rows double column, metal line will be divide to 8 portions
- The Pull-up transistors will latch the address at the EoC.
- Duty cycle latch circuitry is used to adjust the READ signal.

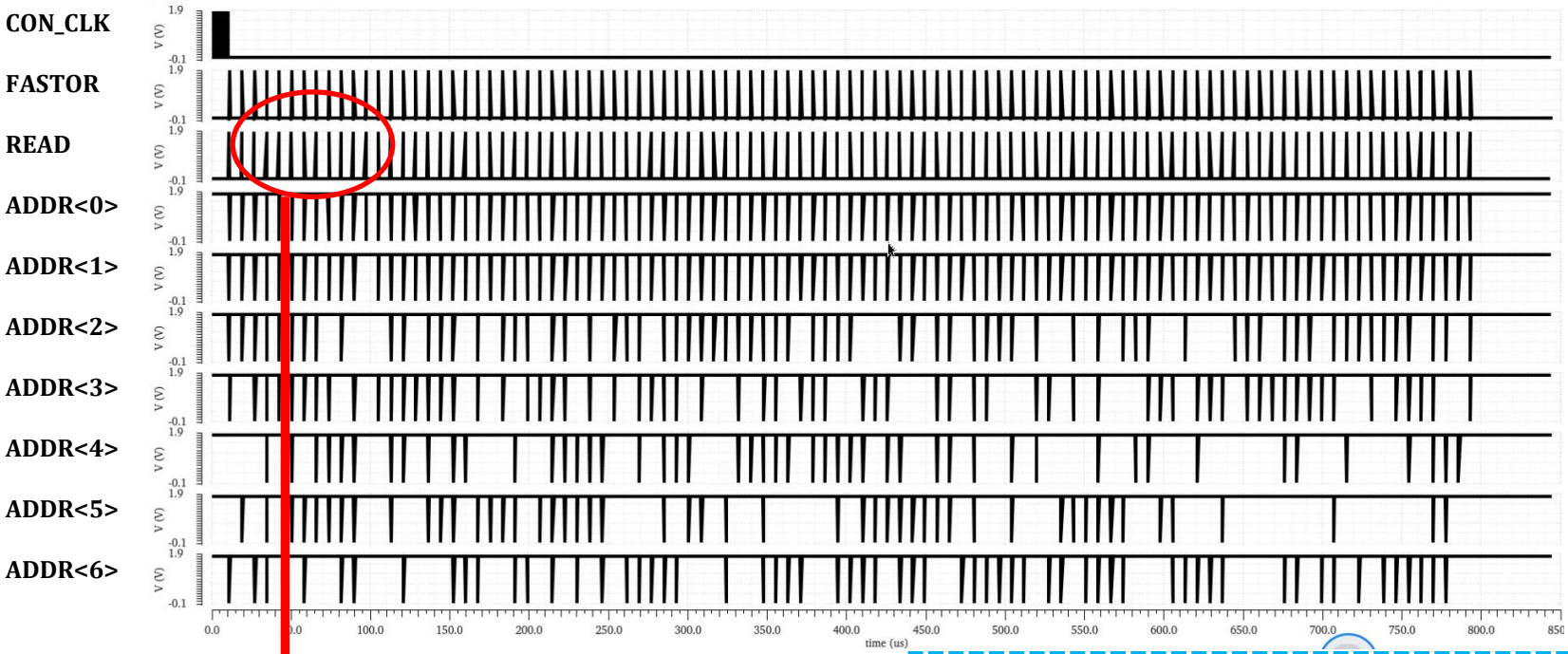
Principle of scheme2(ALPIDE like)

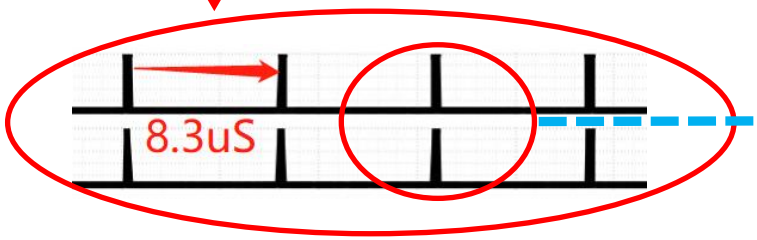


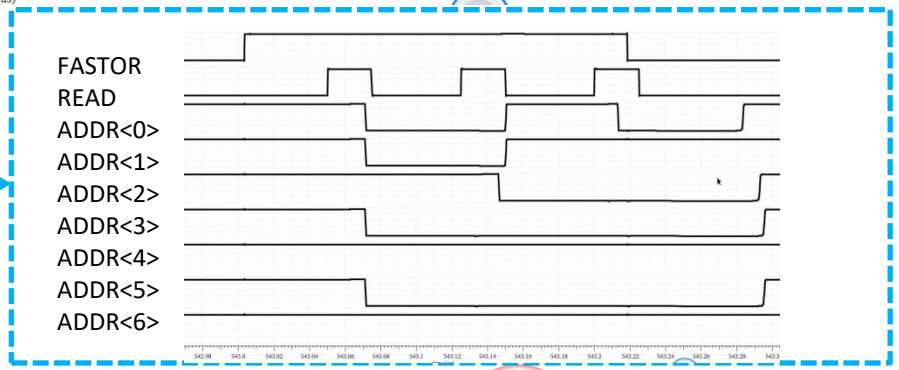
- the output of AERD should keep high-z state when there is no hit.
- The tristate buffer is used to control each portion of AERD.
- The Pull-up transistors will latch the address at the EoC.

Simulation of power density

Simulation condition: The waveform shows the result of scheme 1. Every 8.3us generates 3 random hits.

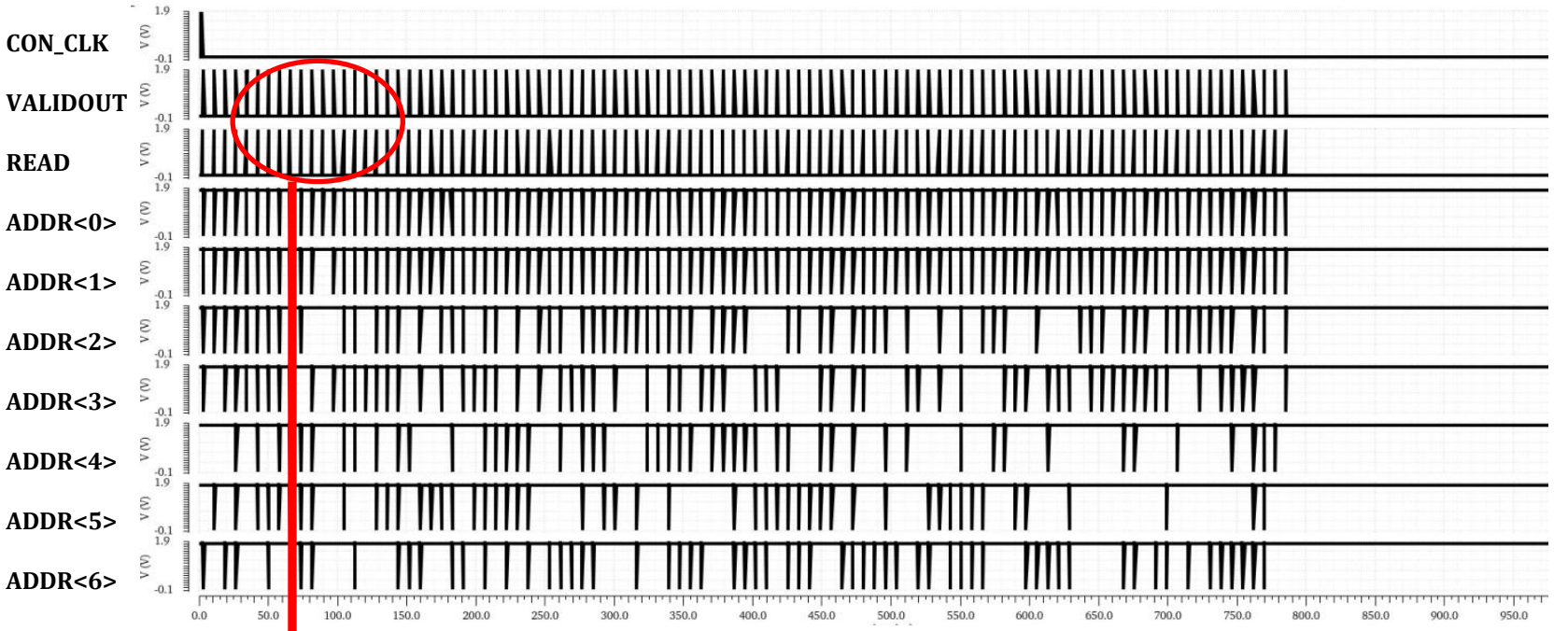


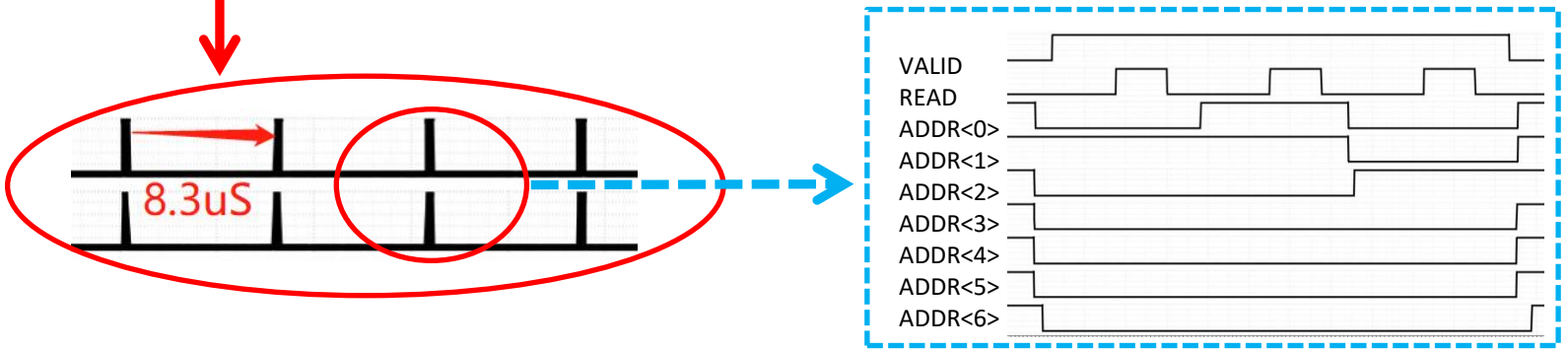




Simulation of power density

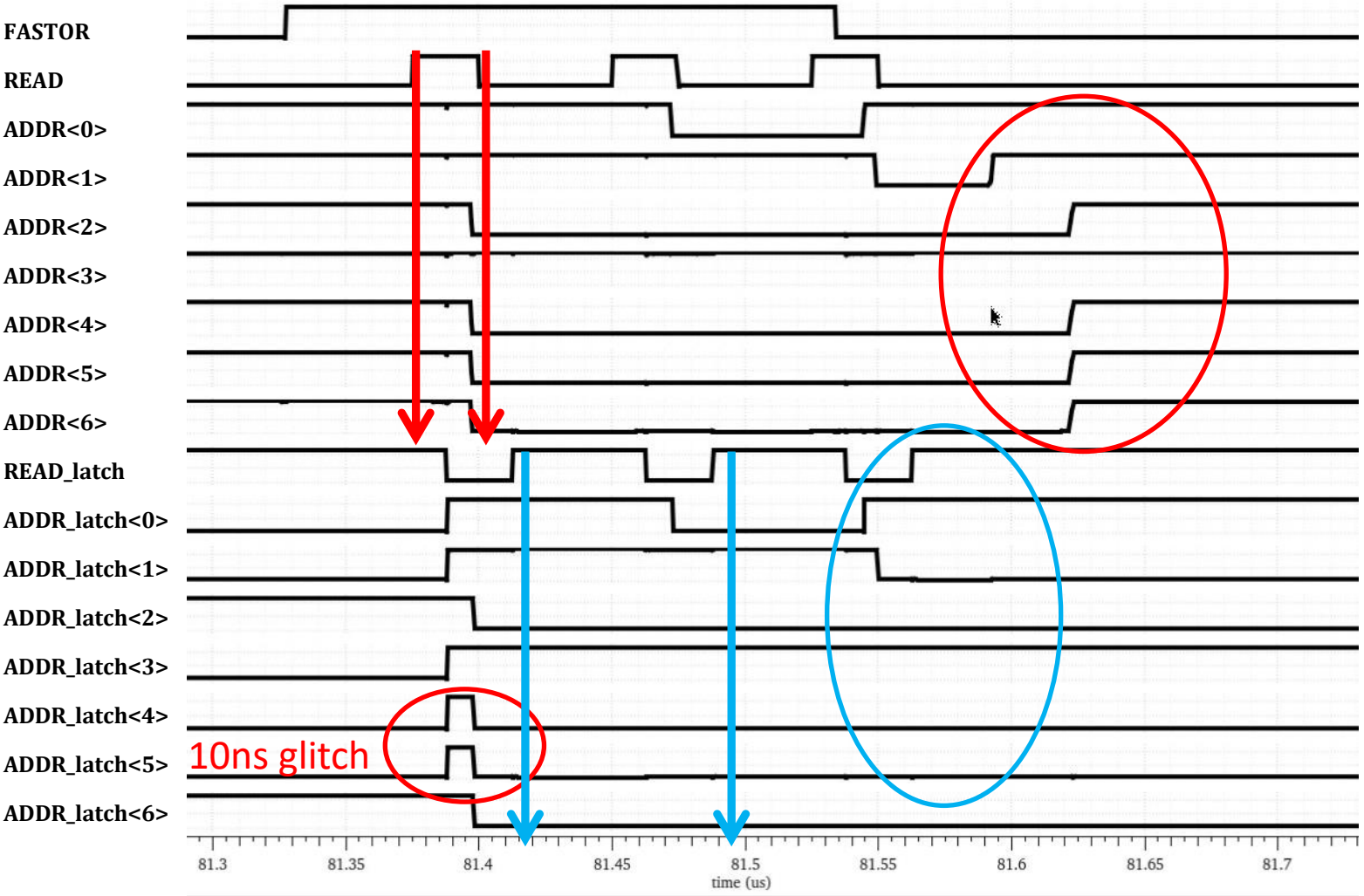
Simulation condition: The waveform shows the result of scheme2. Every 8.3us generates 3 random hits.





Simulation of data latch

Simulation condition: Latch the data at the end of column, with the duty cycle of read signal 37.5+12.5



Simulation of power density (Martrix:512x1024)

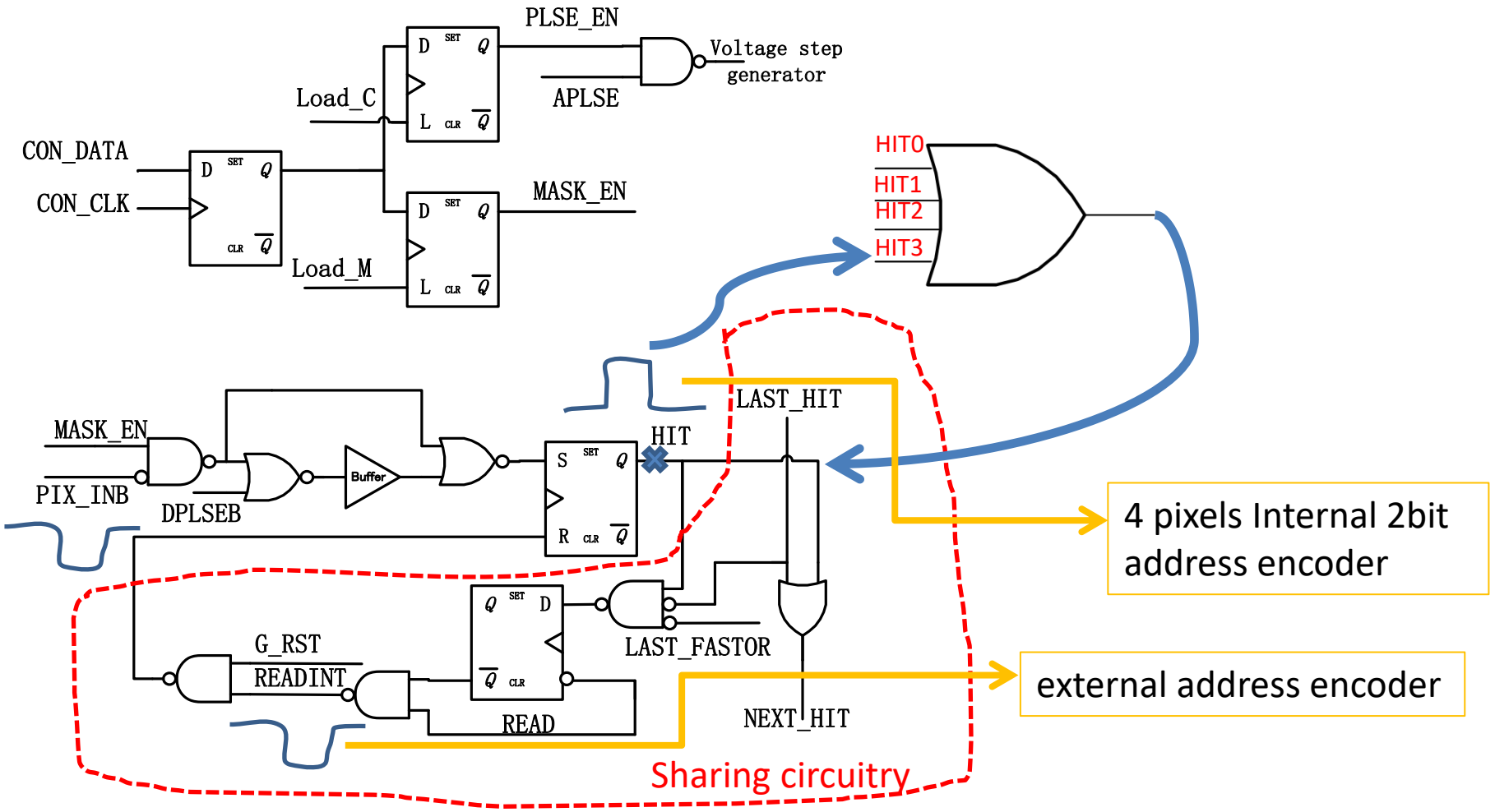
Simulation condition: Both of schemes are based on pull up transistors, without latch part.

Average Power	FEI3 upgrade	ALPIDE upgrade
Initialization phase	161.366uA	211.13uA
Readout phase(max)	271.516uA	353.08uA
Static phase	47.4nA	3.43uA
Average current (every 8.3us)	8.786uA	12.846uA
Power density during readout phase	76.36mW/cm2	99.303mW/cm2
Power density average	2.46mW/cm2	3.61mW/cm2

Calculation of Power density:

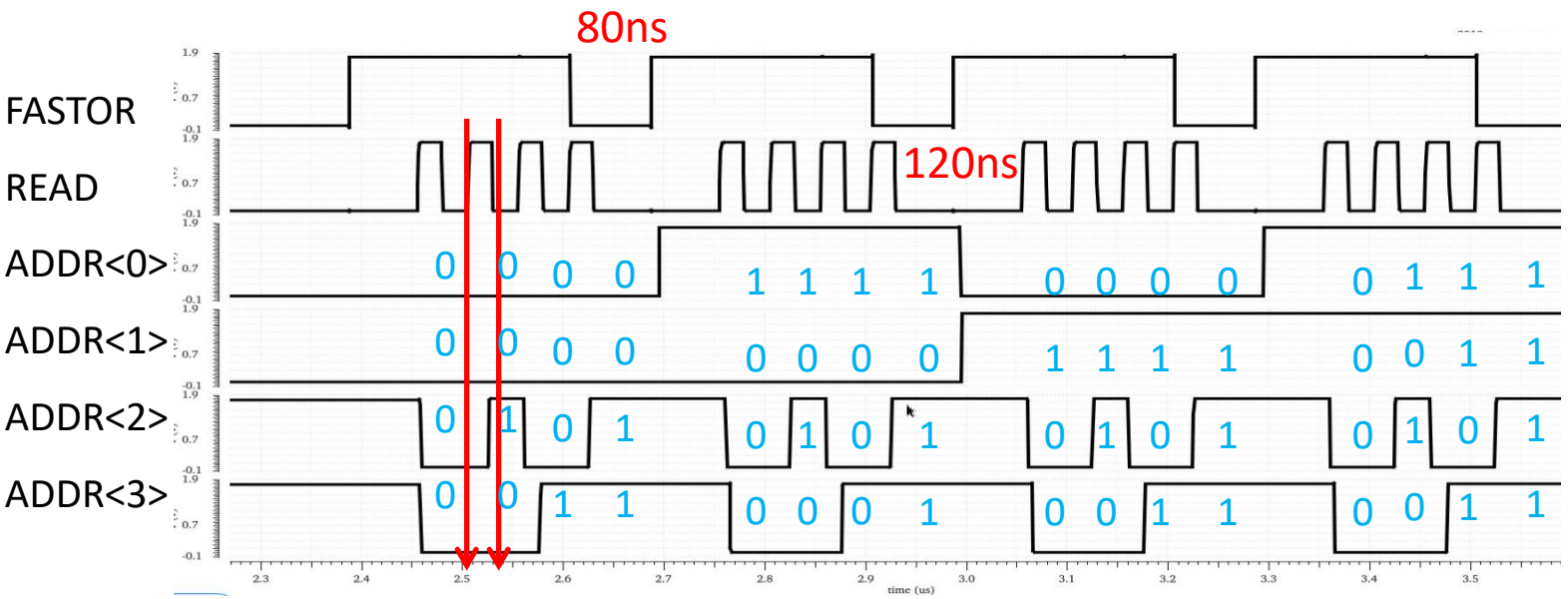
Power density(FE-I3)= 271.516uA*1.8V / (512x25umx50um) =76.36mW/cm2

A possible solution for SuperPixel



Simulation result

- Simulation condition: Generate 4 hits for each superPixel at the same time
- The inside time space for each Superpixel is 300ns.
- Some events will be missed when the inside time space is less than 230ns.
- One superPixel can record only one event at one point.
- FE-I3 like structure will read the data at the falling edge.



Summary

- We are going to use 37.5ns+12.5ns structure?
- How big is the matrix of our next submission?
- If READ latch circuitry works, shall we use the normal ALPIDE structure?
- It seems hard to implement superPixel in next MPW.

Next work:

- Complete final schematic for the next submission.
- Study the feasibility of extending the layout of AERD structure.

Institut de Física d'Altes Energies

EXCELENCIA SEVERO OCHOA

BIST Barcelona Institute of Science and Technology

Thanks for your attention.

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