Status and plan of the TaichuPix chip for the high-rate CEPC Vertex Detector

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On behalf of the CEPC MOST2 Vertex detector design team

2019-12-25

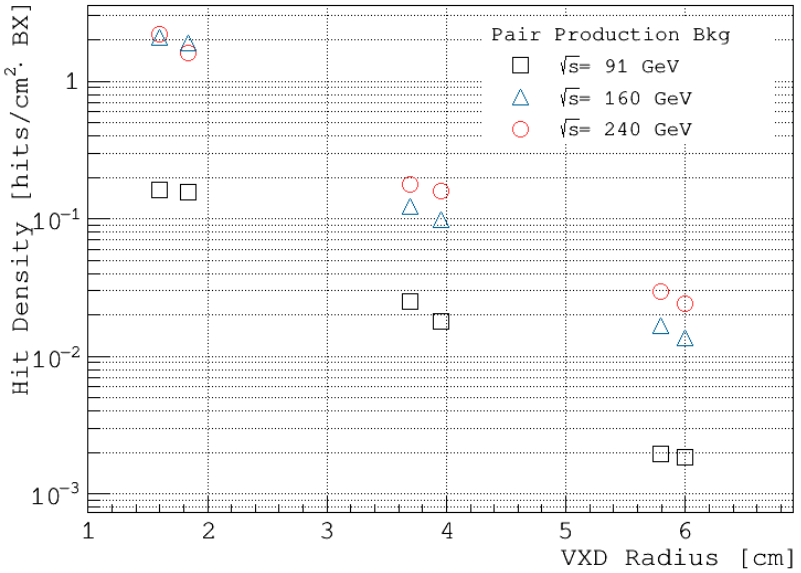
Outline

- **Status of the first MPW submission**
- **Status of the preliminary test**
- **Recent design status and plan**

Main specs of the full size chip for high rate vertex detector

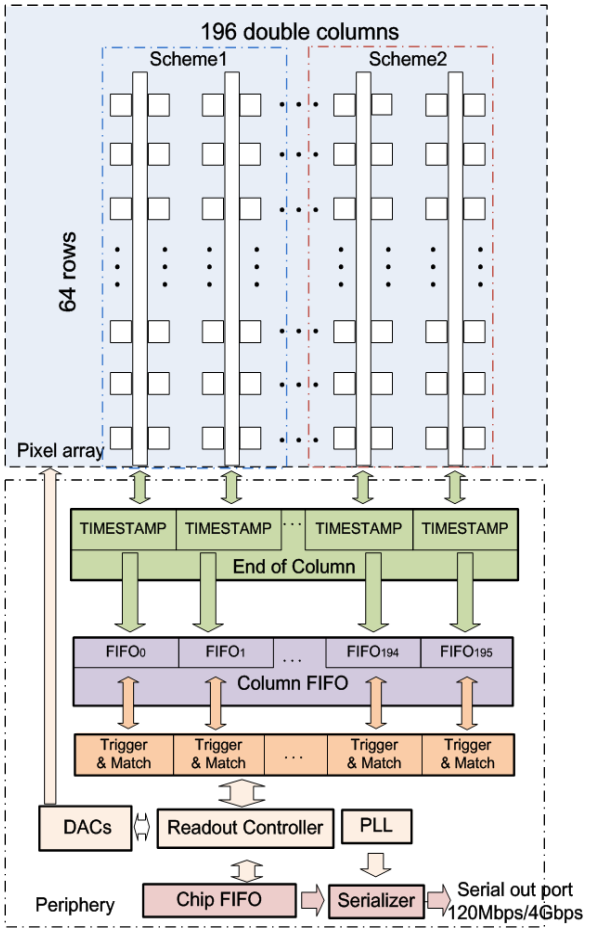
- **Bunch spacing**
  - **Higgs: 680ns; W: 210ns; Z: 25ns**
  - **Meaning 40M/s bunches (same as the ATLAS Vertex)**
- **Hit density**
  - **2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z**
- **Cluster size: 3pixels/hit**
  - **Epi- layer thickness：~18μm**
  - **Pixel size：25μm×25μm**

From the CDR of CEPC

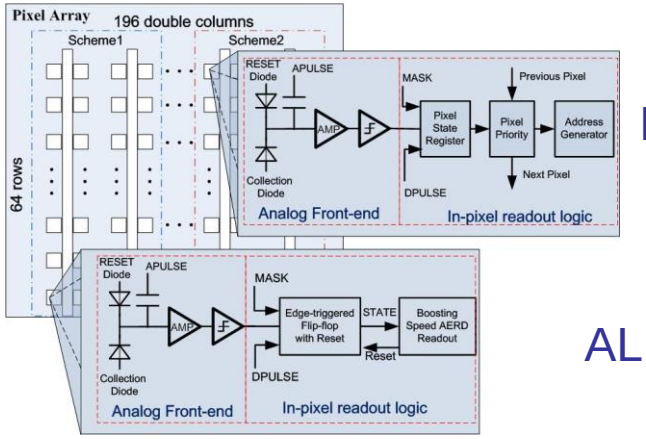


For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm^2 (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm

New proposed architecture by TaichuPix1



From Tianya Wu in User Manual

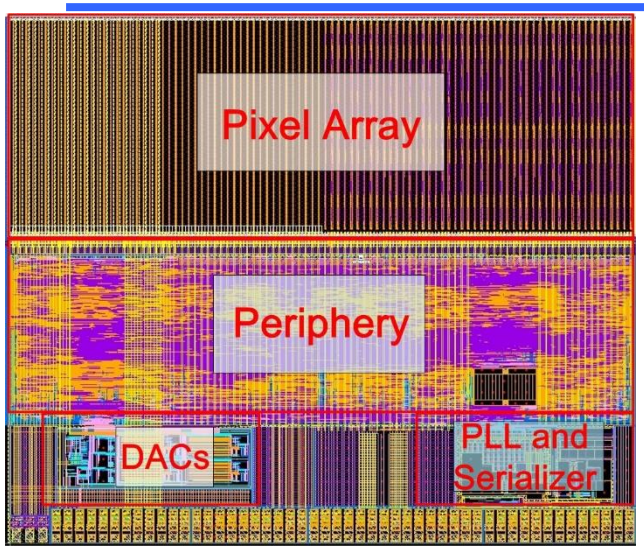


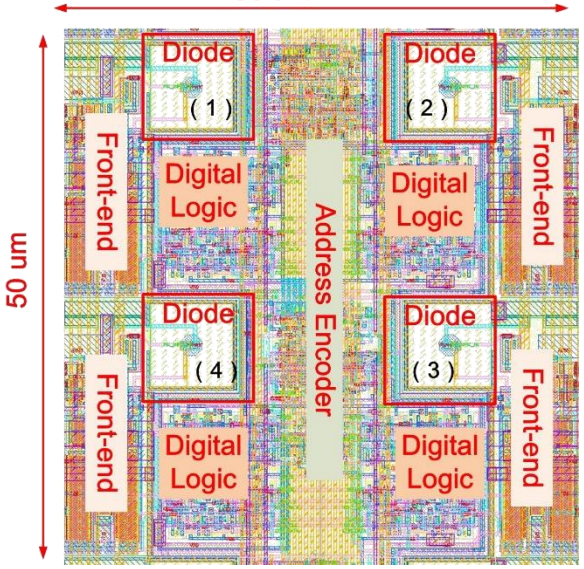
FE-I3-like Pixel

ALPIDE-like Pixel

- **Similar to the ATLAS ITK readout architecture: "column-drain" readout**
  - **Priority based data driven readout**
  - **Modification: time stamp is added at EOC whenever a new fast-or busy signal is received**
  - **Dead time: 2 clk for each pixel (50ns @40MHz clk), negligible compared to the average hit rate**
- **2-level FIFO architecture**
  - **L1 FIFO: In column level, to de-randomize the injecting charge**
  - **L2 FIFO: Chip level, to match the in/out data rate between the core and interface**
- **Trigger readout**
  - **Make the data rate in a reasonable range**
  - **Data coincidence by time stamp, only matched event will be readout**

Chip Status

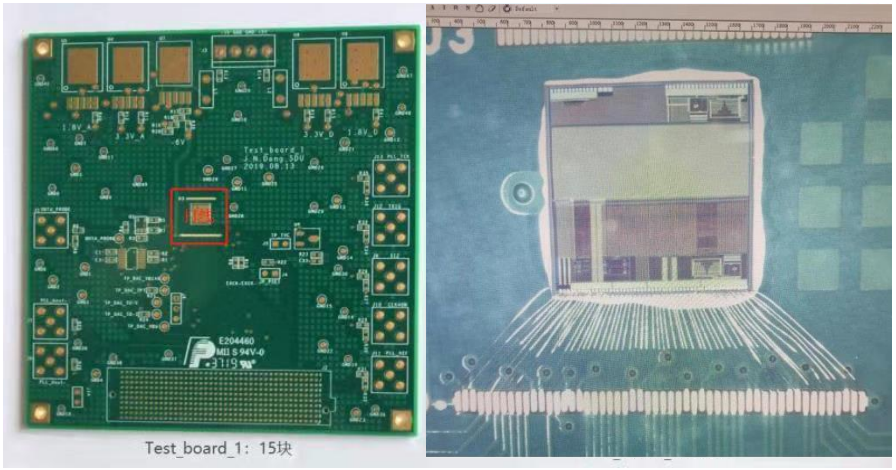


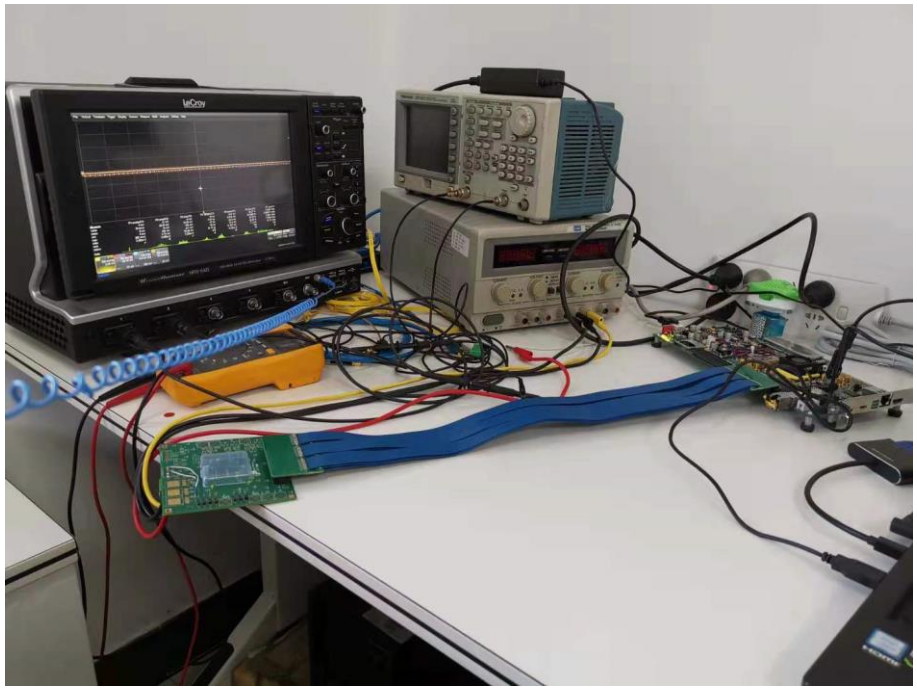


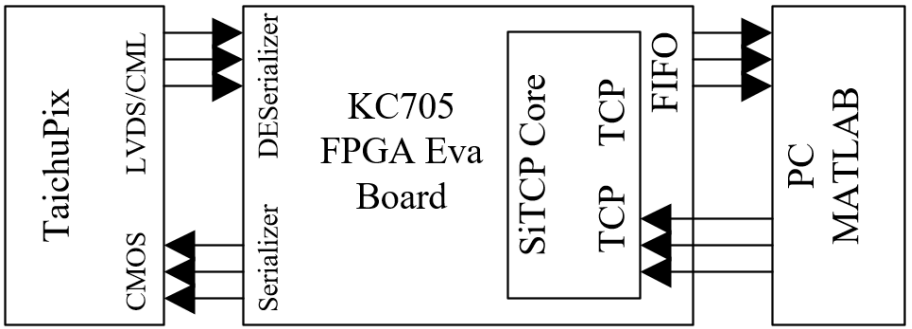
Chip size：5mm×5mm
Pixel size：25μm×25μm

- First MPW tapeout was submitted in June
  - Thanks IFAE for their tunnel for submission to TJ
- Chip received in Nov.
  - With 60 chips, 40 chips delivered to China
- One block area of 5mm×5mm was fully occupied
  - A full functional pixel array (small scale)
    - 85% of the block area
    - A 64×192 Pixel array + Periphery + PLL + Serializer
    - Bias generation included
    - I/O arranged in one edge, as the final chip
  - other independent test blocks (less critical)
    - LDO + PLL
- We got the news from IFAE that to use the modified TJ, we still need to get a permit from CERN

Test setup for chip evaluation

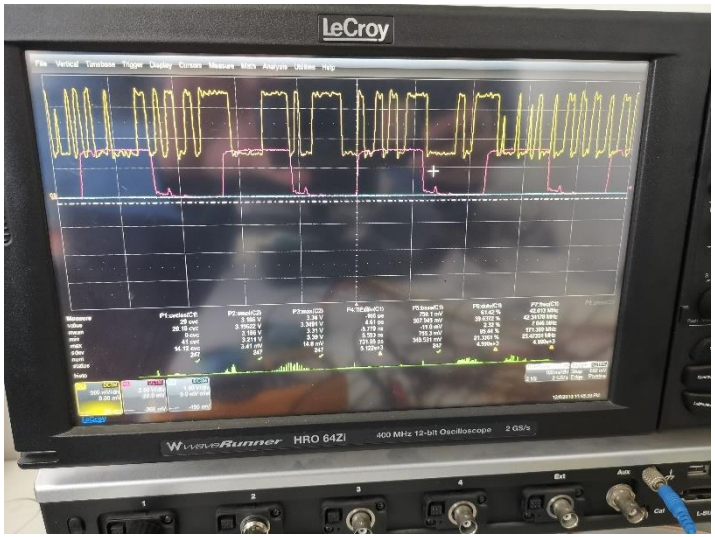




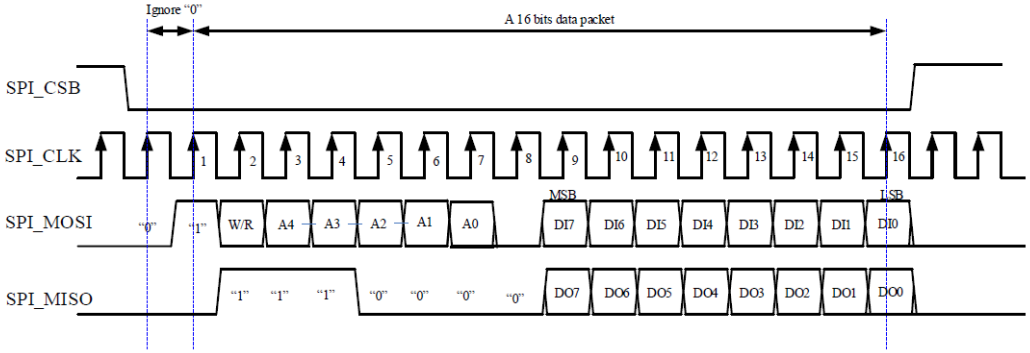


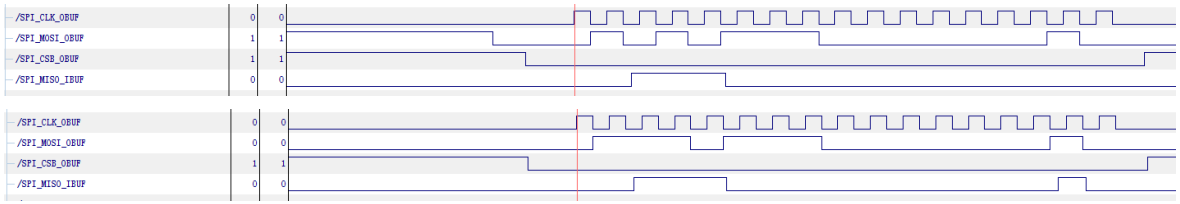
- **Test setup based on KC705 Xilinx FPGA Eva board**
- **General data stream**
  - **Downstream from PC to chip: TCPIP@MATLAB → SPI package@ FPGA → TaichuPix Periphery**
  - **Upstream from chip to PC: TaichuPix Serializer → FIFO@FPGA → TCPIP@MATLAB**
- **Test Firmware is developing in IHEP (China side) by Jun HU and Wei WEI**
  - **Debugging has just initiated in Dec.**
  - **~3~4 weeks towards firmware fully release for performance test**

Preliminary test status – signs for functionality



Serializer PRBS test stream @160Mbps





SPI incoming & outcoming stream by ChipScope

- **Chip in test only for one week…**
- **Signs for the chip functionality:**
  - **PLL evaluated: locked@40MHz -> central freq. 2.24GHz**
    - **First condition of Triggerless capability satisfied**
  - **Serializer PRBS test @160Mbps stream observed**
  - **SPI control & output stream succeed**
  - **…**
- **Analog part to be tested**

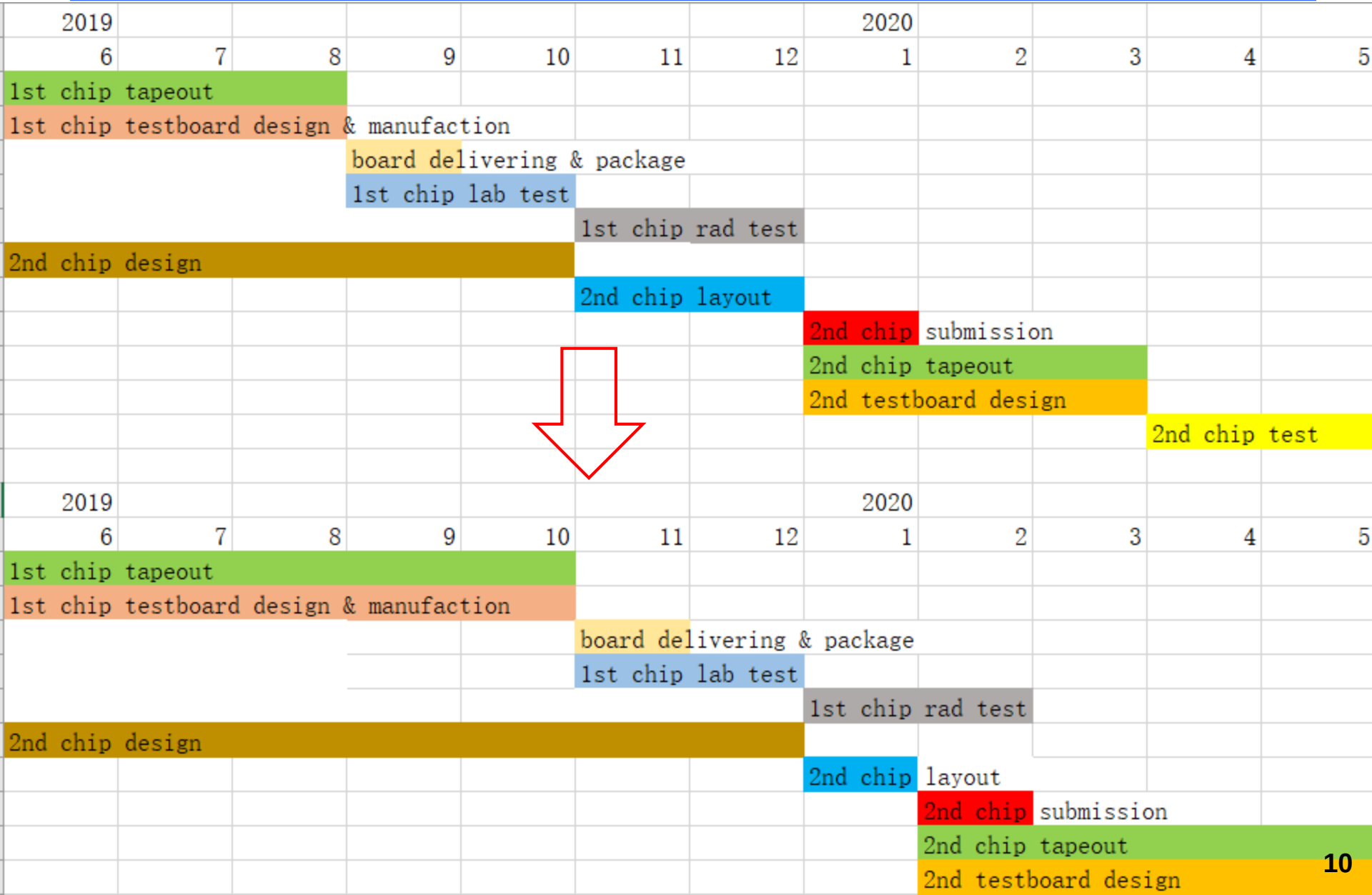
Recent chip design status

- **Possible improvements and optimizations for the next version were proposed and discussed**
  - **Design is progressing according to those directions**
- **Optimization directions**
  - **Readout scheme**
    - **To make larger headroom for the timing (✔)**
      - **Data latching @ 1clk -> 1.5clk**
    - **Address encoder pull-up added to avoid high-Z state (✔)**
  - **Area optimization**
    - **Compress the size of periphery – in progressing**
    - **Smaller pixel size**
      - **Address encoder shrunk thanks to the timing improvement (✔)**
      - **Pixel analog layout improvement still wait for the 1st MPW test results**
  - **Data interface finalization**
    - **Serializer frequency and data stream protocol**
      - **Waiting for the test results to see the highest possible clock frequency**

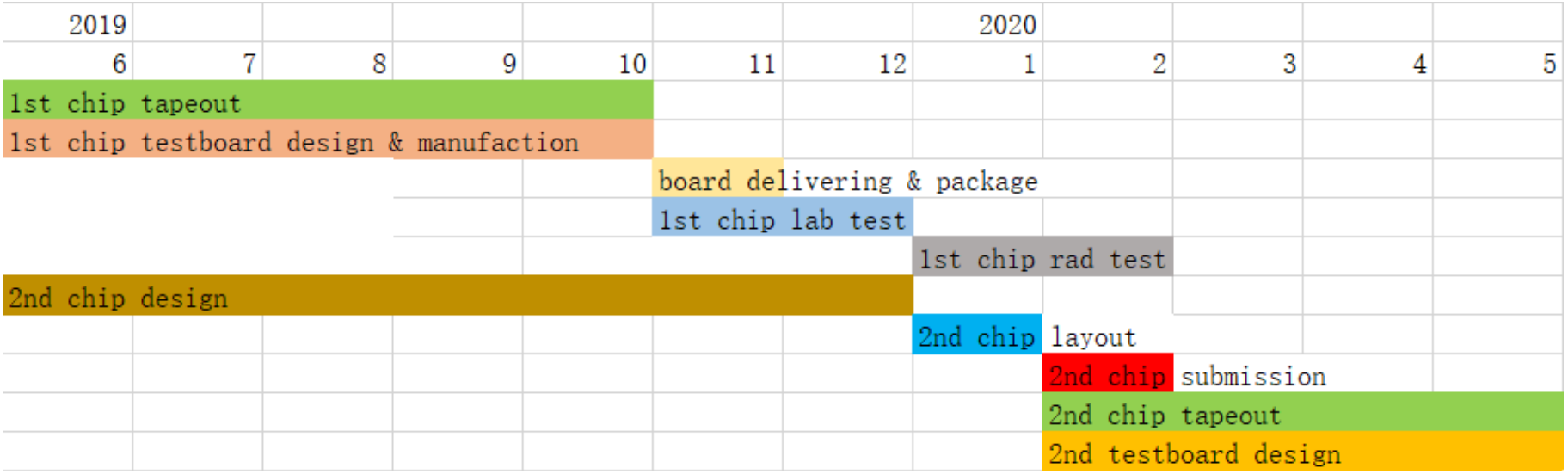
Recent Schedule

- **MOST2 Mid-term review in April 2020**
  - **First MPW test report (✔)**
  - **Second MPW submission**
    - **To submit in the next shuttle in Feb. 10， 2020**
- **Proposed design and improvement in the 2nd MPW (TBD)**
  - **A fully integrated, fully functional chip, all blocks included**
  - **Necessary improvement for the timing**
  - **Shrunk area of the periphery logic with improved power consumption**
  - **New ideas to implement chip-to-chip interconnections**
    - **In order to save the routing space in the Flex Cable**
  - **To improve the testability**
  - **Possible new scheme of SuperPixel architecture to shrink the pixel size**
  - **The matrix will be likely to keep in the same dimension of 64*192**

Schedule delayed due to the long turnaround of TJ



Proposal for the schedule of the next version



- **Goals for this year (modified):**
  - **submit the 2nd MPW prototype before the midterm review**
  - **Deadline: 2020. 5**
- **Estimated date for the 2nd MPW tapeout:**
  - **2019.12.31 -> 2020. Feb. 10**
- **Potential problems**
  - **The design of 2nd MPW will start in parallel and without the test results from 1st MPW**

Thank you !

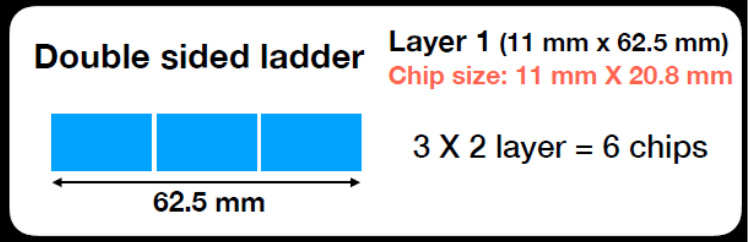
Ladder Prototype

Silicon Vertex Detector Prototype – MOST (2018–2023)

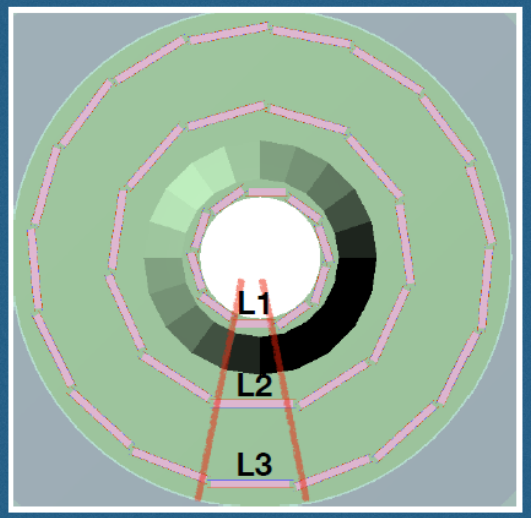
Sensor technology CMOS TowerJazz

- Design sensor with large area and high resolution
- Integration of front-end electronic on sensor chip

Benefit from MOST 1 research program



3-layer sector



Baseline MOST2 goal:
3-layer prototype

Default layout requires different size ladders

Keep it simple for baseline design

L1
L2
L3

3-layers
same size
same chip

Goals:
1 MRad TID
3-5μm SP resolution

Integrate electronics readout

Design and produce light and rigid support structures

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- Ref: Introduction to the Pixel MOST2 Project, Joao Costa, 2018.6

Team organization

- Slides from Y. Zhang, Satellite meeting of MOST2 in Oxford, 2019.4

- **Design team:**
  - **IHEP, SDU, NWPU, IFAE & CCNU**
  - **Biweekly/weekly video design meeting on chip design (convened by IHEP)**

Institutes	Tasks	Designers
IHEP	Full chip modeling & simulation Pixel Analog, TCAD simulation High speed interface: PLL + Serializer	Wei Wei, Ying Zhang Xiaoting Li, Weiguo Lu, Mei Zhao
CCNU/IFAE	Pixel Digital	Tianya Wu, Raimon Casanova
NWPU	Periphery Logic, LDO	Xiaomin Wei, Jia Wang
SDU	Bias generation	Liang Zhang

- **Chip characterization**
  - **Test system development: SDU & + other interested parties**
  - **Electrical test: all designers supposed to be involved in the related module + other interested parties**
  - **Irradiation test: X-ray irradiator + beam line**