Status of the JadePix3 chip

Yunpeng Lu

On behalf of the JadePix3 design team

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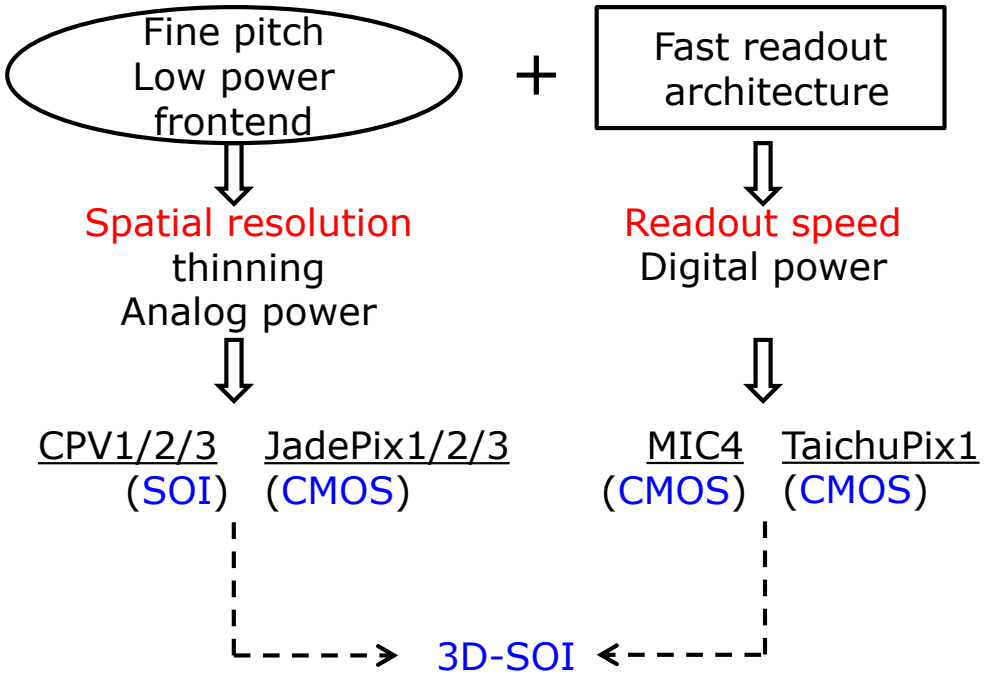
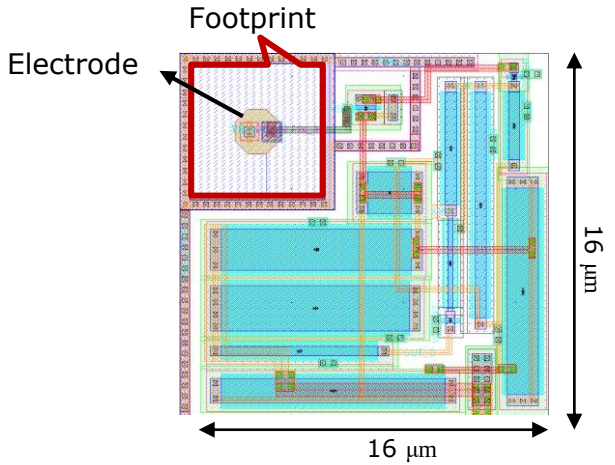
R&D activities on pixel sensors

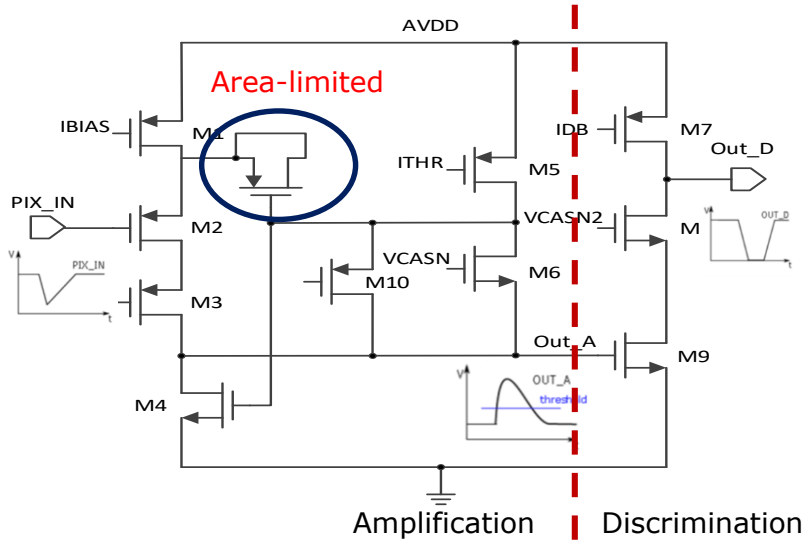
- Step 1: optimized separately either for spatial resolution or for readout speed;
  - CPV1/2/3 and JadePix1/2/3
  - MIC4 and TaichuPix1
- Step 2: combine the two parts with advanced technologies
  - 3D-SOI is being pursuing

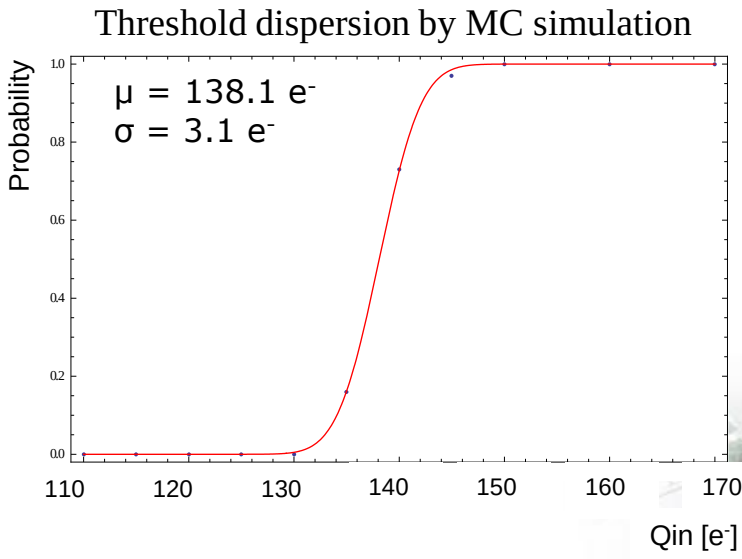


JadePix3: Diode & Front-end design

- Design goals: small pixel size and low power consumption
- Sensing diode: negatively biased for high Q/C
  - Electrode size 4 μm², with a small footprint 36 μm²
- Frontend: tradeoff between FPN and layout area
  - Improvement on the FPN = 3.1e⁻ (simulation)
  - Reduction on the layout area, ~200 μm²
  - A low power version (20nA), equivalent to 9 mW/cm²

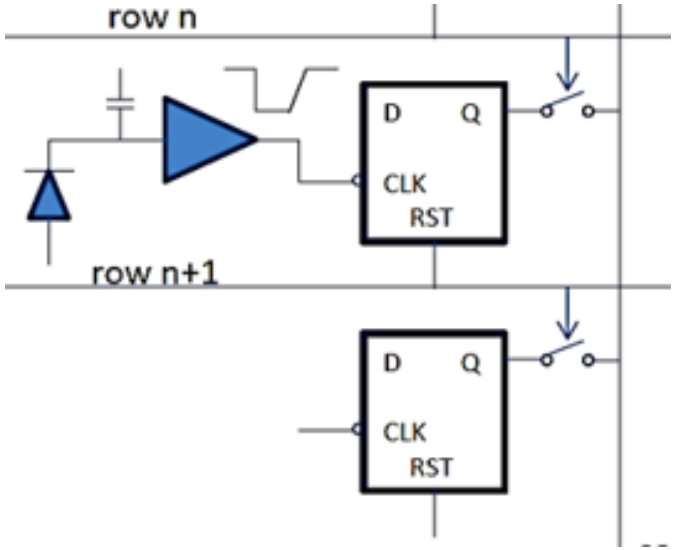


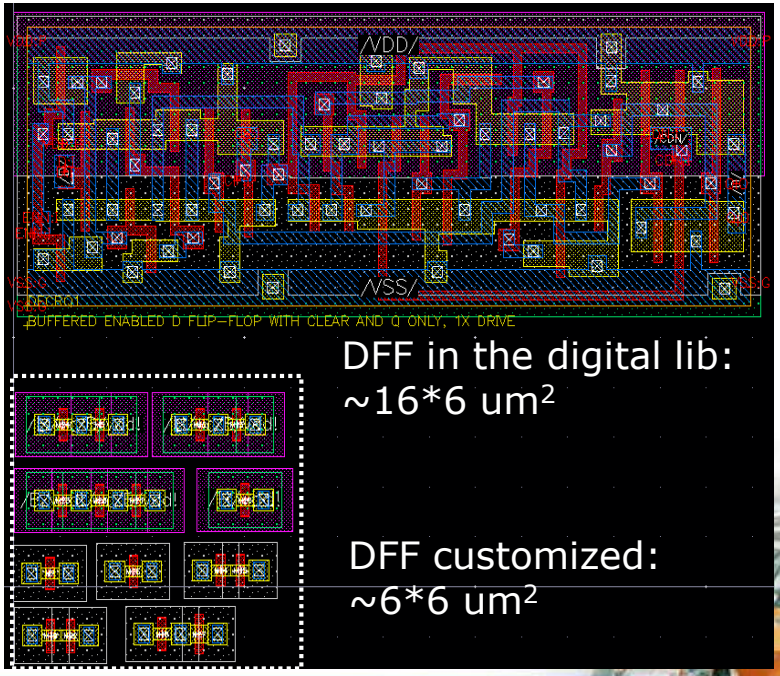




JadePix3: Customized D-FlipFlop

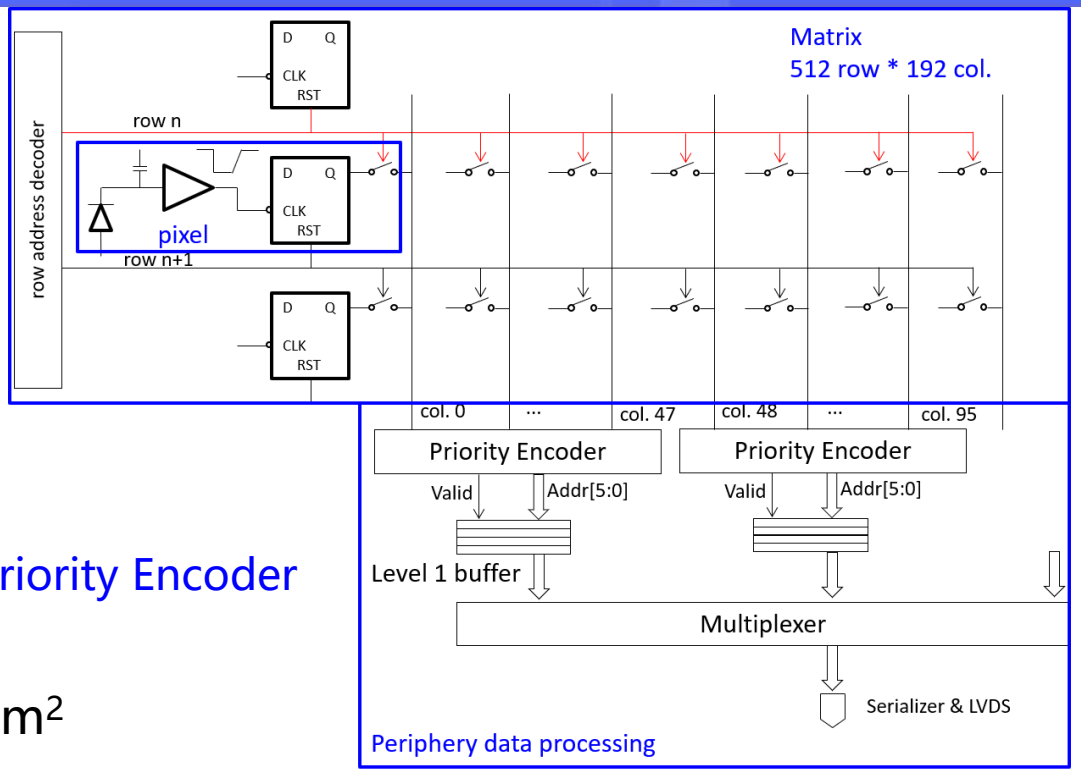
- D-FlipFlop (DFF) used to register the ‘Hit’ from the discriminator
  - Set to 1 by the leading (falling) edge of discriminated pulse
  - Reset to 0 by the shared row line
  - Enhanced to drive the column line (capacitive)
  - Customized design to reduce the layout area



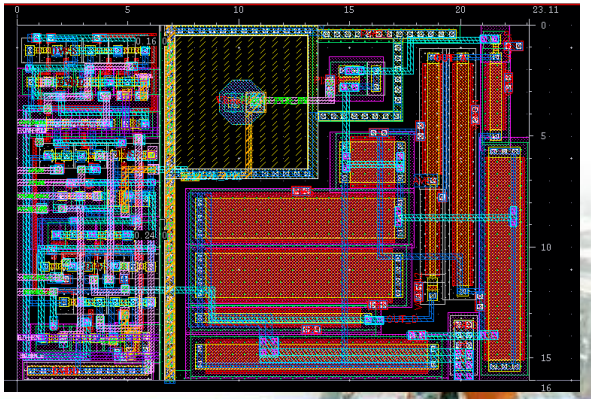


JadePix3: Rolling shutter readout of matrix

- In-pixel circuit
  - Low power binary front-end
  - Optimized DFF
- Rolling shutter readout
  - 512 row * 192 col.
  - One row selected at a time
  - 102 us to finish 512 rows
  - Every 48 columns fed into the Priority Encoder at the end of columns.
- Minimum pixel size 16× 23.11 μm²
  - 4 variants to investigate possible optimizations



Sector	Diode	Front-end	Pixel digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	16×26 μm²
1	2 + 2 μm	FE_V0	DGT_V1	16× 26 μm²
2	2 + 2 μm	FE_V0	DGT_V2	16× 23.11 μm²
3	2 + 2 μm	FE_V1	DGT_V0	16×26 μm²

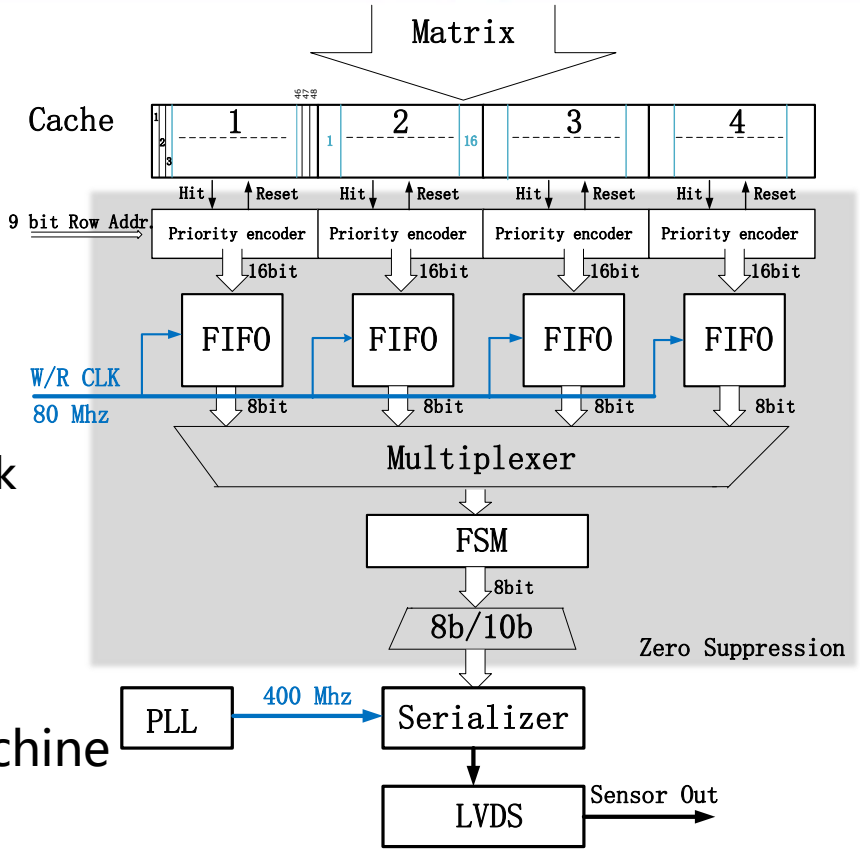


JadePix3: Periphery data processing

- Zero suppression at the end of column
  - Each 48 columns divided into 16 blocks
  - ‘Fired’ blocks identified sequentially by a 4-bit priority encoder
  - 12.5 ns * 16 blocks = 200 ns/row
- Only hit information fed into FIFO

Row #	Block #	hits in block
9-bit	4-bit	3-bit

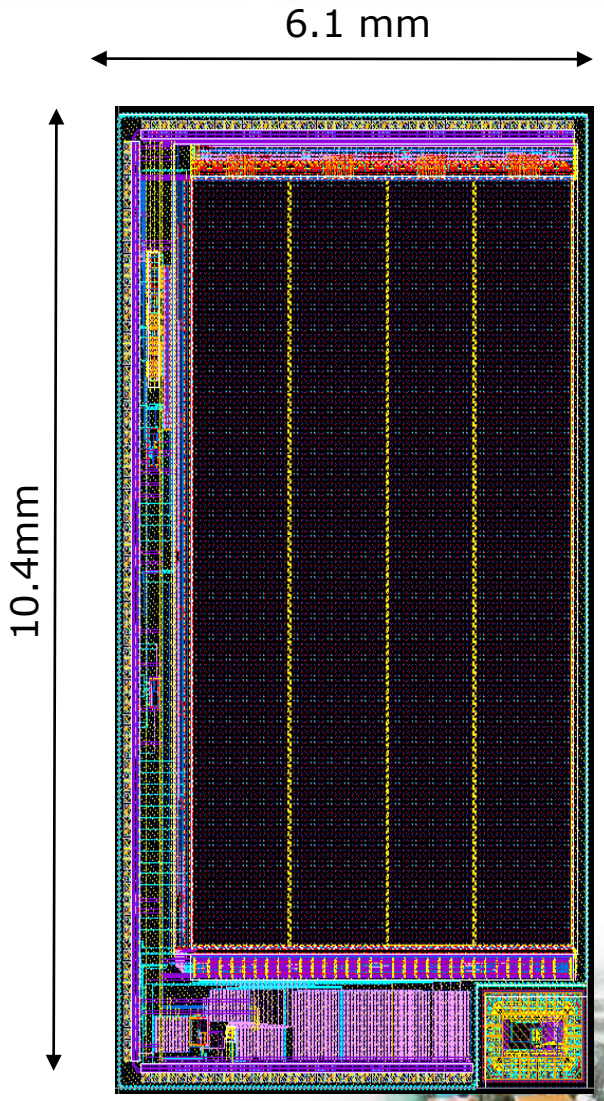
  - FIFO R/W clk: 80 MHz
  - FIFO depth: 48
- Data stream steered by a Finite State Machine
- Data after 8b/10b: 800 Mbit/s
- Estimated Power consumption 60mW
  - 15mW (Zero suppression), 25mW (Serializer), 20mW (PLL)



JadePix3: Status

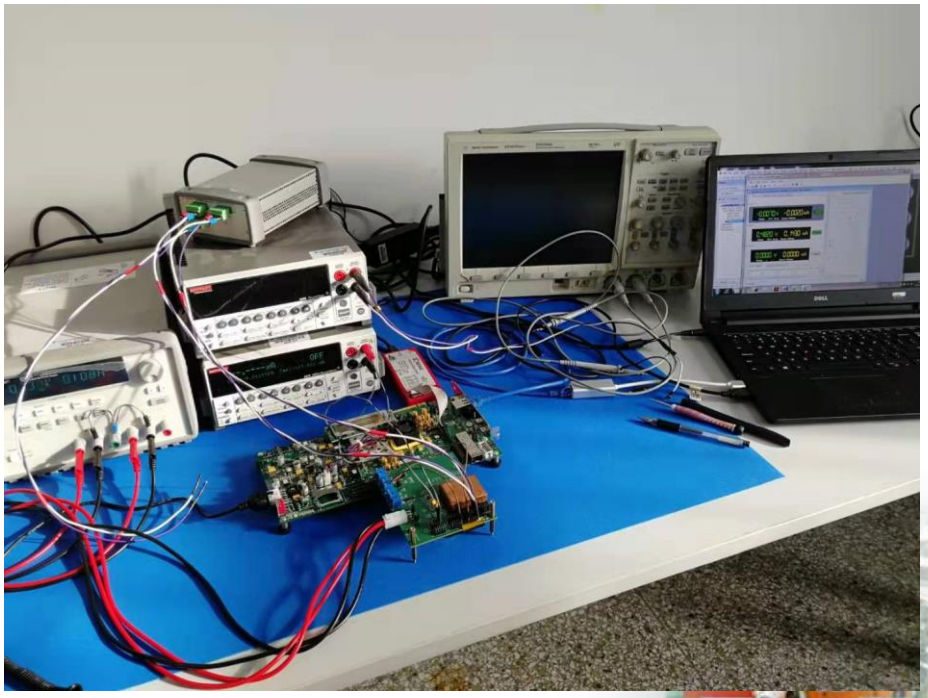
- Submitted in Oct. 2019
  - 10.4mm * 6.1 mm
- Minimum pixel size 16× 23.11 μm^2
  - Rolling shutter readout 102 us/frame
- Estimated power consumption ~ 51 mW/cm^2
  - 9mW/cm^2 (Pixel)
  - 30mW/cm^2 (Zero suppression)
  - 6.25mW/cm^2 (Serializer)
  - 5mW/cm^2 (PLL)

} If shared by 1 * 2 cm^2 chip



Test System

- Based on a common FPGA development kit, KC705
  - Being used in the SOI/CPV3 test
- Preparation for the Jadepix3 test
  - Custom sub-board
  - FPGA firmware to be adapted to the JadePix3 interface
  - DAQ Software can be reused



Summary

- High resolution low power CMOS sensor is in development for the CEPC vertex
  - Minimum pixel size 16× 23.11 μm^2
  - Estimated power consumption ~ 55 mW/cm^2
  - Rolling shutter readout 102 us/frame
- Test system based on the existing KC705 platform
  - Plan to start testing from June

JadePix3 design team

- IHEP: Yunpeng Lu, Ying Zhang, Yang Zhou, Zhigang Wu, Qun OuYang
- CCNU: Yang Ping, Weiping Ren, Le Xiao, Di Guo, Chenxing Meng, Anyang Xu, Xiangming Sun
- Dalian Minzu Unv: Zhan Shi
- SDU: Liang Zhang

Thank you for your time!