# Digital pixel verification for testing

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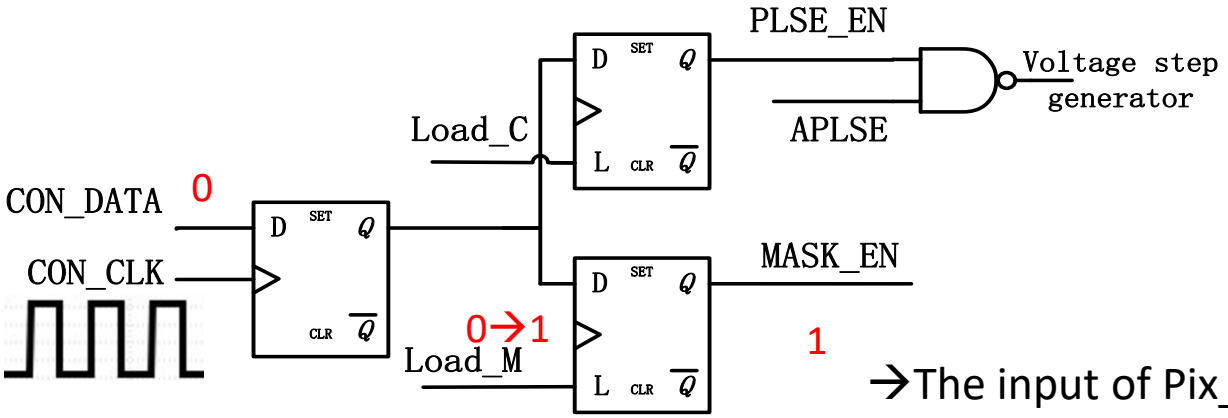
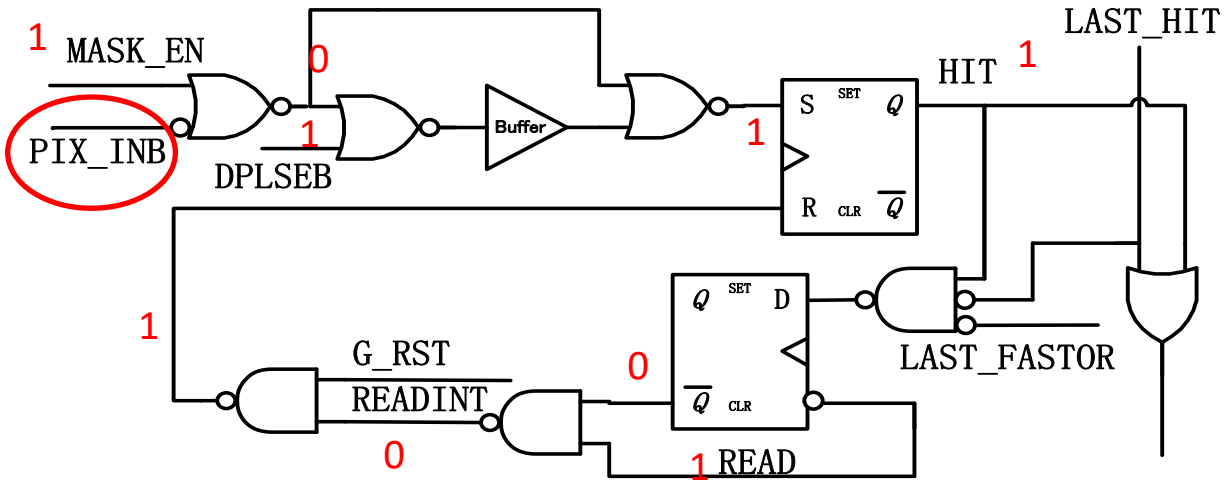
# OUTLINE

- Simulation of Digital Pulse test
- Simulation of MASK_EN
- Timing of next submission

# Principle of scheme1(FE-I3 like)



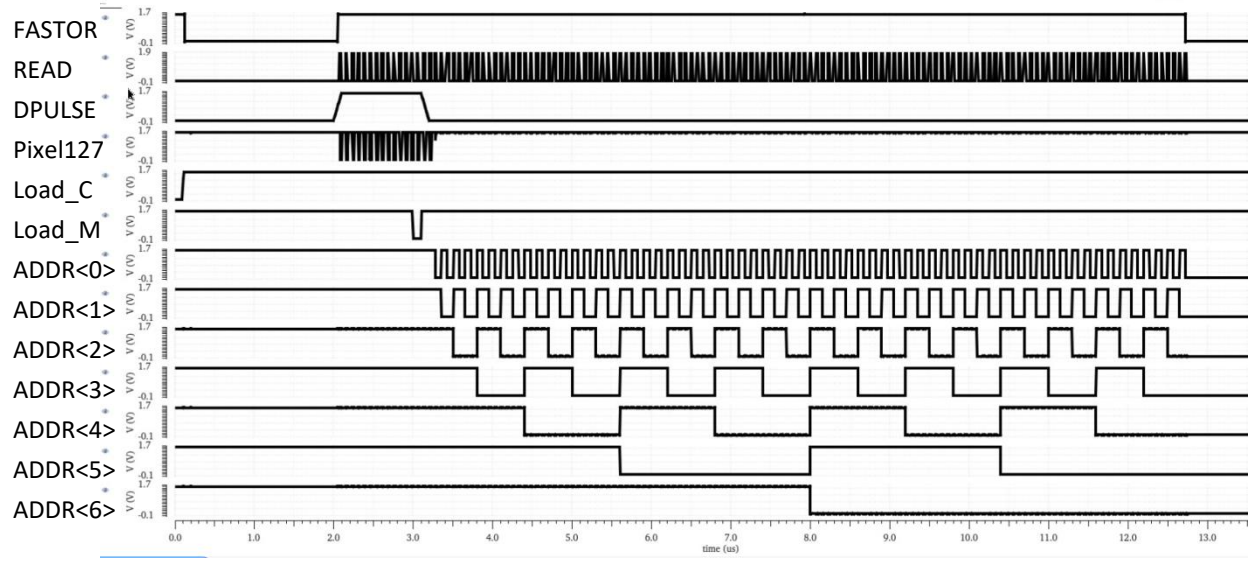

→The input of Pix_INB can't effect Dpulse, it can work all the time.



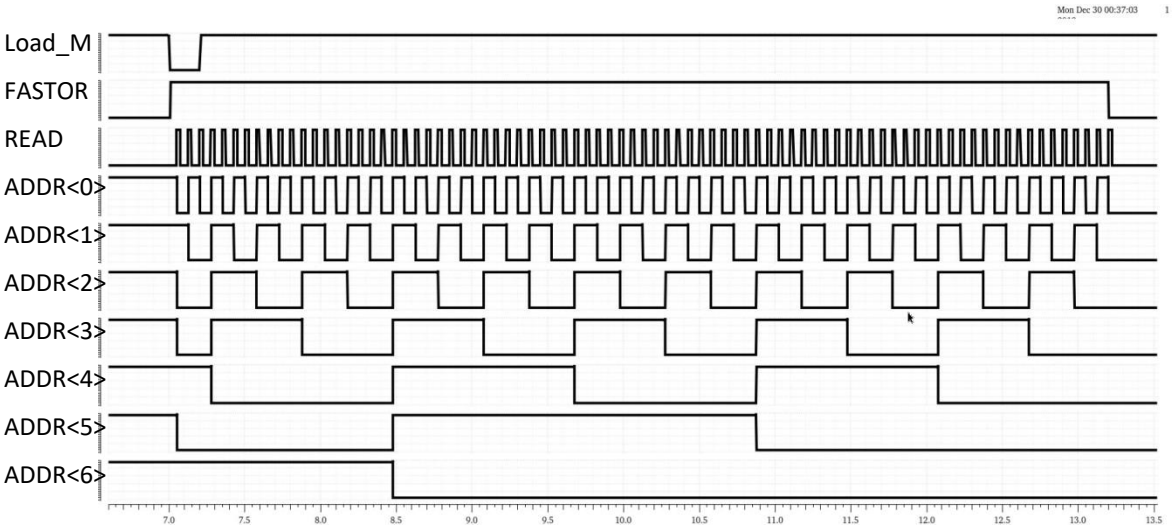

→If MASK_EN changes from 0→1,it will generate a pulse and record by the circuit.

# Simulation Results

For FE-I3 like scheme Dpulse simulation：




For FE-I3 like scheme MASK simulation：




→The simulation shows that there is something wrong when to mask all the signal.

→ The Pixel82 to Pixel0 will generate a pulse at the input PIN.

→ When the Power supply of the logics is 1.6V, the condition will be worse, it will start from pixel86.

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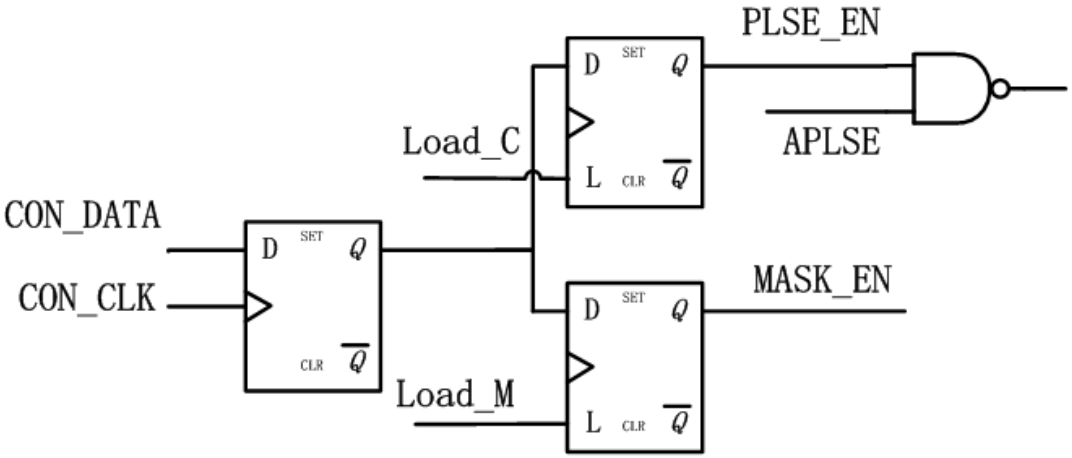
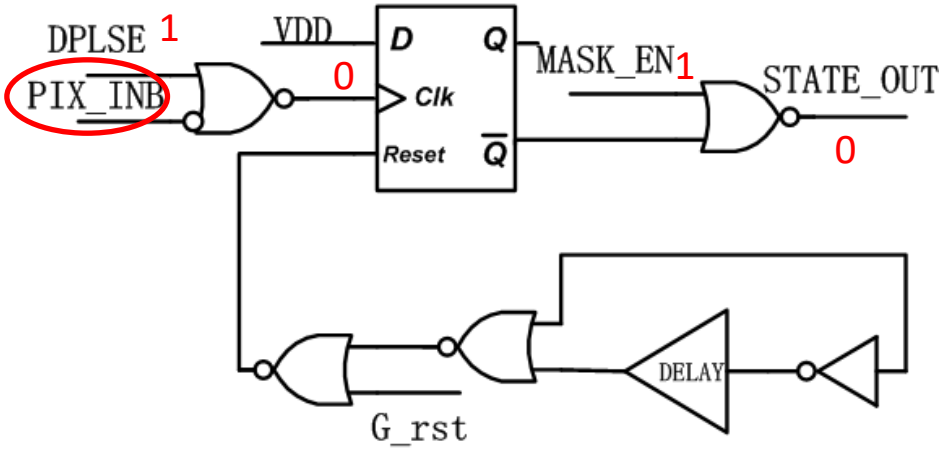
# Principle of scheme2(ALPIDE like)



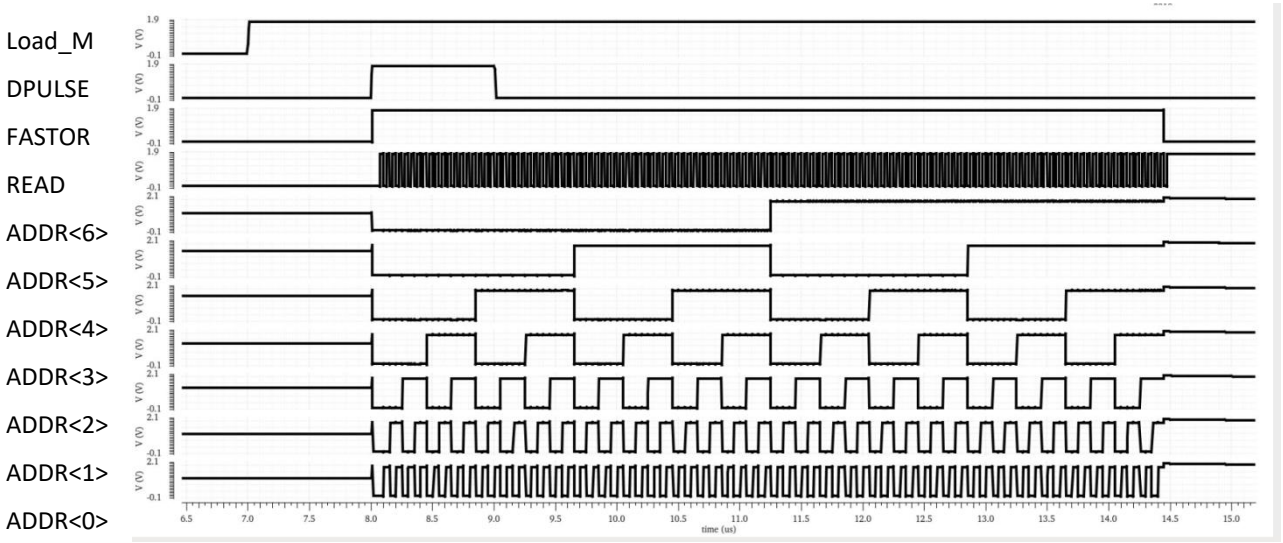

→The mask and calibration chain is the same with scheme1.

→ For the readout electronics, the Pix_INB must be 1 , so that the DPLSE can function properly.

→ The MASK_EN will mask total pixel.

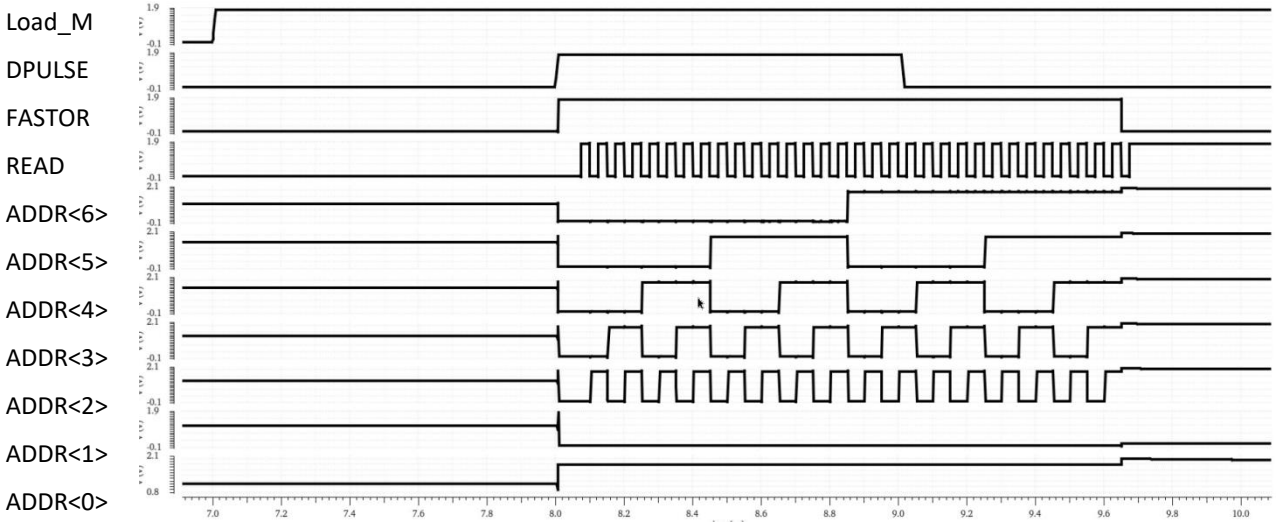
# Simulation Results

For ALPIDE scheme Dpulse simulation：




→The simulation shows that everything is fine with the digital injection pulse and mask the pixels.

For ALPIDE scheme MASK simulation：



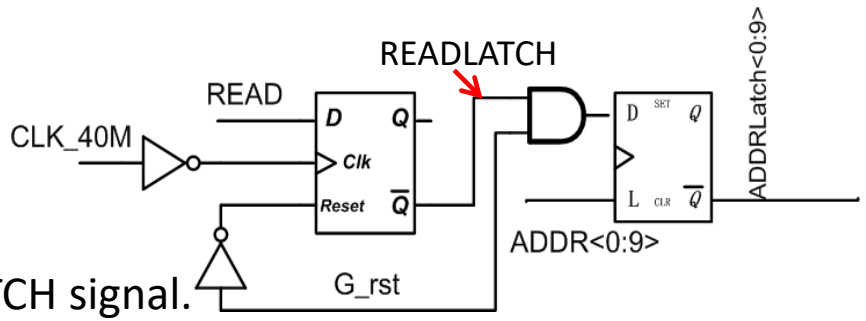

→ The bottom figure show the result of ¾ pixels masking, only ¼ pixels can be readout.

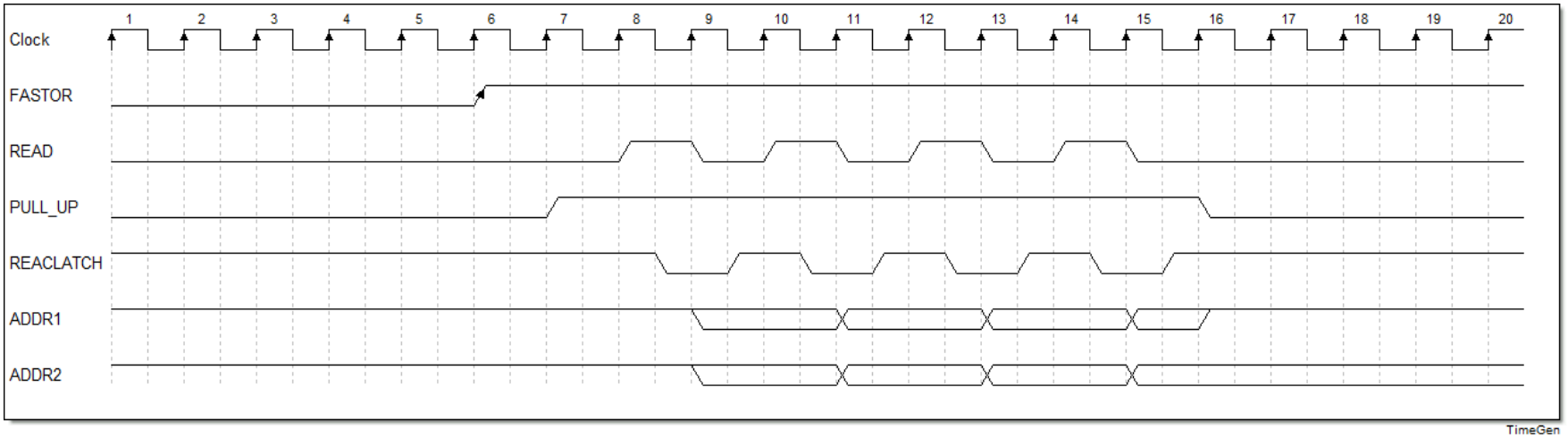
# Timing for data latch

→From the discussion with Ms Wei, it is not so safe to latch the data at the negative half cycle of READ?

→ The main idea of the schematic is to generate a inversing READ and delay a half cycle with DFF.

→ The ADDR data will be latched with the READLATCH signal.



# Thanks for your attention.