The 2020 international Workshop on the High Energy Circular Electron-Positron Collider (CEPC), 26 - 28 October 2020, Shanghai, China

OVERVIEW OF CEPC SILICON DETECTORS

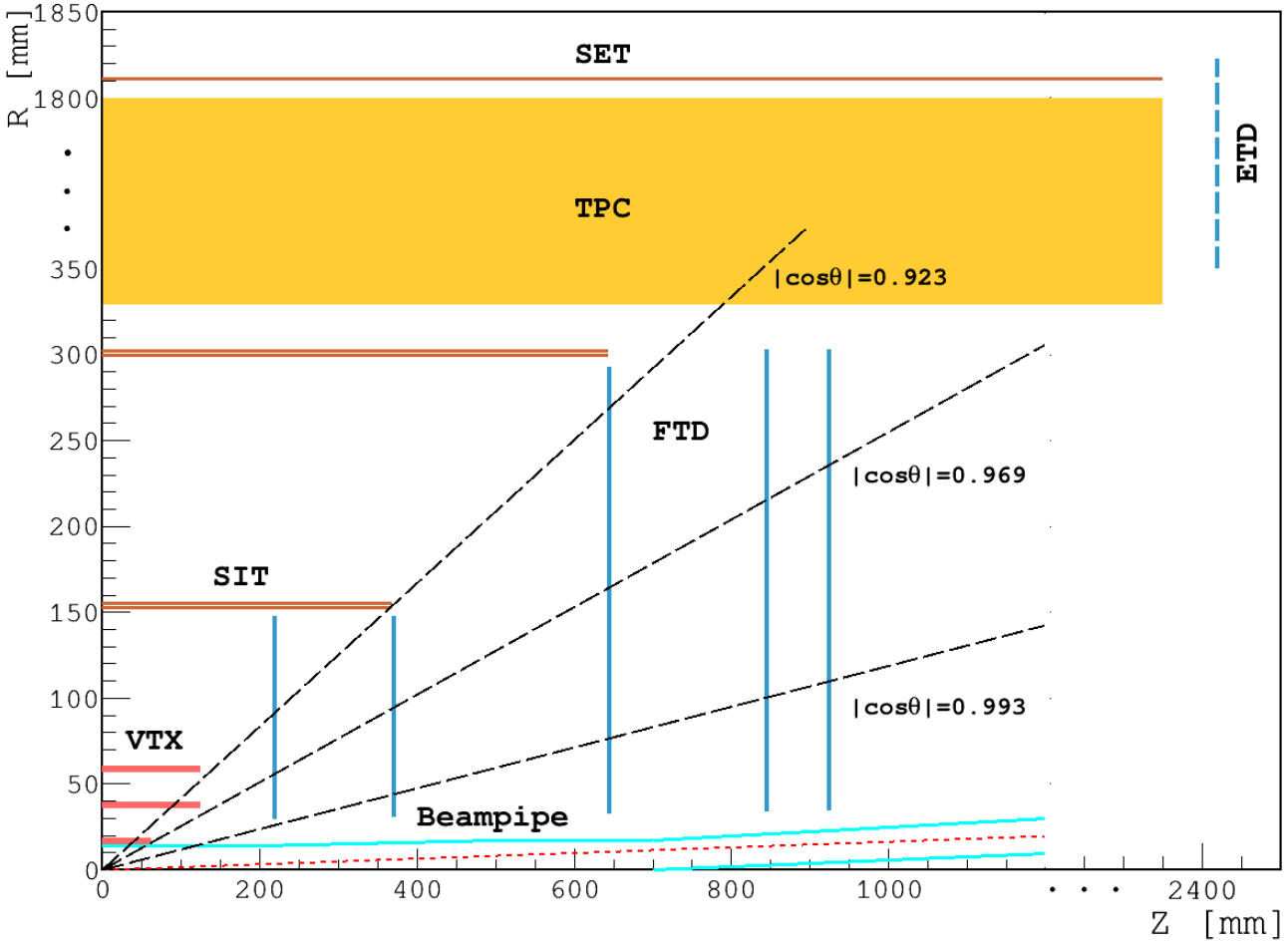
Hongbo Zhu (IHEP)

On behalf of the CEPC Study Group

OUTLINE

- CEPC tracker layout and requirement
- Vertex detector design and R&D
- Silicon tracker design and R&D
- Summary

BASELINE TRACKER LAYOUT



- Time Projection Chamber (TPC) +“Silicon Envelope” adopted from ILD

VERTEX DETECTOR REQUIREMENTS

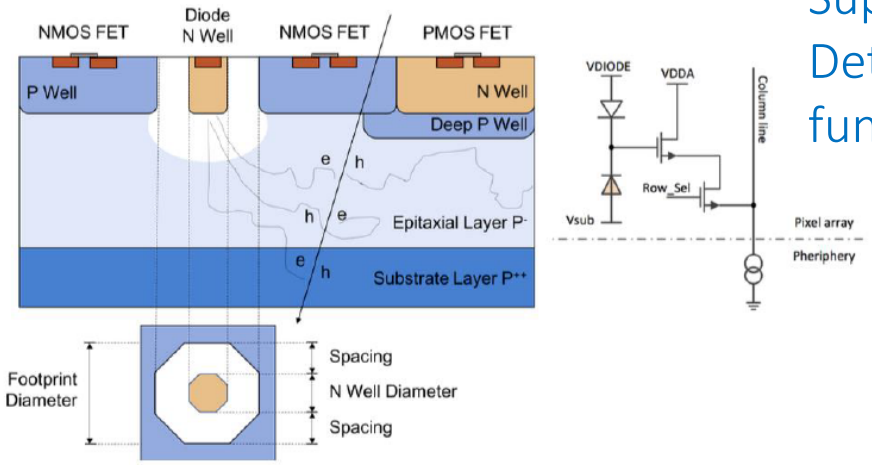
- High precision vertex detector essential for the heavy-flavor and τ-lepton identification; designed to achieve

$$\sigma_{r\varphi} = 5\ \mu m \oplus \frac{10\ \mu m}{p(\mathrm{GeV}) \cdot \sin^{3/2}\theta}$$

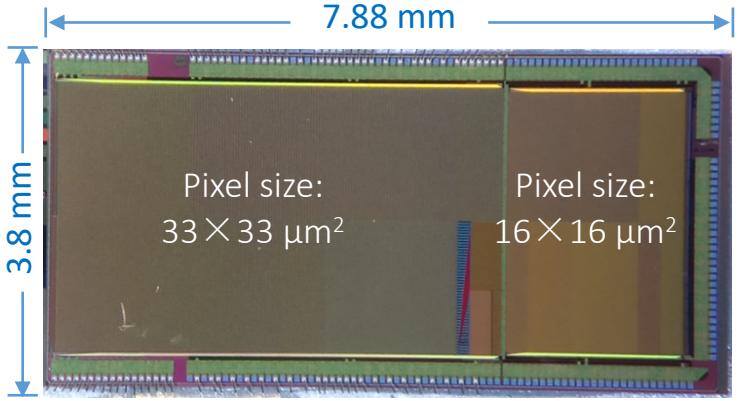
- With the baseline design, this implies:
  - Single point resolution < 3 μm → small pixel pitch, e.g. 16 μm
  - Material budget 0.15%X_0 per layer→ thin & low power 50 mW/cm^2
  - Detector occupancy below 0.5% → small pixel & fast readout
  - Radiation tolerance **(per year):** 1 MRad &2×10^{12} 1 MeV n_{eq}/cm^2

JadePix-1 Pixel Design

- 1st prototype sensor developed with TJ 0.18 µm CIS process
- Design goal: diode geometry optimization



Supported by the State Key Lab of Particle Detection and Electronics & IHEP Innovation fund, **with lots of helps from IPHC**

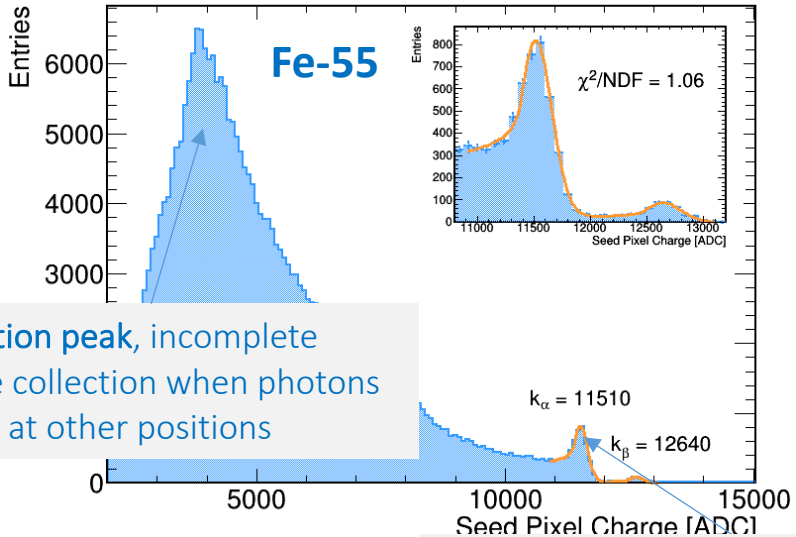


Impacts of electrode size and footprint on charge collection performance

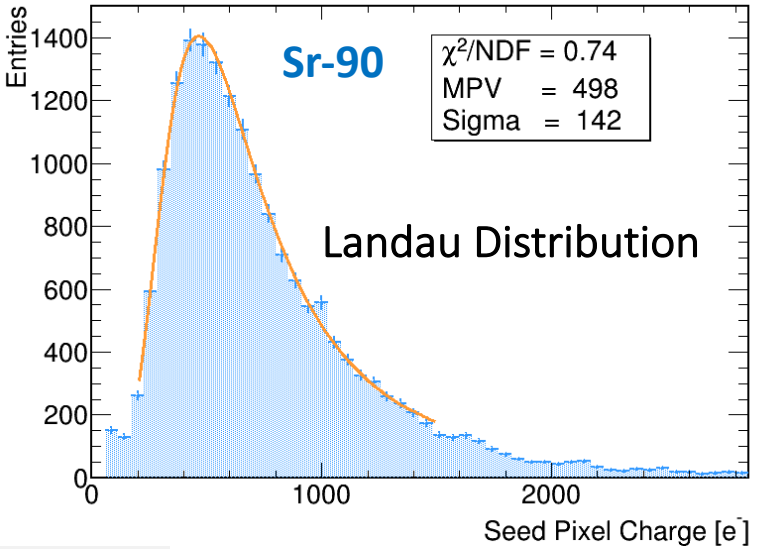
- Submission in November 2015, test system developed and verified in 2016; detailed performance characterization in 2017& 2018

CHARACTERIZATION WITH RADIOACTIVE SOURCE

- Fe-55: Low energy X-ray photons (5.9 keV) for calibration



Collection peak, incomplete charge collection when photons hitting at other positions

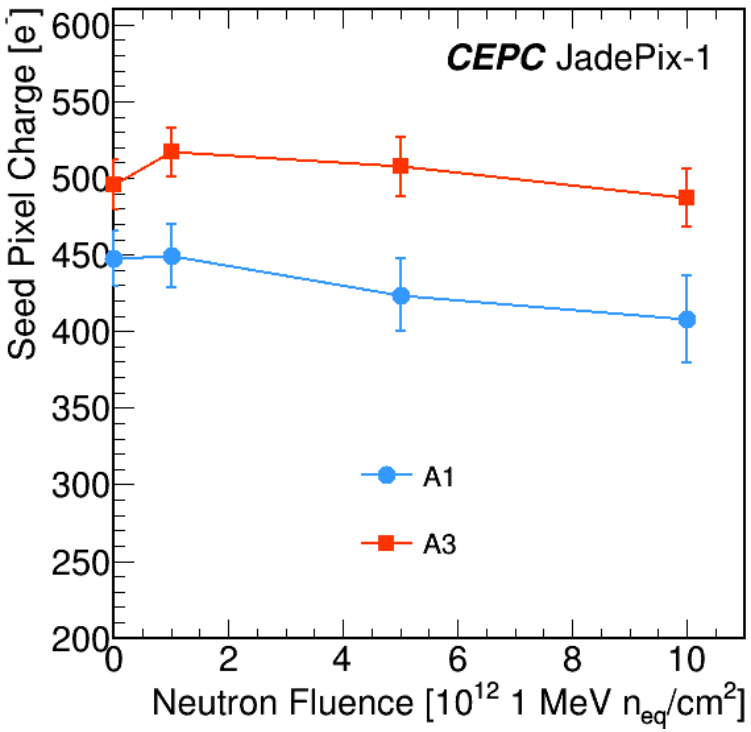


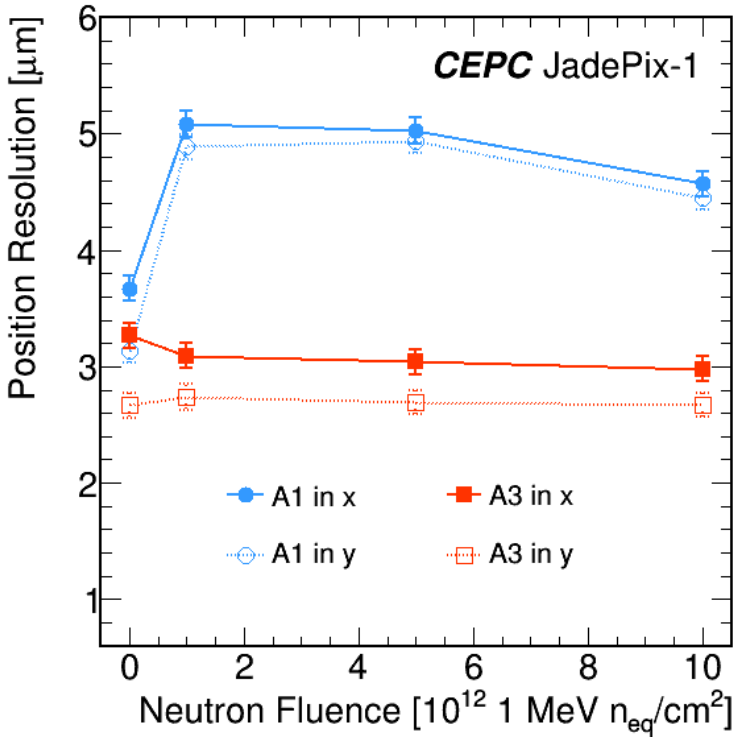
Calibration peak, X-ray photons hitting the electrode area and generated charge nearly 100% collected

- Sr-90: MIP-like electrons for charge collection performance
- Small electrode and large footprint preferred to achieve high Q/C ratio → reduction in analog power consumption

TEST BEAM MEASUREMENTS

- Prototype samples irradiated up to 10^{13} n_{eq}/cm^2 with neutrons and tested at the DESY test beam facility

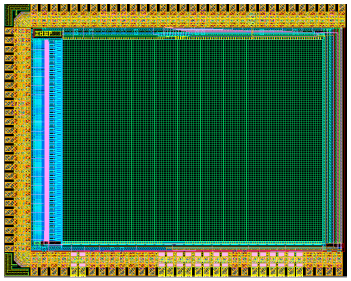




JADEPIX-2/3

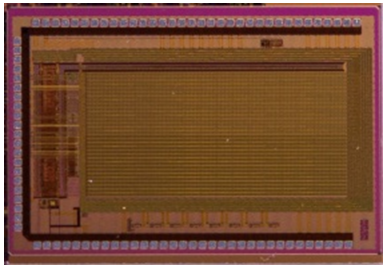
Funded by MOST 1

	Pixel size (μm²)	In-pixel Circuit	R/O Architecture
JadePix2	22 × 22	Amplification, discriminator, binary output	Rolling shutter
MIC4	25 × 25	Low power front-end, address encoder	Data-driven, Asynchronous
JadePix3	16 × 26 16 × 23.11	Low power front-end, binary output	Rolling shutter with end of col. priority encoder



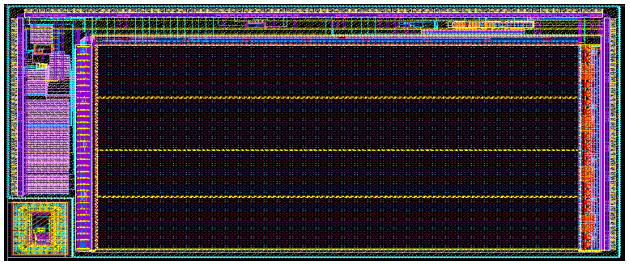
JadePix2 (IHEP)

3×3.3 mm²



MIC4 (CCNU & IHEP)

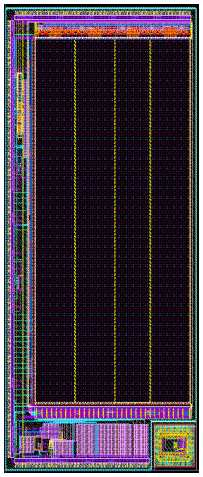
3.1×4.6 mm²



JadePix3 (IHEP, CCNU, DMU, SDU)

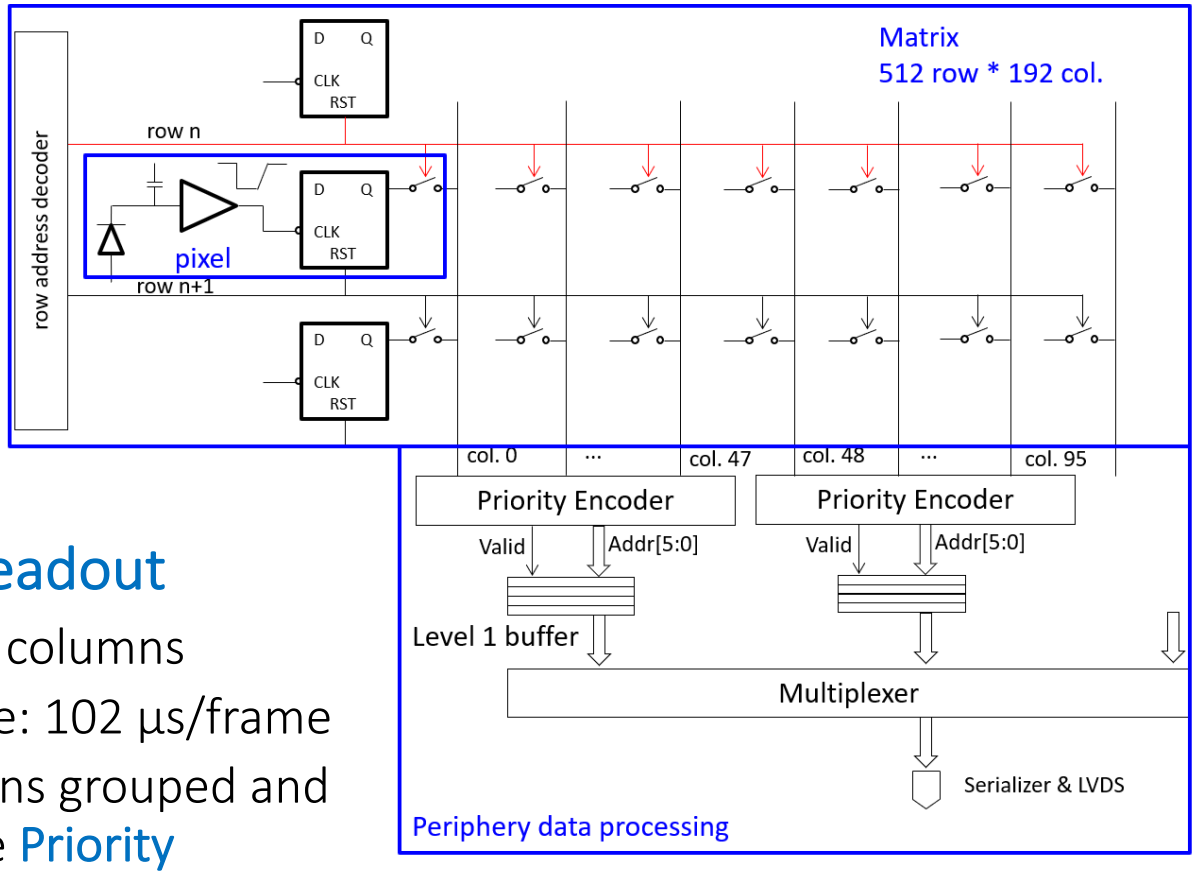
10.4×6.1 mm²

JADEPIX-3 DESIGN



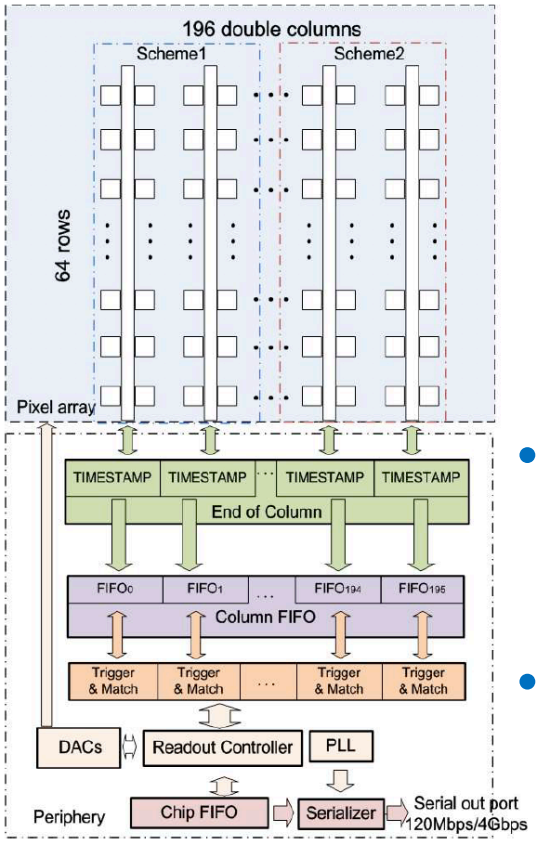
Chip under test

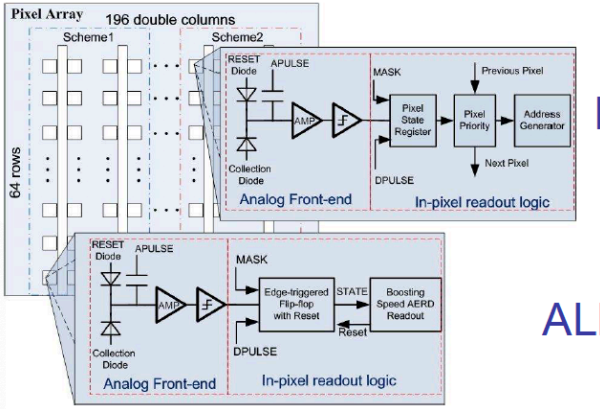
Small pixel: Low power FE + Rolling shutter Readout



- Rolling shutter readout
  - 512 row ×192 columns
  - Integration time: 102 μs/frame
  - Every 48 columns grouped and written into the Priority Encoder at the end of columns

TAICHUPIX



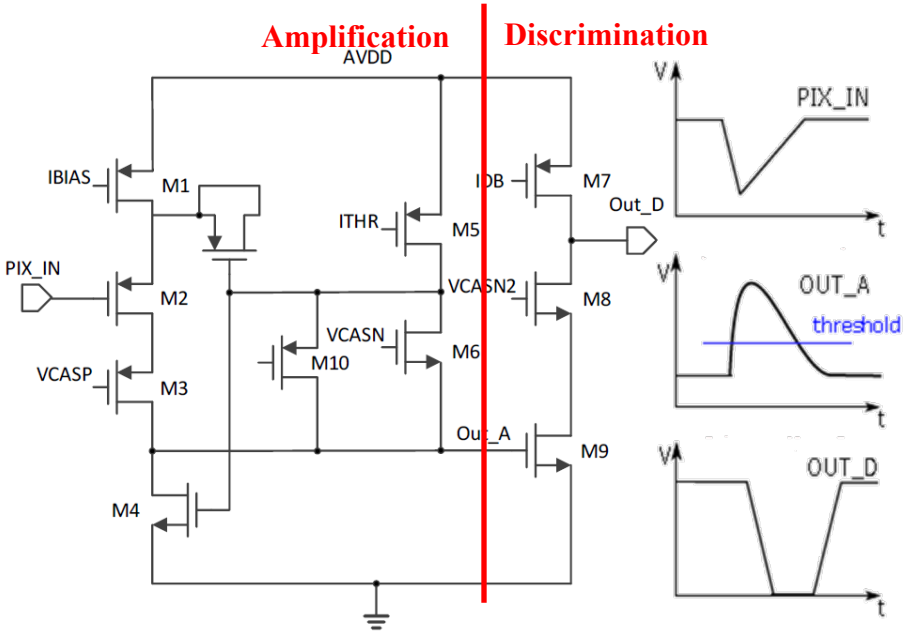


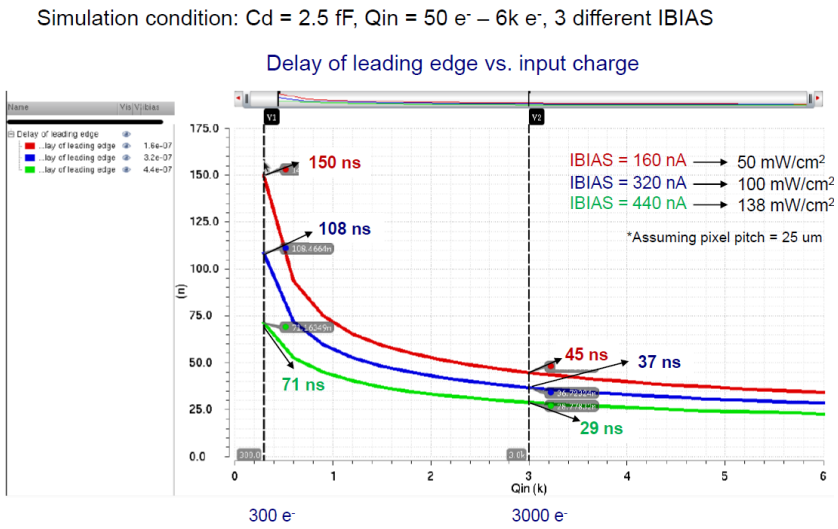
FE-I3-like Pixel

ALPIDE-like Pixel

- Column-drain readout
  - Priority based data driven readout; time stamp at EOC
  - Dead time: 2 CLK for each pixel (50ns @40MHz CLK)
- 2-level FIFO architecture
  - L1: column level, to de-randomize injection charge
  - L2: chip level, to match in/out data rate between core and interface
- Trigger readout:
  - Coincidence by time stamp, matched event read out

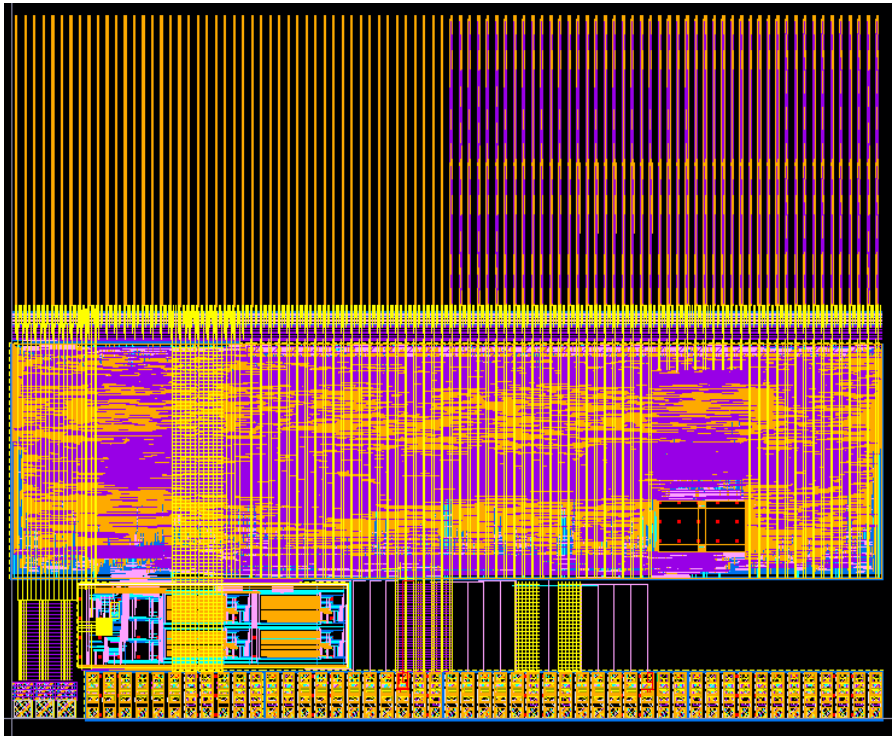
IN-PIXEL ELECTRONICS

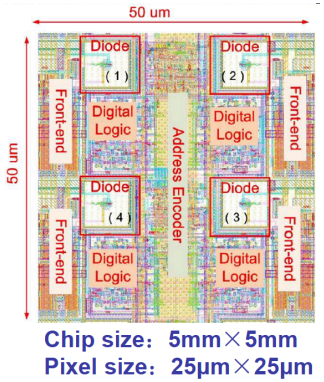


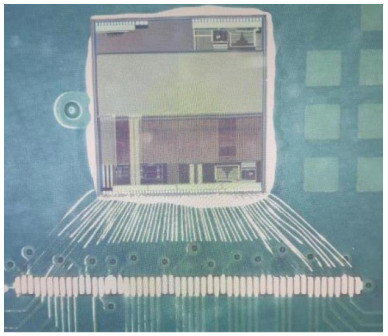


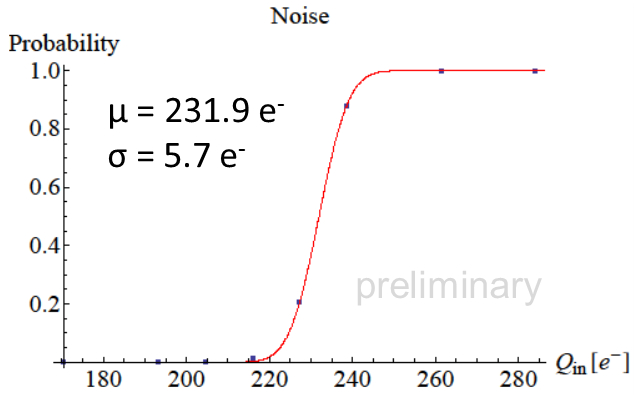
- Analog design derived from ALPIDE (structure tested in the MIC4 design)
- Biasing current increased for short peaking time of ~25 ns
  - Increased power consumption
  - Waiting for modified TJ process to achieve fast charge collection
- Digital-in-Pixel scheme: in pixel discrimination & register

TAICHUPIX-1



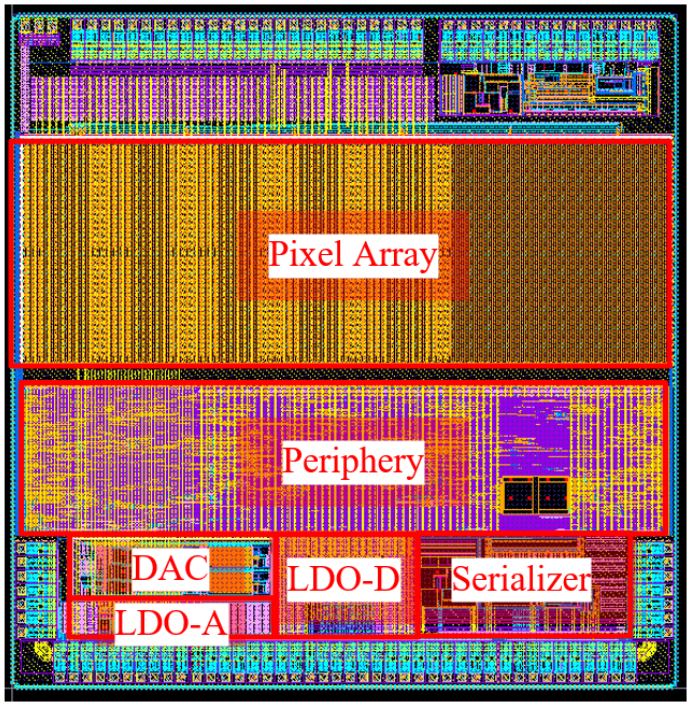


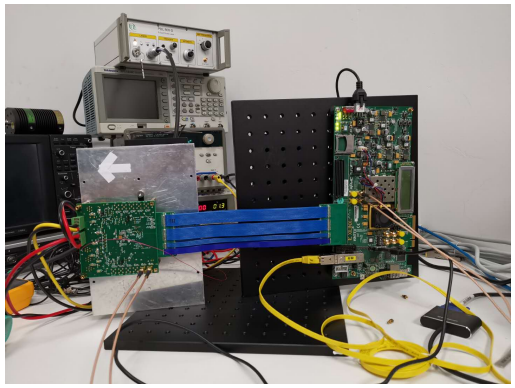




- 64×192 Pixel array + Periphery + PLL + Serializer
- Pixel digital functionality partially approved, bugs identified
- Measured noise: 5.7 e^-, time walk: 36 ns@300 ~1.5 ke^-

TaichuPix-2





- 64×192 pixel array with the same dimension as TaichuPix-1
  - 32 double column modified FE-I3 readout, 32 modified ALPIDE readout
  - 6 variations of pixel analog design, each with 16 columns
- New features added to TaichuPix-2
  - Two LDOs for power supplies
  - 8b10b encoder added for Triggerless output and balanced data stream
  - X-chip buses added for multiple chip interconnections
- Test status: functional verification completed (I/O, bandgap, PPL …), more detailed tests on-going

SOI Pixel Sensors

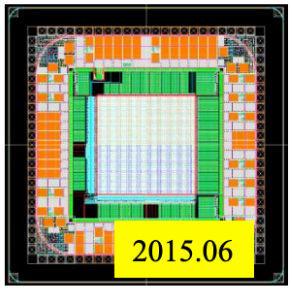
LAPIS 200nm Pinned Depleted Diode process

Prototypes in LAPIS 200nm Double-SOI process

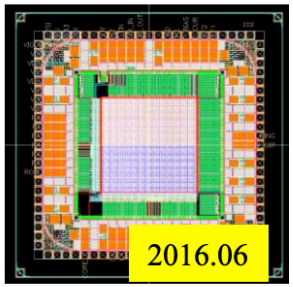
- 16μm *16μm with in-pixel discrimination
- Double-SOI process for shielding and radiation enhancement

- Thinned down to 75μm thick
- Temporal noise ~6e$^-$
- Threshold dispersion (FPN) ~114e$^-$
- Single point resolution ~2.3μm measurement under infrared laser beam

- Dedicated bias scheme to minimize capacitance
- Optimized for low FPN 12e$^-$
- Pixel matrix divided as 45 regions, to verify design options



CPV1 (IHEP)
3 ×3 mm^2



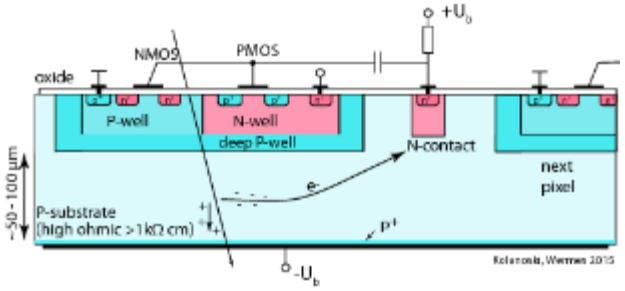
CPV2 (IHEP) 3 × 3 mm^2
NIMA 924(2019) 409-416

CPV3 (IHEP)
6 × 6 mm^2

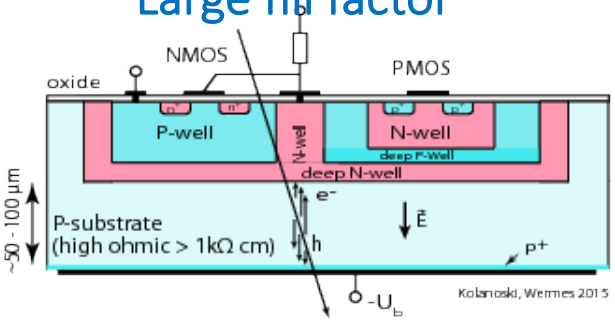
SILICON TRACKER

- Large tracking area to be covered with silicon sensors
- Not intended to start sensor design from scratch → limited R&D time and no need to re-invent the wheel
- CMOS pixel sensors proposed for the ATLAS outer most pixel layer (and strip) but not matured enough for construction → continuing efforts for the CEPC tracker

Small fill factor



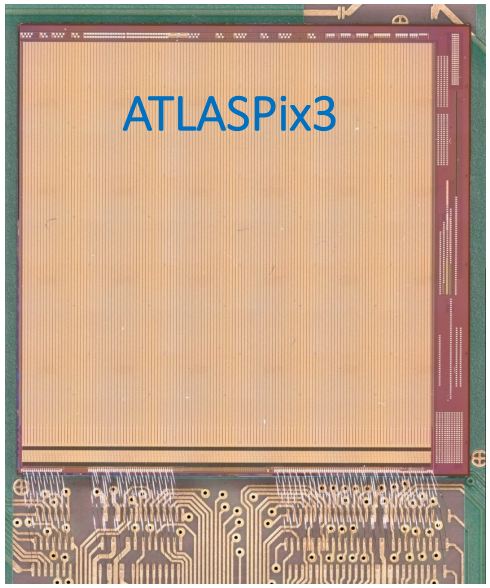
Large fill factor



More details in Ivan Peric's talk

ATLASPIX3

- Depleted CMOS sensor
  - Fully integrated readout
  - Fast charge collection
  - Low material budget



Sensors and DAQ boards distributed to participating institutes

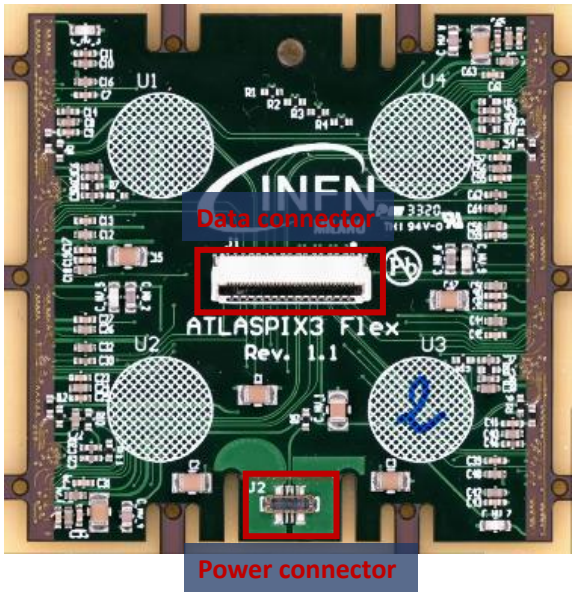
ATLASPIX3 FEATURES:

- Pixel size 50 × 150 μm^2
- Reticle size 20 × 21 mm^2
- TSI 180 nm HV process on 200 Ωcm substrate
- 132 columns × 372 rows
- Digital part of the matrix located on periphery
- Both triggerless and triggered readout possible
- **Up to 1.28 Gbps downlink**

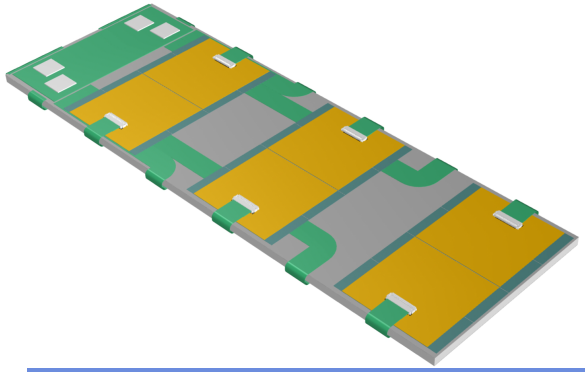
More details in Attilio's talk

DEMONSTRATOR (SHORT STAVE)

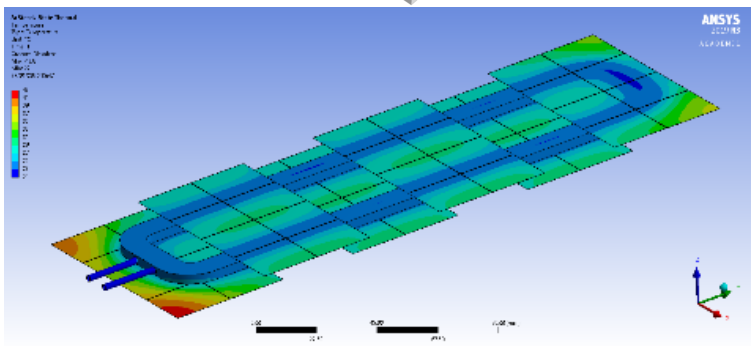
QuadModule Concept



- Multiple modules on light composite support
  - Alternate tile pattern for hermeticity
  - Aggregation of data/optical conversion at the end-of-stave; serial powering



- Readout unit based on 4 chips
  - Shared services among 4 sensors by common power connections and configuration lines
  - Benefits of in-chip regulators to reduce connections

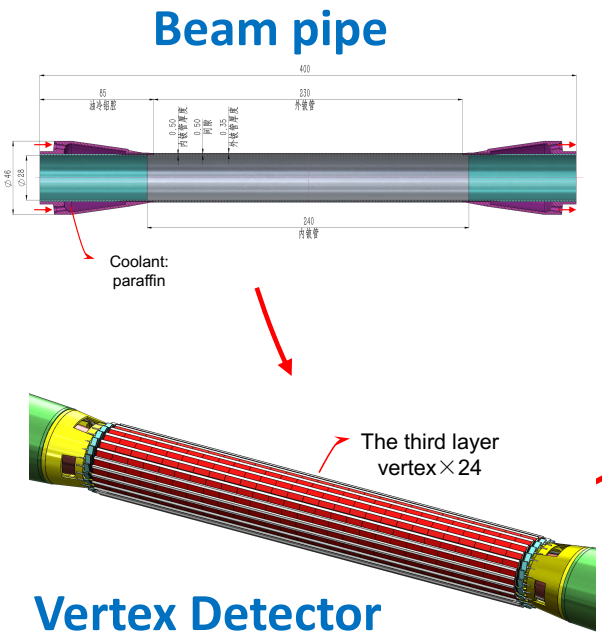


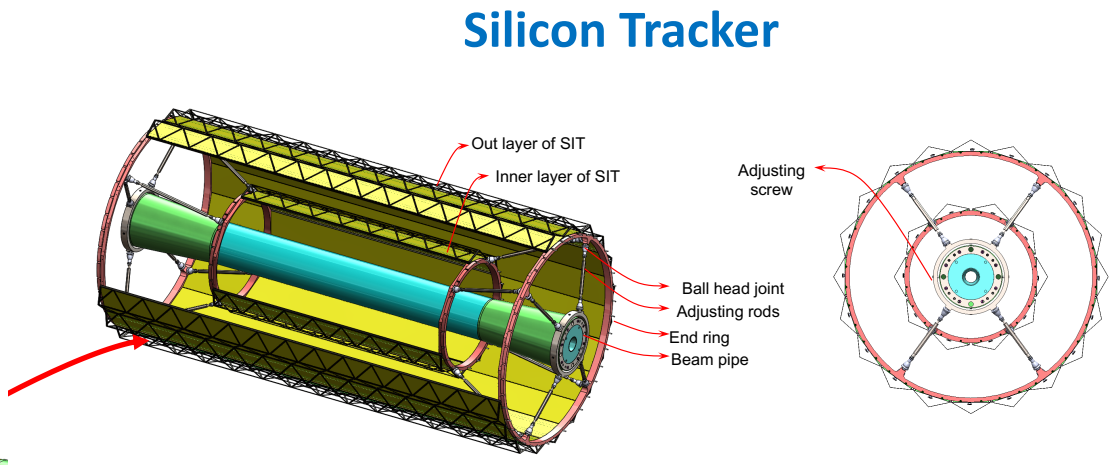
BEYOND THE DEMONSTRATOR

- Pixel sensor design optimization toward the requirements of the CEPC silicon tracker
  - Pixel size: 50×150 → 25×300
  - Lower power consumption: less demanding if active cooling applied
  - Powering scheme: serial powering to save material budget
  - Other functionalities to be discussed
  - Migrate the design to Chinese foundry
- Light weighted support structure (stave core)
  - Improved design inspired by ALICE/ATLAS truss structure, longer extension, higher rigidity and stability (challenging to align detector elements with less tracks)

System Design

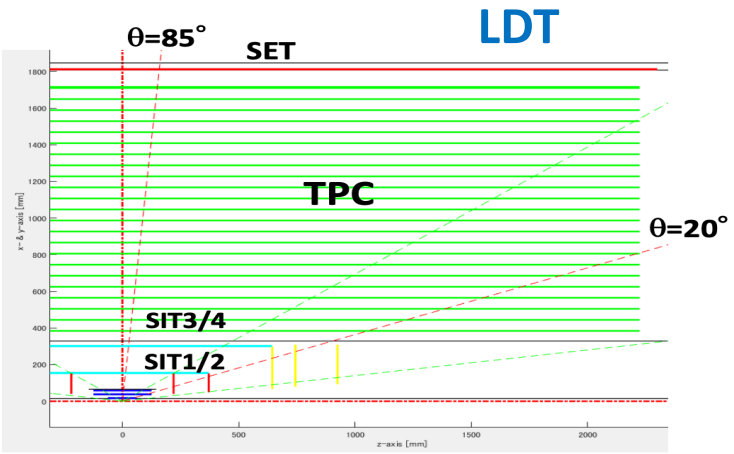
- System design (CDR baseline detector) started with the best knowledge and to be further optimized (interfacing between sub-detectors and integration scheme)

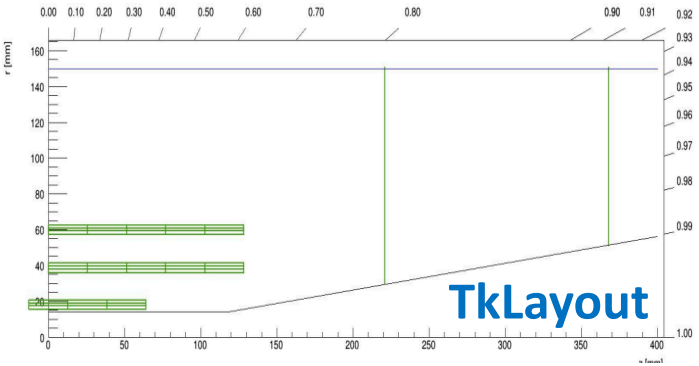


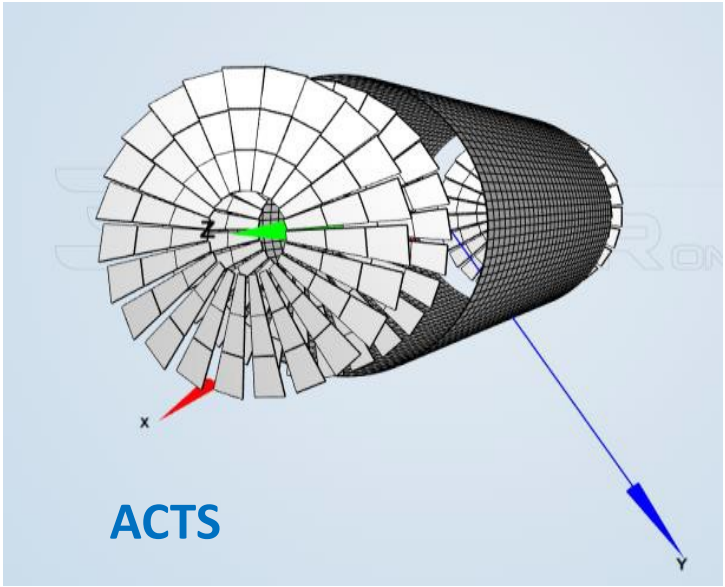


TRACKER LAYOUT RE-OPTIMIZATION

- **LDT** or **TkLayout** to validate basic tracking performance before implementing detailed geometry in **ACTS**





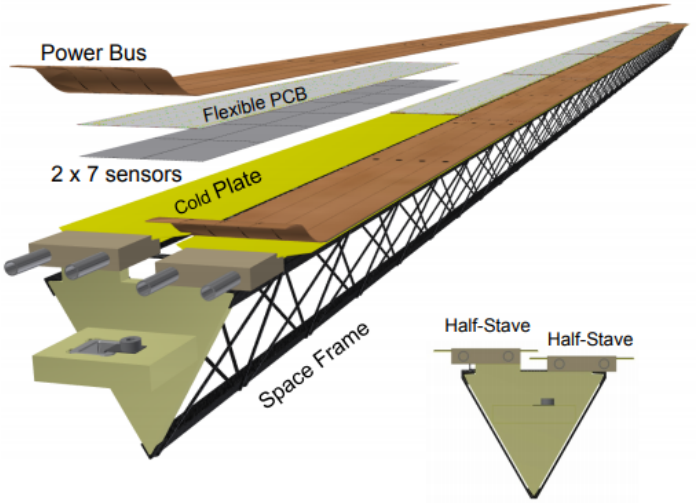


SUMMARY

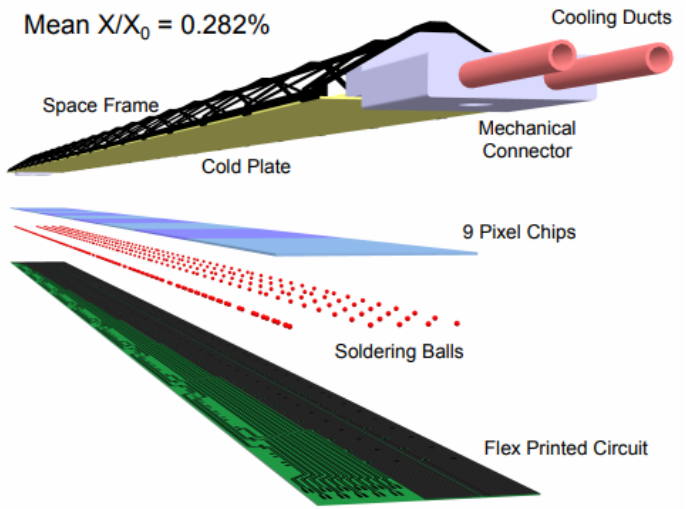
- Vertex: R&D on CMOS pixel sensors to achieve high spatial resolution, fast readout, low power consumption …
  - Prototype sensors: JadePix-1/2/3, MIC4, Taichu-1/2
- Tracker: effort started on the silicon tracker
  - Start building a short stave with available components (ATLASPix3, QuadModule, stave core …)
  - Sensor design: ATLASPix3 to CEPCPix
- Mechanical design started and vertex/tracker layout being re-optimized for improved performance

SUPPORTING STRUCTURE

ALICE Outer Layer Stave ~0.8% X_0

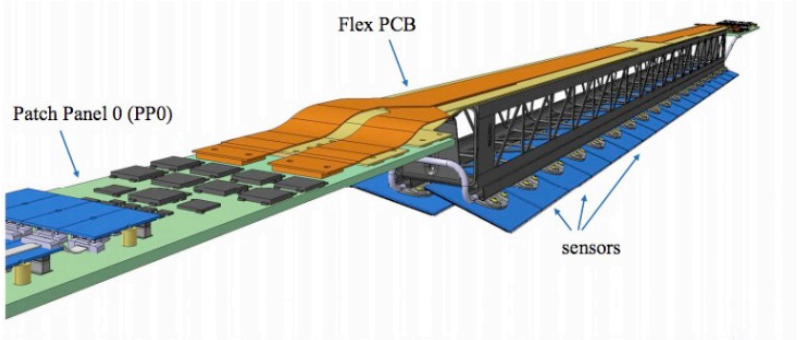


ALICE Inner Layer Stave ~0.3% X_0



ATLAS-ITK: 0.5% X_0 ITK alpine stave (+module)

ATLAS IBL: 0.7% X_0 IBL stave, (+module)



CEPC design target:

0.65% X_0 for stave + modules

Crucial elements:

- Light-weighted carbon truss structure
- Al based flex (prototype with Cu)