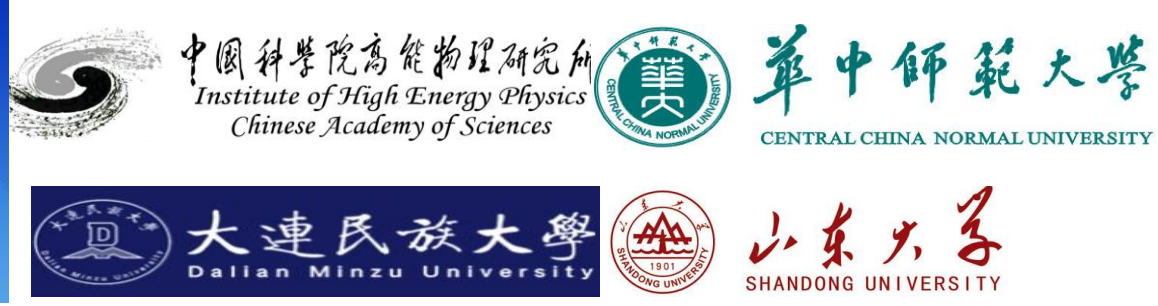


Development of CMOS pixel sensors with high resolution and low power for the CEPC vertex detector

Ying ZHANG (IHEP)

On behalf of the study group

26-28 October 2020, CEPC2020, Shanghai Jiao Tong University, Shanghai

Outline

- **CEPC vertex detector requirements**
- **CMOS pixel sensor R&D activities**
  - Study of sensing diode, low power binary pixel and readout architecture
  - Updates on JadePix3 prototype
- **Perspective for the next step**
- **Summary**

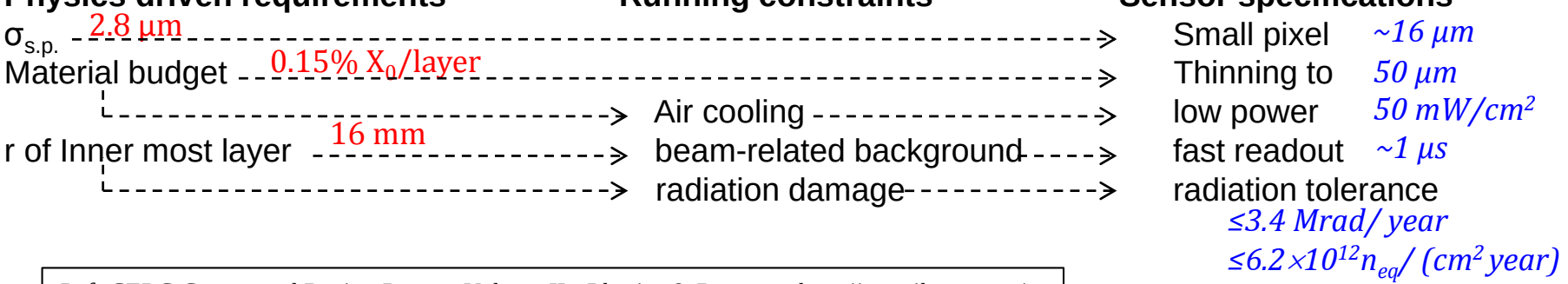
Introduction: requirements (CDR)

On the pixel sensor for the efficient tagging of heavy quarks

- **To achieve single point resolution**
  - Digital pixel with in-pixel discriminator, pitch ~16 μm
  - Analog pixel, pitch ~20 μm (heavily rely on power pulsing as in the ILC)
- **To lower the material budget**
  - Sensor thickness ~ 50 μm
  - Heat load < 50 mW/cm^2 constrained by air cooling
- **To tackle beam-related background**
  - ~ μs level readout, 25 ns beam spacing @ Z-pole operation
  - 3.4 Mrad/year & 6.2×10^{12} neq/ (cm^2·year)

Baseline design parameters for CEPC vertex detector

	R (mm)	$\|z\|$ (mm)	$\|\cos\theta\|$	σ (μm)
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4



Ref: CEPC Conceptual Design Report, Volume II - Physics & Detector, http://cepc.ihep.ac.cn/

Double-sided ladder concept

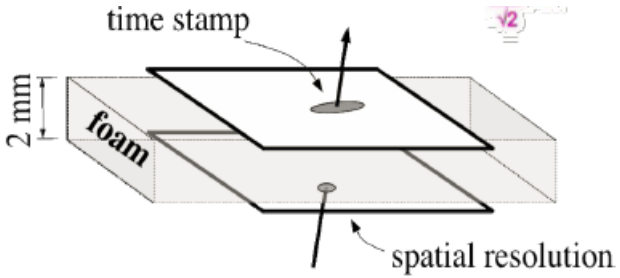
Two different sensors mounted on the opposite sides of the ladder (layer 1-2)

- A fine pitch, low power sensor for layer1

→ To achieve high spatial resolution

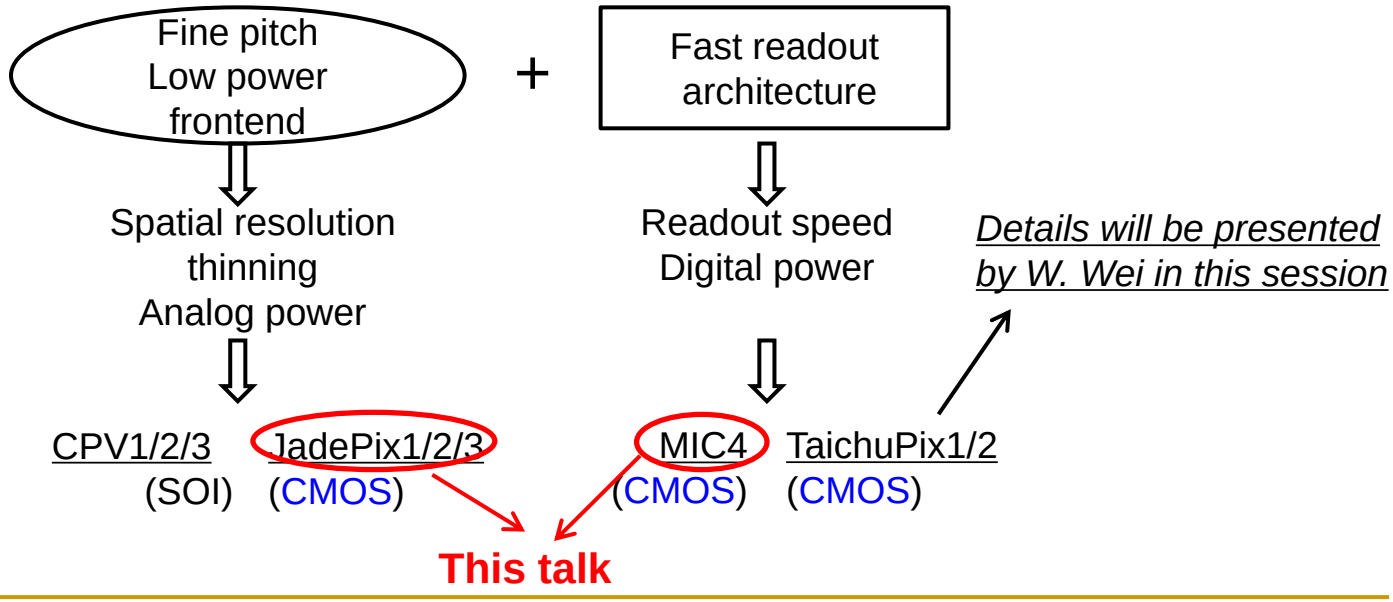
- A faster sensor for layer2

→ To provide necessary time-stamp for tracking



ILD-like double-sided concept without power-pulsing mode

- **R&D for CEPC vertex based on the double-sided concept**

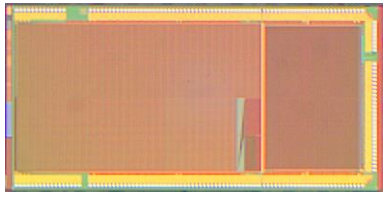


Developed CMOS Pixel Sensor prototypes overview

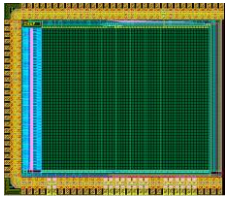
	JadePix1	JadePix2	MIC4	JadePix3
	2015	2017		2019
Architecture	Roll. Shutter + Analog output	Roll. Shutter + In pixel discri.	Data-driven r.o. + In pixel discri.	Roll. shutter + end of col. priority encoder
Pitch (μm^2)	33 × 33 /16 × 16	22 × 22	25 × 25	16 × 26 16 × 23.11
Power con. (mW/cm^2)	--	--	150	~ 55*
Integration time (μs)*	--	40-50	~3	~100
Prototype size (mm^2)	3.9 × 7.9 (36 individual r.o)	3 × 3.3	3.1 × 4.6	10.4 × 6.1
Main goals	Sensor optimization	Small binary pixel	Small pixel + Fast readout+ nearly full functional	Smaller pixel + Low power + fully functional

* Assuming a matrix of 512 ×1024 pixels

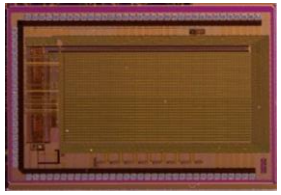
All prototypes in TowerJazz 180 nm process



JadePix1 (IHEP)



JadePix2 (IHEP)



MIC4 (CCNU & IHEP)

JadePix3 (IHEP, CCNU, Dalian Minzu Unv., SDU)

Sensing diode optimization

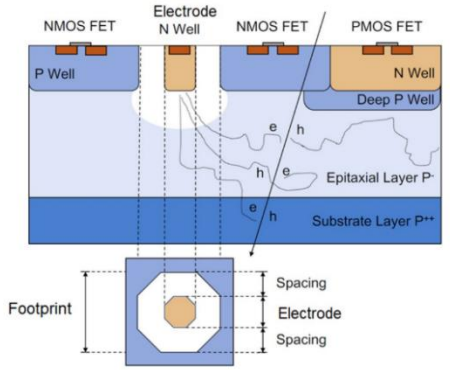
Higher Q/C lower analog power

$$N \propto \frac{1}{\sqrt{g_m}} \quad S = \frac{Q}{C} \Rightarrow \frac{S}{N} \propto \frac{Q}{C}\sqrt{g_m} \propto \frac{Q}{C}\sqrt[2a]{I}$$

$$P \propto I \propto \left(\frac{S/N}{Q/C}\right)^{2a} \qquad g_m \propto I^{\frac{1}{a}}$$

Fixing the S/N for a given bandwidth

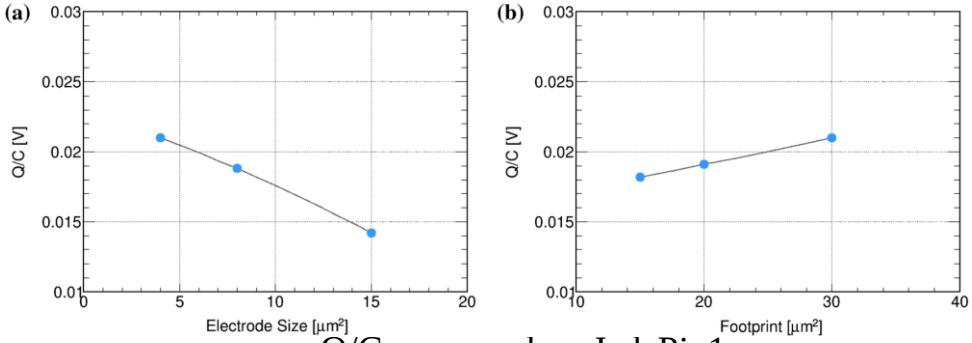
a = 2 in strong inversion
a = 1 in weak inversion



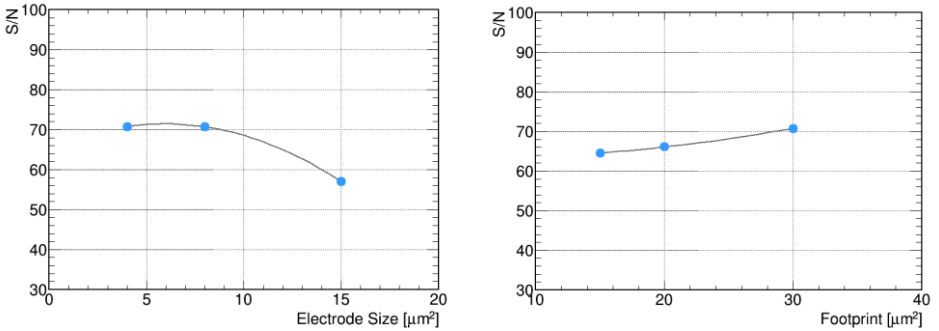
Schematic cross section of a CPS pixel

- **Different sensor geometries verified in JadePix1**
  - Small collection electrode and large footprint preferred to achieve high Q/C
  - Small collection electrode and large footprint can yield high S/N ratio → preferred for efficient detector operation
- **Electrode size = 4 μm², Footprint = 36 μm² chosen for JadePix3**
- **Apply a negative bias voltage (up to -6V) to the substrate in JadePix3**

  → to reduce C, enhance Q/C



Q/C measured on JadePix1



S/N measured on JadePix1

Binary pixel validated

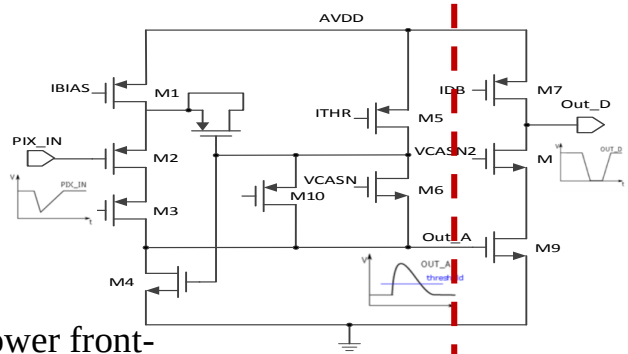
- **In-pixel discrimination preferred for lower power comparing with end-of-column dis.**
- **Two different approaches validated**

➢ Digital pixel in MIC4

- Based on a low power binary front-end (derived from ALPIDE chip*), with modified data-driven readout architecture

Ref: D. Kim et al., 2016 JINST 11 C02042

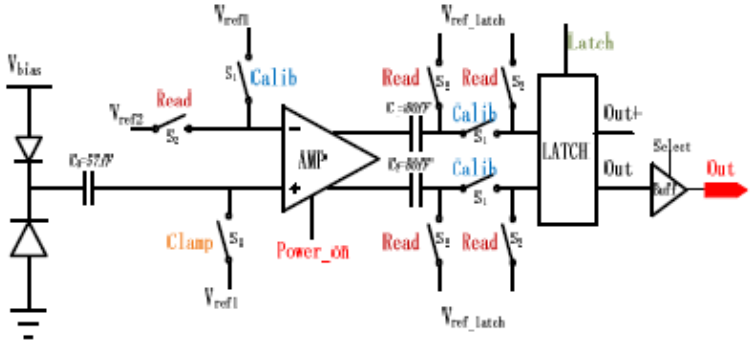
- Measured ENC ~32 e^-, analog power ~0.11 μW/pixel
- Pixel size: 25× 25 μm^2
- pros: fast readout (integration time of ~ 3 μs)
- cons: difficult to achieve ~3 μm resolution



A low power front-end in MIC4

➢ Digital pixel in JadePix2

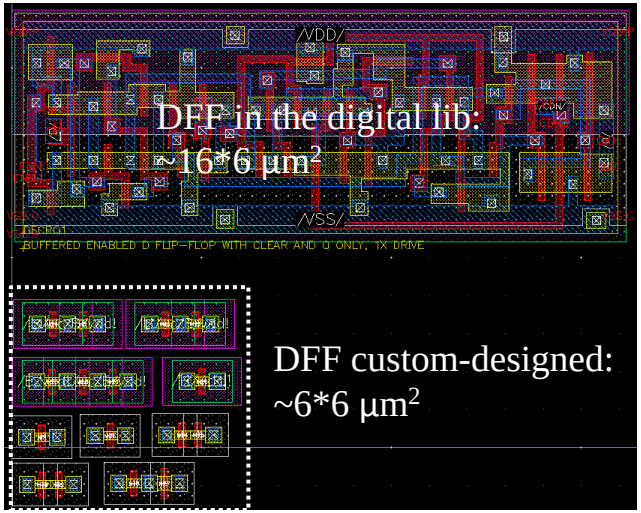
- AC-coupled sensor (allows a larger S/N) + amplifier + comparator + dynamic latch + rolling shutter readout
- Measured ENC: ~31 e^-, analog power of ~6.7 μW/pixel
- Pixel size: 22× 22 μm^2
- pros: expected to offer < 4 μm resolution
- cons: difficult to evolve 30 μs readout time

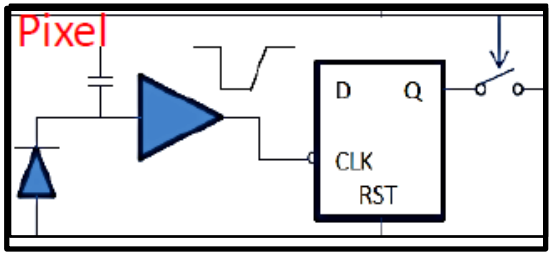


A binary pixel in JadePix2

Binary pixel design in JadePix3

- **Design goals: smaller pixel size and low power**
- **16 × 23.11 μm² binary pixels implemented in JadePix3**
  - Low power binary front-end benefits from MIC4
    - Reduction on the layout area
    - Lower analog power: 0.04 μW/pixel (60% reduction)
  - Pixel read out in rolling shutter mode → very limited in-pixel logics needed (D-FlipFlop & switch) ➔ reduce area
  - Custom-designed DFF to reduce the layout area by 60%





Pixel structure of JadePix3

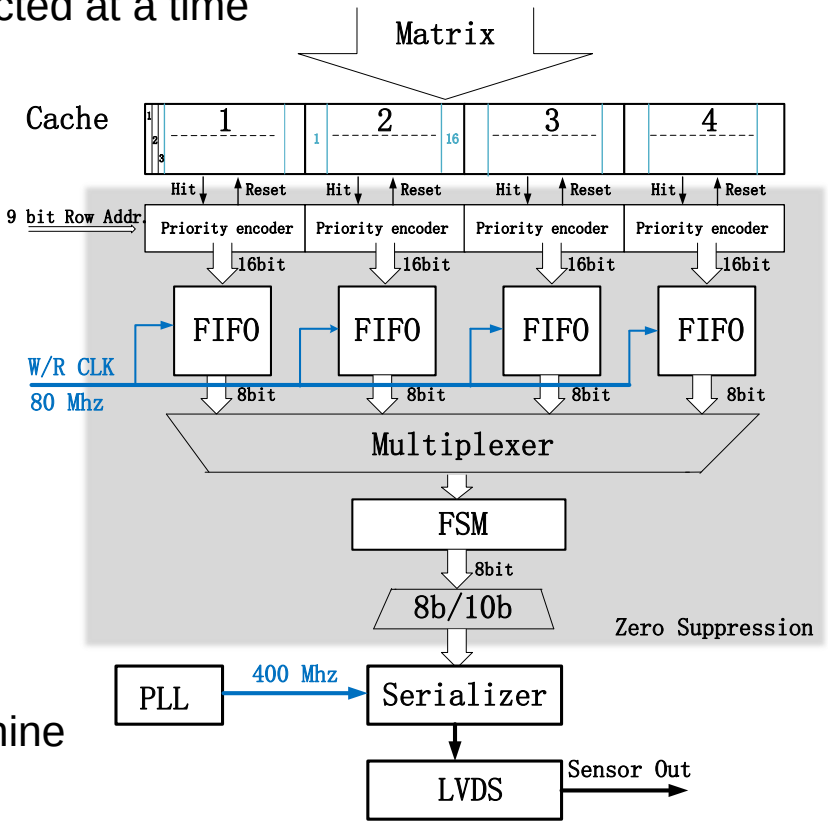
Periphery data processing of JadePix3

- **Rolling shutter readout combined with a novel zero suppression scheme**
  - 512 row × 192 column pixels, one row selected at a time
  - **Zero suppression at the end of column**
    - Every 48 columns divided into 16 blocks
    - 'Fired' blocks identified sequentially by a 4-bit priority encoder at the end of column
    - Readout time: 200 ns/row → 102 μs/frame
  - Only hit information fed into FIFO

Row #	Block #	hits in block
9-bit	4-bit	3-bit

    - FIFO R/W at 80 MHz
    - FIFO depth: 48
  - Data stream steered by a Finite State Machine
  - Data rate after 8b/10b: 800 Mbit/s
  - Estimated power cons. ~76 mW
    - 15 mW (Zero suppression), 25 mW (Serializer), 20 mW (PLL), 16 mW (LVDS)

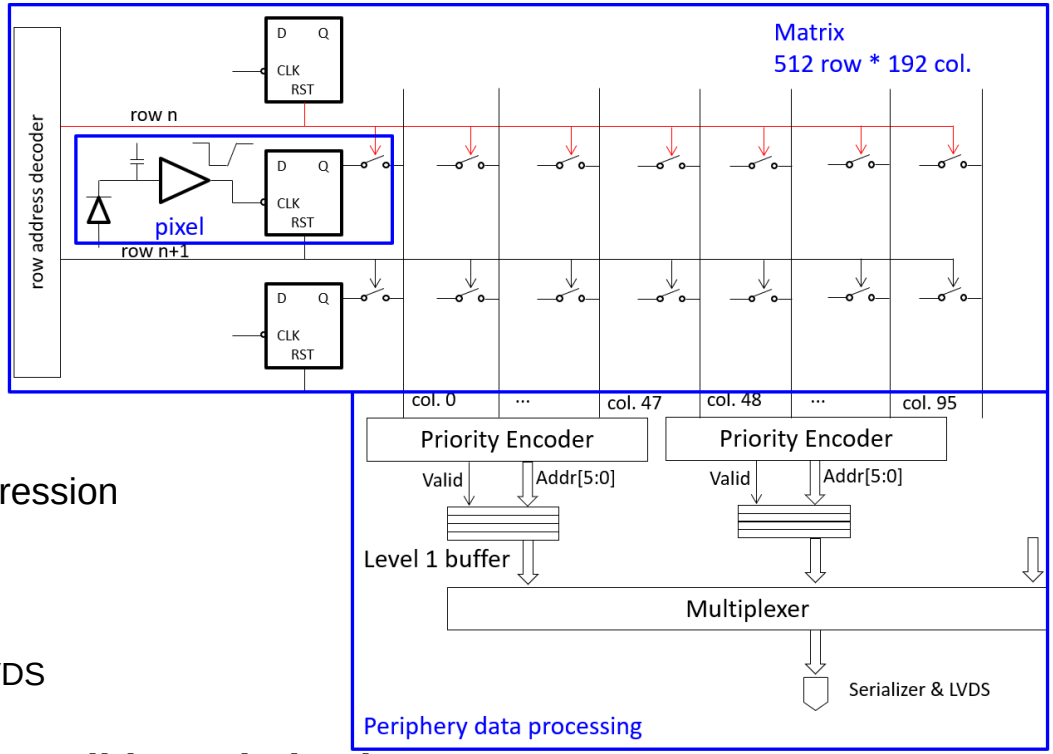
    → Expected power density of **55 mW/cm^2**, considering a matrix of 1 × 2 cm^2



Block diagram of periphery circuit in JadePix3

JadePix3: fully functional prototype with small pixel

- **Submitted in Oct. 2019**
- **Fabrication finished in May 2020**
- **Chip size 10.4 mm × 6.1 mm**
- **512 row × 192 col. pixel array**
  - Rolling shutter readout
- **Fully functional periphery logics**
  - Fully integrated logics for zero suppression
  - On-chip bias generation
  - Data transmission logics
    - 8B/10B encoder, PLL, serializer, LVDS



- **4 variants of pixel to investigate possible optimization**

Sector	Diode	Front-end	Pixel digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	**16×26 μm²**
1	2 + 2 μm	FE_V0	DGT_V1	**16× 26 μm²**
2	2 + 2 μm	FE_V0	DGT_V2	**16× 23.11 μm²**
3	2 + 2 μm	FE_V1	DGT_V0	**16×26 μm²**

Characterization of JadePix3 will start soon

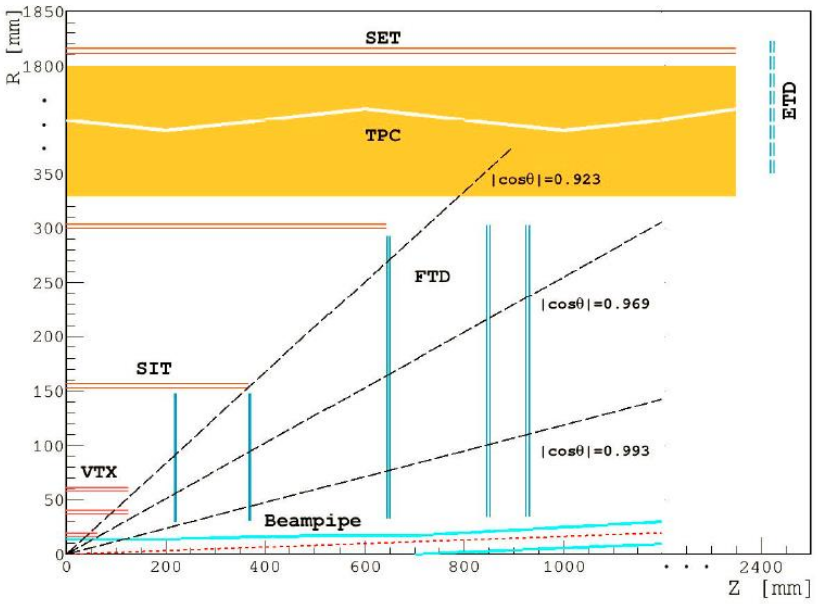
Plan of JadePix3 test and next prototype design

- **Test board for JadePix3 under fabrication, readout system finalizing**
- **Tests to do:**
  - Electrical test to characterize the individual parts on chip, noise, threshold, power, data rate, etc.
  - Measurement with radioactive sources
  - Beam test in 2021

- **Next prototype (JadePix4) design**

  With the concept of double-sided ladders, two options considered:
  - Option 1: Expanding pixel matrix to 512 rows by 1024 columns using the architecture of JadePix3, to provide ~3 μm spatial resolution
  - Option 2: Exploiting prototype with ~μs level readout, which may derived from MIC4, to features the required speed

Perspective for the R&D of next few years



Design parameters of the CEPC vertex system in CDR

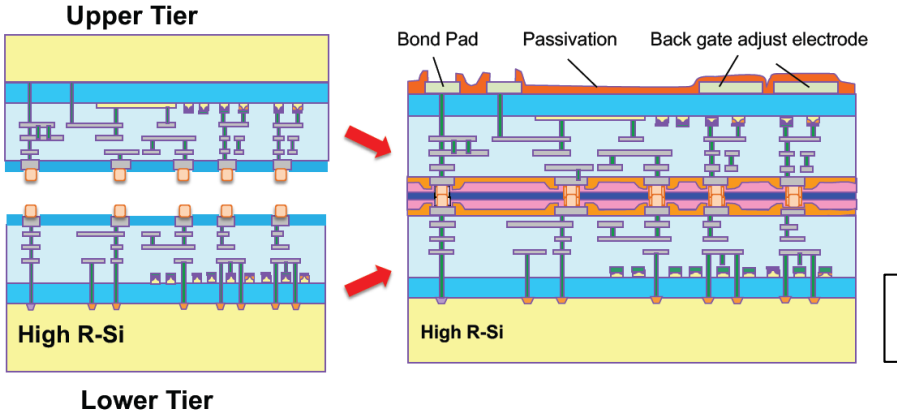
	R(mm)	| Z |(mm)	$\sigma(\mu m)$	material budget
Layer 1	16	62.5	2.8	0.15%/X_0
Layer 2	18	62.5	6	0.15%/X_0
Layer 3	37	125.0	4	0.15%/X_0
Layer 4	39	125.0	4	0.15%/X_0
Layer 5	58	125.0	4	0.15%/X_0
Layer 6	60	125.0	4	0.15%/X_0

- **Optimization for system requirements: resolution, radiation level, Z-pole operation mode, …**
- **Development of CMOS sensors with fast readout and time stamp**
- **Exploration of new process to improve JadePix3 performance**
  - 3D-integrared process
  - 65 nm CMOS process

  } allow improving readout speed, while keep/reduce pixel size (min.16 × 23.11 μm^2 in JadePix3)
  - Ultra-light, self-supported layers with stitching CMOS sensors, allow for a loosen requirement on the spatial resolution

SOI based 3D integration

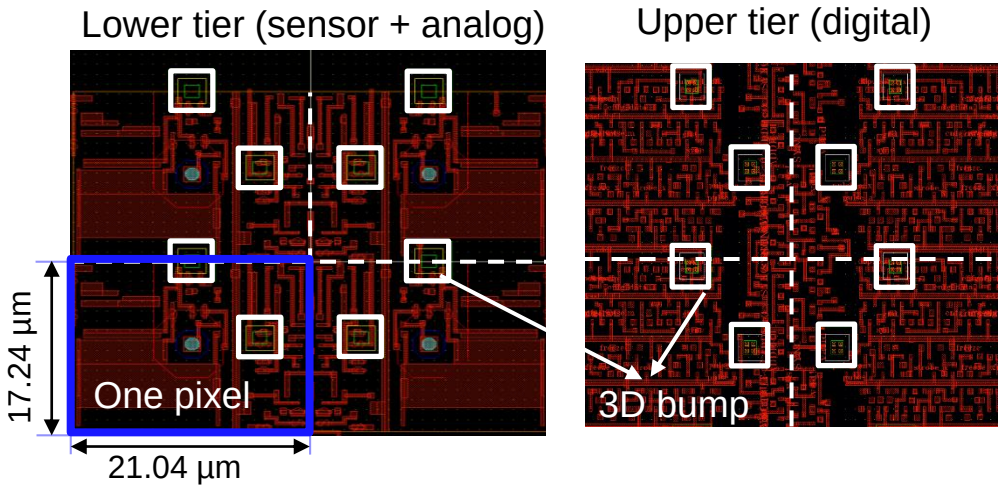
- **SOI-3D has been demonstrated by the SOFIST 3D chip for the ILC**



T-Micro process

Ref: M. Yamada, IEEE 3DIC, Oct. 8th, Sendai, Japan, 2019

- **IHEP designed the first SOI-3D chip (CPV4_3D) for CEPC**
  - Pixel size: 17.24 × 21.04 μm^2
  - Readout time: ~1 μs
  - Power density: ~ 50 mW/cm^2
  - will be submitted in Nov. 2020

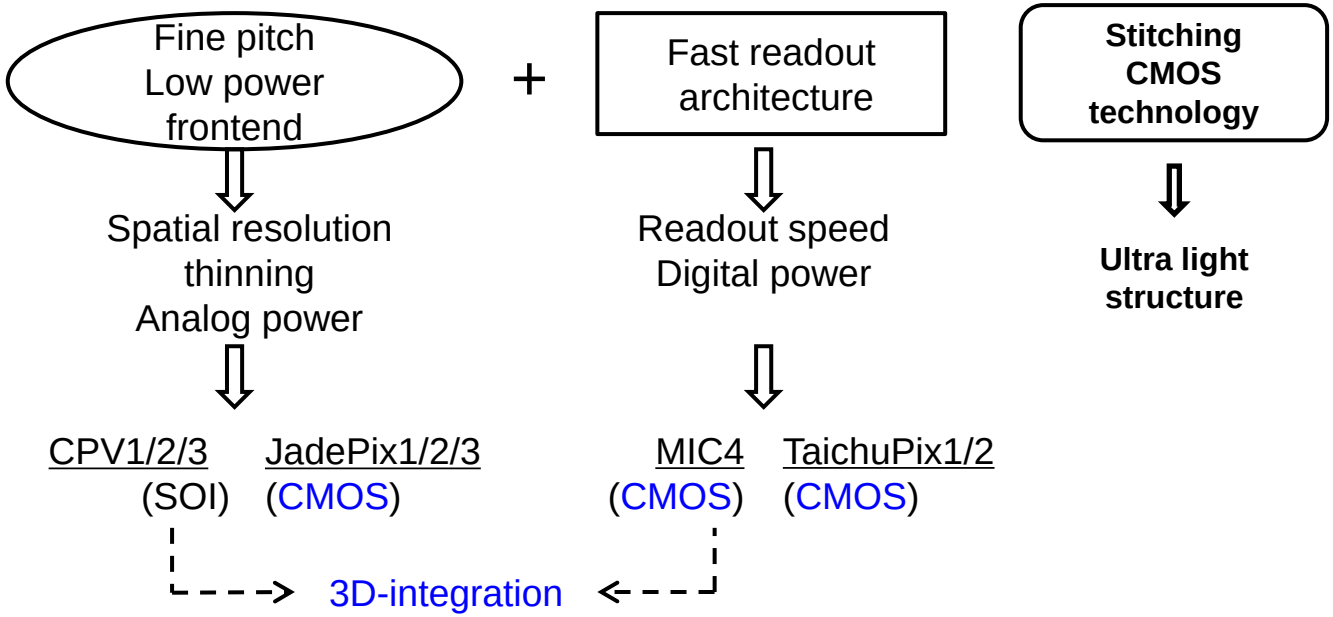


The lower tier can be either SOI or CMOS pixel sensor

➔ a hybrid 3D-integration of CMOS + SOI may considered

Summary

- **Stringent requirements for CEPC vertex detector have driven R&D programs**
- **JadePix3, a medium scale (512 × 192 pixels) fully functional CMOS prototype, fabricated and will be tested soon**
  - small pixel: min.16 × 23.11 μm^2
  - power density < 100 mW/cm^2
- **New process (65 nm process, a hybrid 3D-integration of CMOS + SOI) and stitching CMOS technology will be explored**



ACKNOWLEGMENTS

- IHEP: Y. Lu, Y. Zhang, Y. Zhou, Z. Wu, L. Song, J. Dong, Q. Ouyang, L. Chen, H. Zhu, R. Kiuchi, X. Shi, K. Wang, N. Wang
- CCNU: P. Yang, L. Xiao, D. Guo, D. Zhang, W. Ren, C. Meng, A. Xu, X. Sun
- Dalian Minzu Unv: Z. Shi
- SDU: L. Zhang, M. Wang

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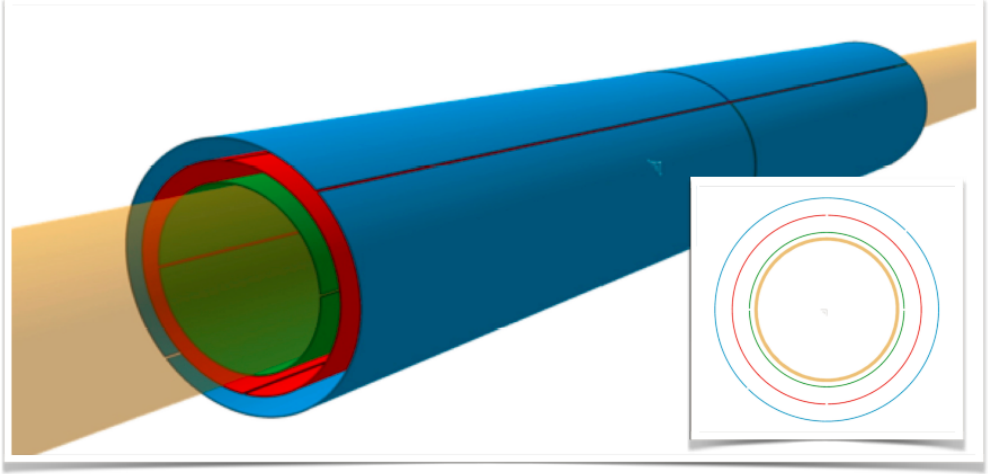
- the National Key Program for S&T Research and Development (2016YFA0400400, 2016YFE0100900)
- the National Natural Science Foundation of China (11605217, 11575220, 11935019, 11505207)
- the CAS Center for Excellence in Particle Physics (CCEPP)

Thanks for your attention !

Backup slides

ALICE ITS3 with stitching CMOS technology



Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

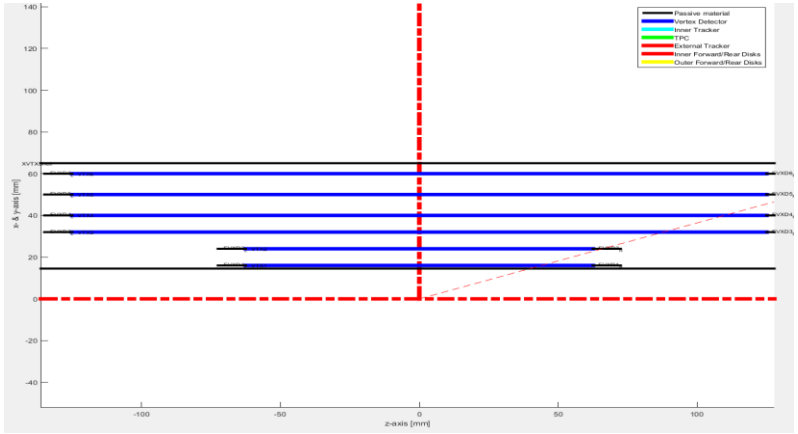
- New beam pipe:
  - "old" radius/thickness: 18.2/0.8 mm
  - new radius/thickness: 16.0/0.5 mm
- Extremely low material budget:
  - Beam pipe thickness: 500 µm (0.14% X0)
  - Sensor thickness: 20-40 µm (0.02-0.04% X0)
- Material homogeneously distributed:
  - essentially zero systematic error from material distribution

Similar layout with CEPC layer 1-3

M. Mager | ITS3 | VERTEX 2019 | 17.10.2019 | 14

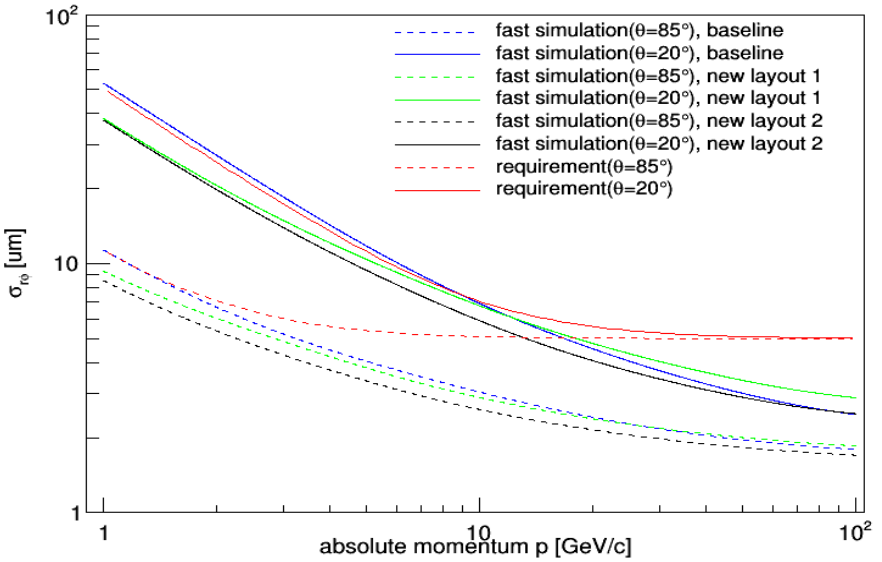
An ultra light structure vertex layout

	R(mm)	|Z|(mm)	σ(μm) (layout1/layout2)	material budget
Layer1	16	62.5	4/2.8	0.05%X_0
Layer2	24	62.5	4/4	0.05%X_0
Layer3	32	125	4/4	0.05%X_0
Layer4	40	125	4/4	0.05%X_0
Layer5	50	125	4/4	0.05%X_0
Layer6	60	125	4/4	0.05%X_0



- Technology to be explored with 55 nm CIS process
- Joint effort of CCNU and IHEP

ZG Wu, Optimization on silicon detectors at CEPC, CEPC workshop, Nov.2019, Beijing



Comparing with baseline layout

- better performance (~20% improvement) for layout1 at low momentum, but poor performance at high momentum
- both within the requirement

Ref: Q. Ouyang, 30 July, ICHEP 2020

CEPC Beam Timing

	Higgs	W	Z (3T)	Z (2T)
Center-of-mass energy (GeV)	240	160	91	
Number of IPs	2			
Luminosity/IP (10^{34} cm^{-2} s^{-1})	3	10	16	32
Number of years	7	1	2	
Total Integrated Luminosity (ab^{-1}) - 2 IP	5.6	2.6	8	16
Total number of particles	1×10^{6}	2×10^{7}	3×10^{11}	7×10^{11}
Bunch numbers (**Bunch spacing**)	242 (**680 ns**)	1524 (**210 ns**)	12000 (**25ns + 10% gap**)	

- Continuous colliding mode
  - Duty cycle ~ 50% @ Higgs, close to 100% @ W/Z
- General requirement on the detector development:
  - Precise measurement, Low power, Fast readout, Radiation-hard

Y. LU, Circular Electron Positron Collider workshop, Beijing, Nov. 2018.

Beam-induced Radiation Backgrounds

- **Radiation level for VTX first layer**

	H (240)	W (160)	Z (91)
Hit Density [hits/cm^2·BX]	2.4	2.3	0.25
TID [MRad/year]	0.93	2.9	3.4
NIEL [10^{12} 1 MeV n_{eq}/cm^2·year]	2.1	5.5	6.2

Table 9.4: Summary of hit density, total ionizing dose (TID) and non-ionizing energy loss (NIEL) with combined contributions from pair production and off-energy beam particles, at the first vertex detector layer ($r = 1.6$ cm) at different machine operation energies of $\sqrt{s} = 240$, 160 and 91 GeV, respectively.

- **Vertex detector occupancy**

Operation mode	**H (240)**	**W(160)**	**Z (91)**
Hit density (hits · cm^{-2} · BX^{-1})	2.4	2.3	0.25
Bunching spacing (μs)	0.68	0.21	0.025
Occupancy (%)	0.08	0.25	0.23

Table 4.2: Occupancies of the first vertex detector layer at different machine operation energies: 240 GeV for ZH production, 160 GeV near W-pair threshold and 91 GeV for Z-pole.

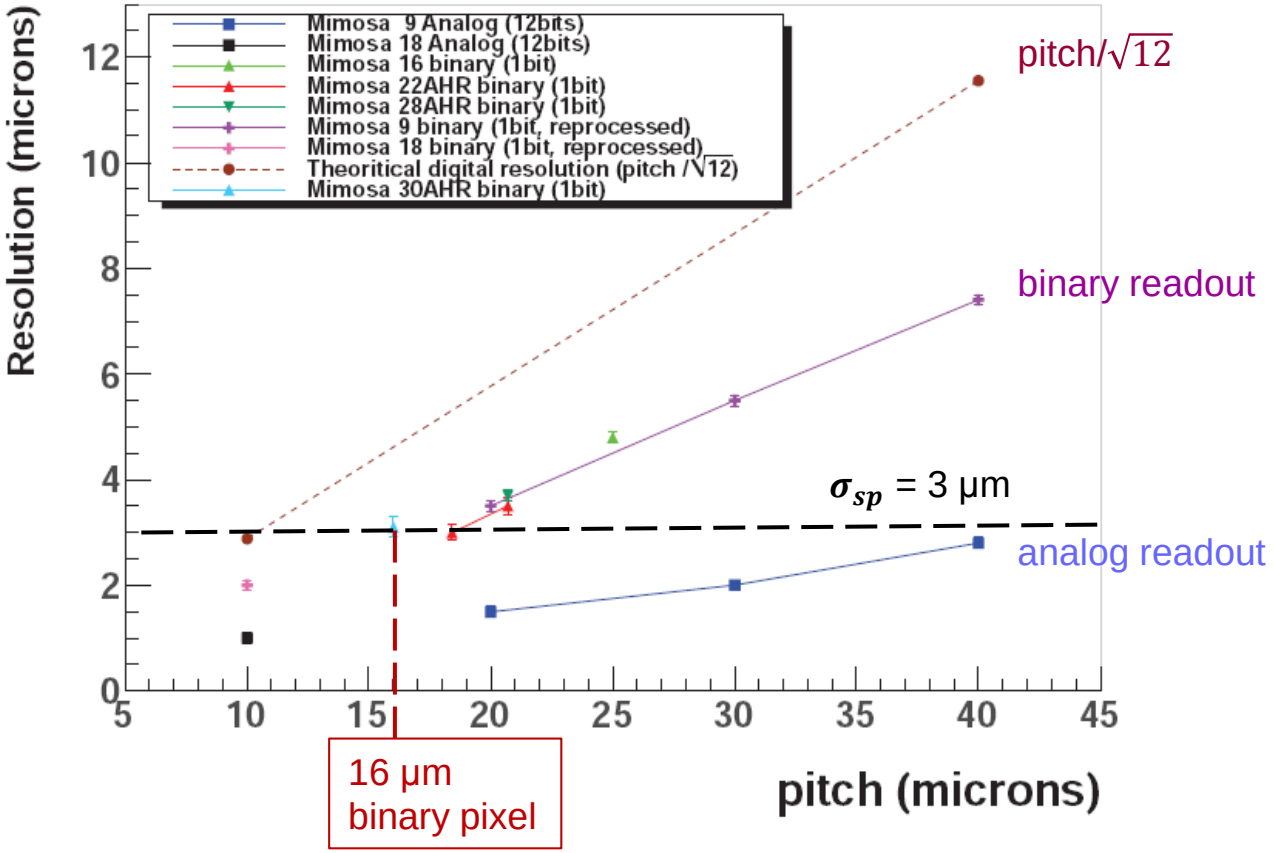
Detector **occupancy < 1%**, assuming 10 μs of readout time for the silicon pixel sensor and an average cluster size of 9 pixels per hit.

CEPC CDR Volume II- Physics & Detector, IHEP-CEPC-DR-2018-02.

Improving the spatial resolution

Single point resolution σ_{sp} ≤ 3 μm ➔ pixel size ?

spatial resolution vs. pixel pitch

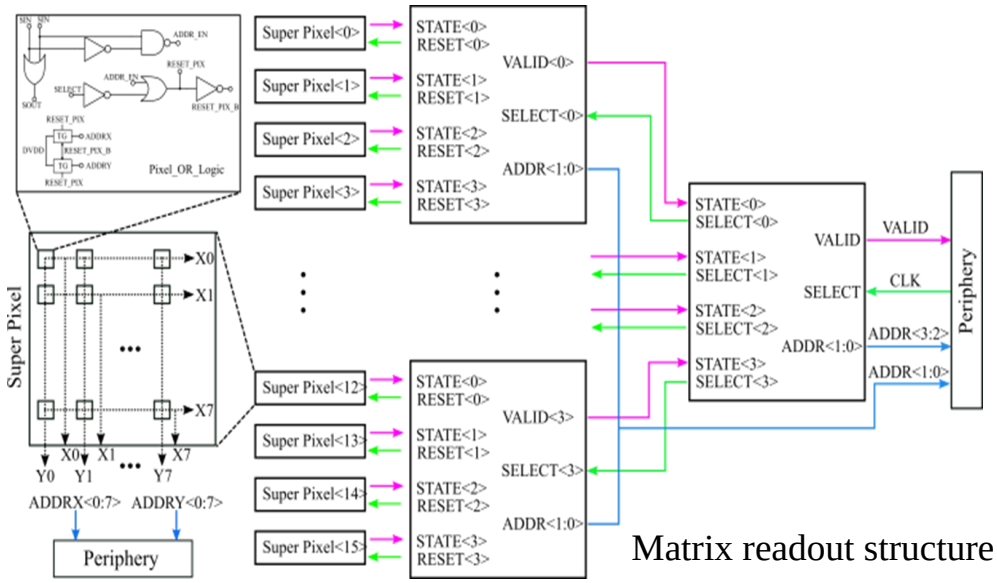


Ref: Y. Voutsinsa, et al., Vertex Detectors 2012

Data-driven readout of MIC4

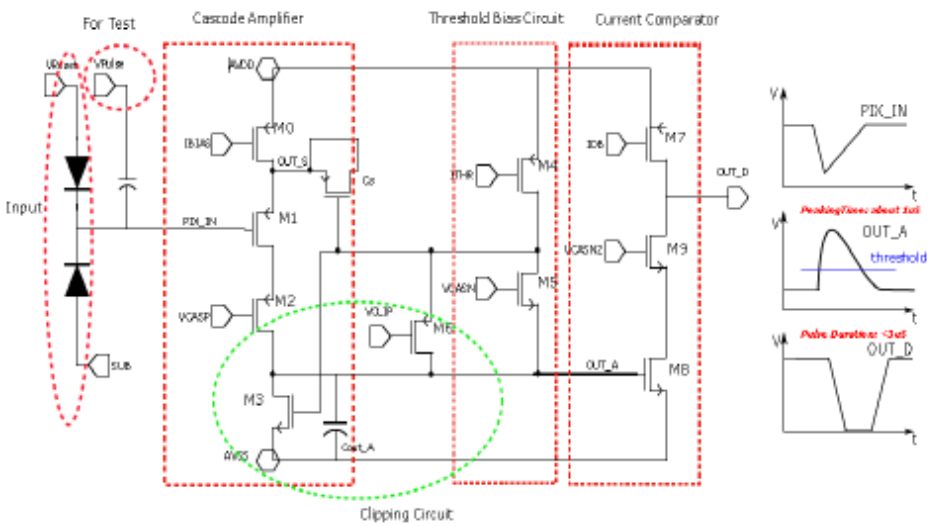
Improvements on pixel matrix readout structure to reduce area

- **25 × 25 μm² binary pixels implemented and verified in MIC4**
  - **OR-gate chain inside a super pixel** (8×8 pixels) to do the zero-suppression, two dimension projection (ADDRX & ADDRY) to identify the hit pixel ➔ save pixel logic and routing lines area
  - **Zero-suppression**: OR-gate chain & Address Encoder and Reset Decoder (AERD) combination ➔ for highly compact pixel & fast readout & low power
  - Measured TN = 6 e^- , FPN = 31 e^- for pixels with version-1 front-end

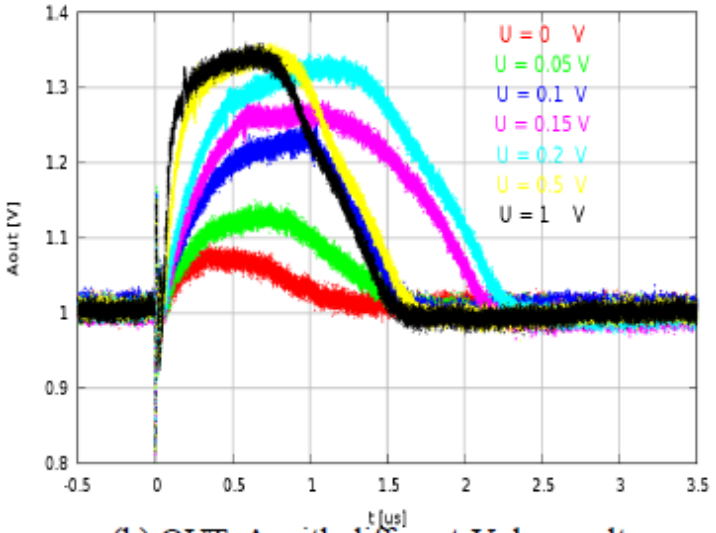


Matrix readout structure of MIC4

Low power front-end in MIC4

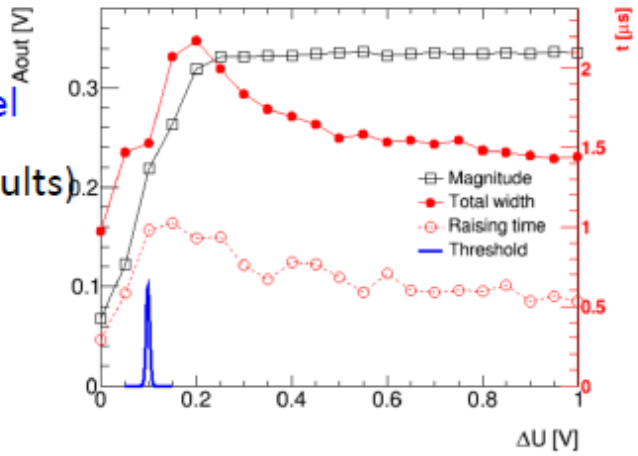


(a)Front-end V2 based on ALPIDE by Weiping Ren @ CCNU



(b) OUT_A with different Vpluse voltage

- The ALPIDE front-end structure, Power: 110 nW/pixel
- Peaking time< 1 μs, duration < 3 μs (sim and test results)
- Mean threshold around 99 e- (test results)
- Mean FPN ~ 31 e-, TN ~ 6 e- (test results)



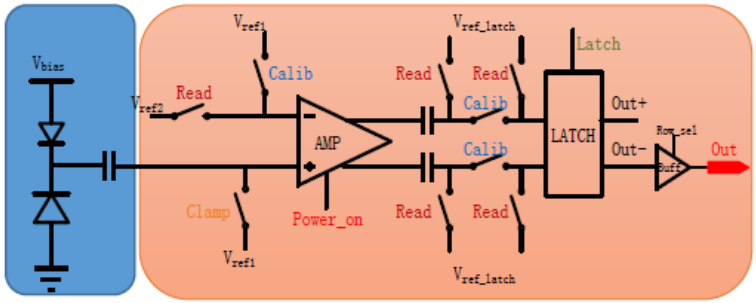
(c) Test results of peaking time and duration time

P. YANG, CEPC workshop, Beijing, Nov. 2019.

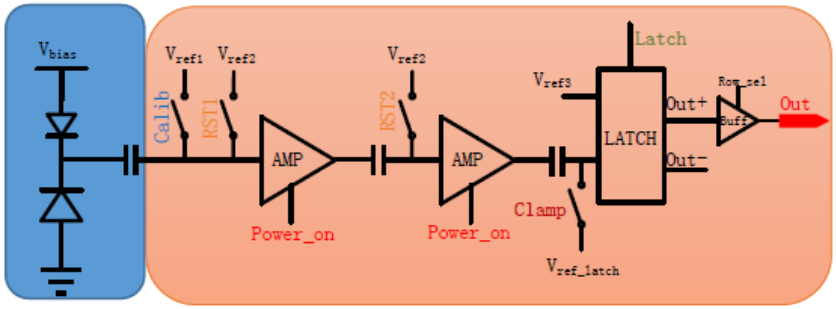
JadePix-2 design

IHEP Team

- **Pixel size: 22 × 22 μm²**
- **Two versions of front-end**
  - Version 1: differential amplifier + dynamic latch
  - Version 2: single-ended amplifier + dynamic latch
- **Offset cancellation and high precision comparator**
  - FPN (Fix Pattern Noise) ~ 20 e-
  - TN (Temporal Noise) ~ 7 e-



Version 1: differential amplifier + latch

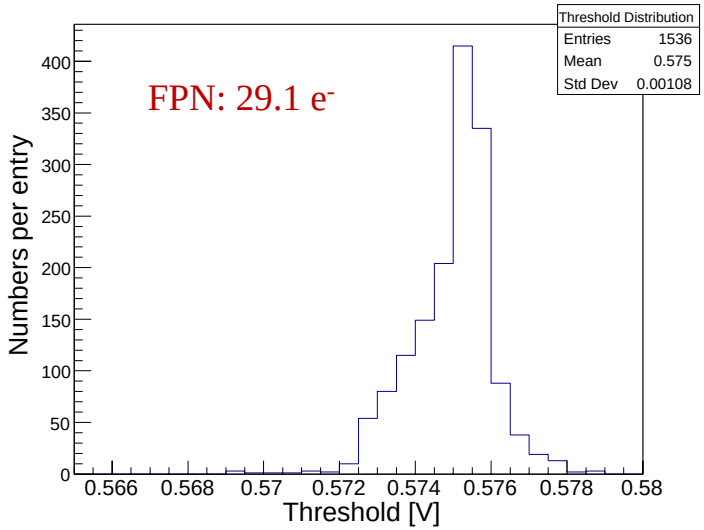


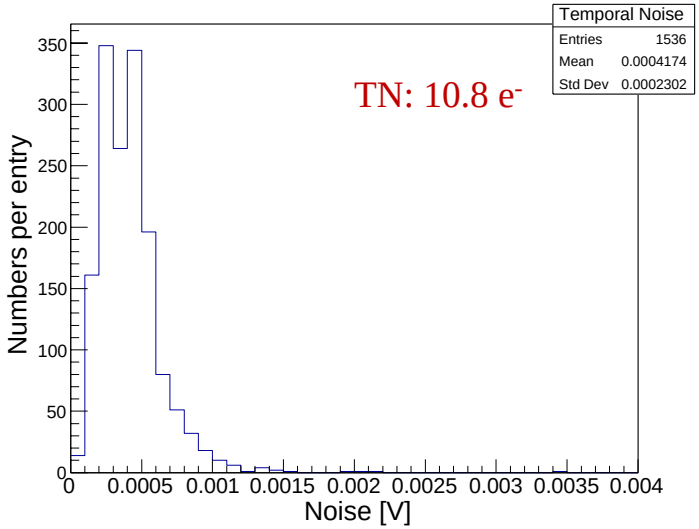
Version 2: two stage common source amplifiers + latch

JadePix-2 test results

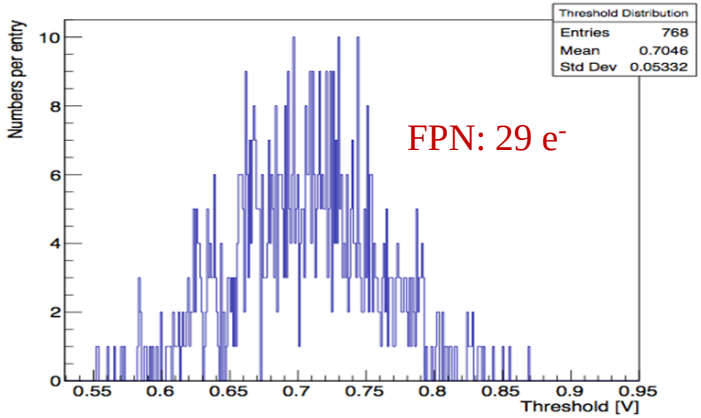
- **Noise performance**

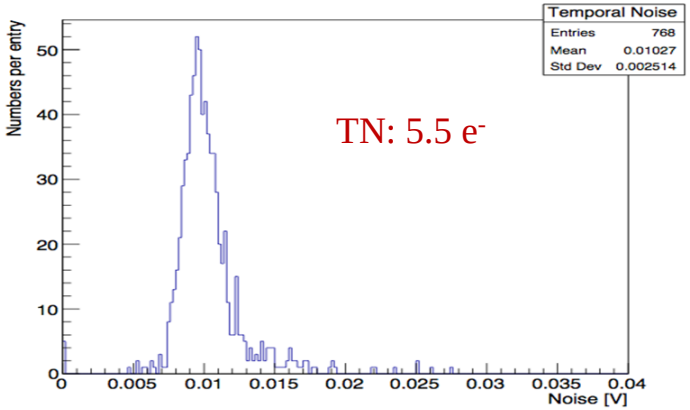
Measured noise of version-1 pixel





Measured noise of version-2 pixel





JadePix3: Diode & Front-end design

- Sensing diode: negatively biased for high Q/C
  - Electrode size 4 μm^2, with a small footprint 36 μm^2
- Frontend: tradeoff between layout area and FPN
  - Reduction on the layout area, ~200 μm^2
  - Improvement on the FPN = 3.1e$^-$ (simulation)
  - A low power version (20nA), equivalent to 9 mW/cm^2