65nm FEE ASIC for TPC

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Outline

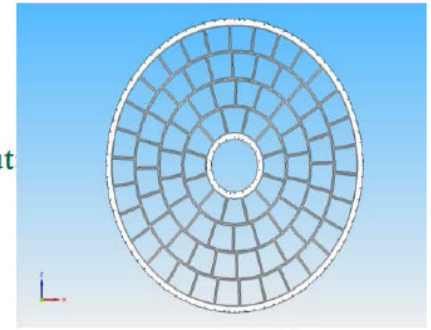
- Introduction
- Preliminary Test Results
- Summary

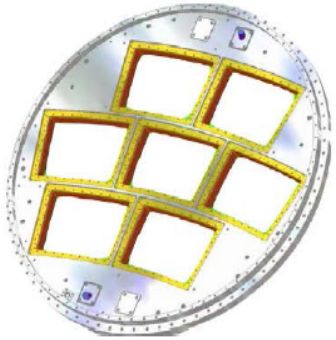
Introduction

Pad TPC and Pixel TPC

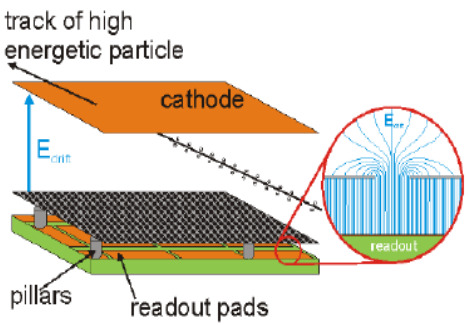
Pad TPC for collider

- Active area: 2×10m²
- One option for endplate readout
  - GEM or Micromegas
  - 1×6 mm² pads
  - 10^6 Pads
  - 84 modules
  - Module size: 200×170mm²
  - Readout: Super ALTRO
  - CO_2 cooling





Pixel TPC for collider

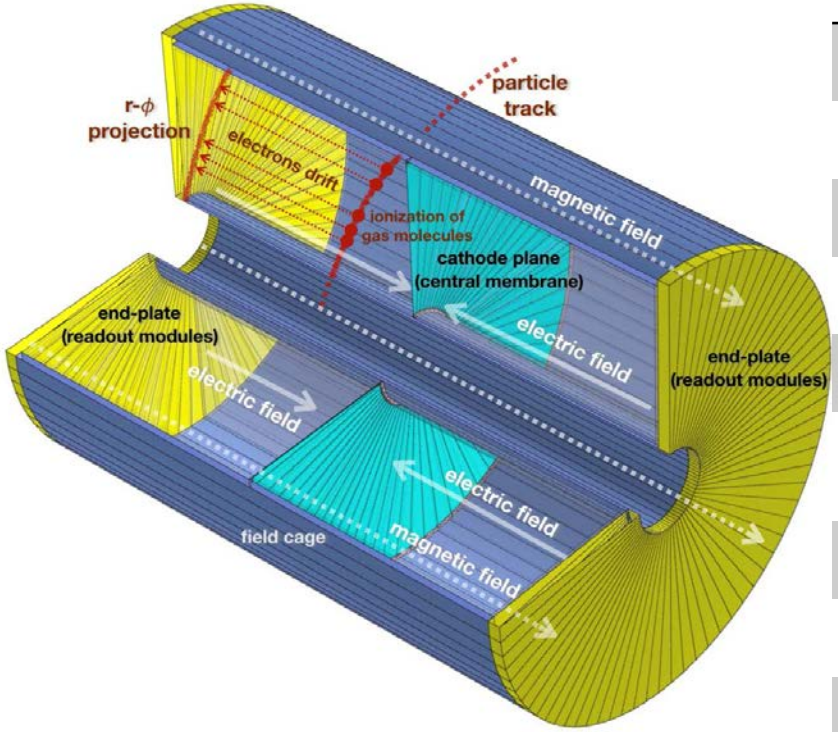


For Collider @cost:
But to readout the TPC with GridPixes:
→100-120 chips/module
240 modules/endcap (10 m^2)
→50k-60k GridPixes
→ 10^9 pixel pads

Benefits of Pixel readout:

- Lower occupancy
  - → 300 k Hits/s at small radii.
  - → This gives < 12 single pixels hit/s.
  - → With a read out speed of 0.1 msec (that matches a 10 kHz Z rate)
  - → the occupancy is less than 0.0012
- Improved dE/dx
  - → primary e- counting
  - Smaller pads/pixels could result in better resolution!
  - Gain <2000
  - Low IBF*Gain<2
  - CO_2 cooling

CEPC TPC



Momentum resolution (B=3.5T)	$\delta(1/p_t \approx 10^{-4}/GeV/c)$
δ_{point} in $r\Phi$	<100 μm
δ_{point} in rz	0.4-1.4 mm
Inner radius	329 mm
Outer radius	1800 mm
Drift length	2350 mm
TPC material budget	$\approx 0.05X_0$ incl. field cage $< 0.25X_0$ for readout endcap
Pad pitch/no. padrows	$\approx$ 1 mm × (4~10mm) /$\approx$ 200
2-hit resolution	$\approx$ 2 mm
Efficiency	>97% for TPC only ($p_t > 1GeV$) >99% all tracking ($p_t > 1GeV$)

- TPC can provide large-volume high-precision 3D track measurement with stringent material budget
- In order to achieve high spatial resolution, small pads (e.g. 1 mm x 6mm) are needed, resulting ~1 million channel of readout electronics
- Need low power consumption readout electronics working at continuous mode

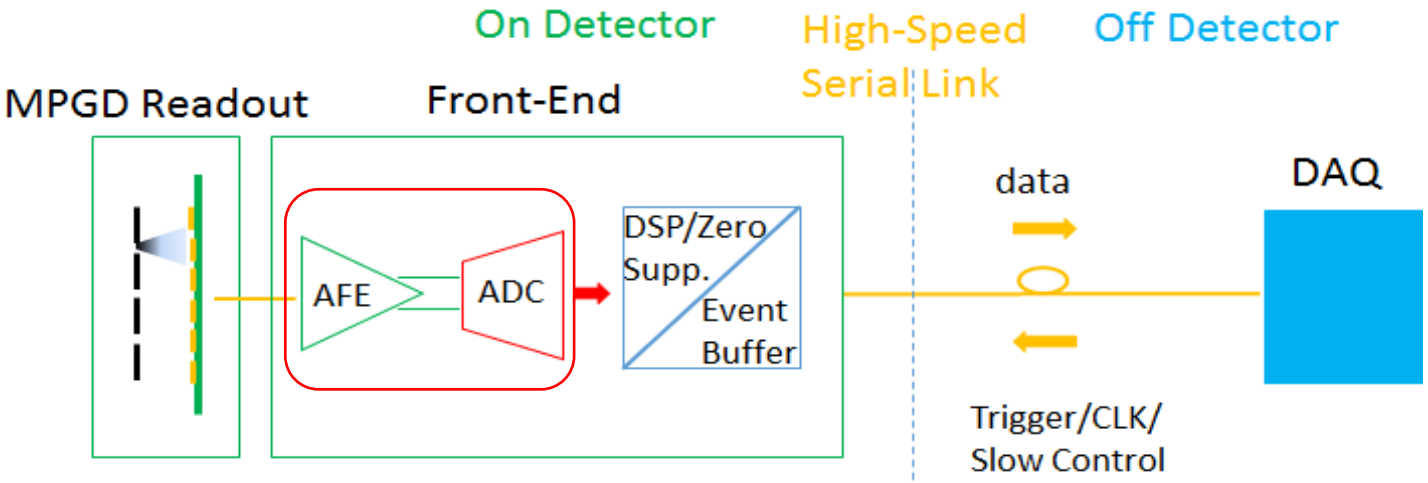
Current TPC Readout ASICs

	PASA/ALTRO	AGET	Super-ALTRO	SAMPA
TPC	ALICE	T2K	ILC	ALICE upgrade
Pad size	4x7.5 mm^2	6.9x9.7 mm^2	1x6 mm^2	4x7.5 mm^2
Pad channels	5.7 x 10^5	1.25 x 10^5	1-2 x 10^6	5.7 x 10^5
Readout Chamber	MWPC	MicroMegas	GEM/MicroMegas	GEM
Gain	12 mV/fC	0.2-17 mV/fC	12-27 mV/fC	20/30 mV/fC
Shaper	CR-$(RC)^4$	CR-$(RC)^2$	CR-$(RC)^4$	CR-$(RC)^4$
Peaking time	200 ns	50 ns-1us	30-120 ns	80/160 ns
ENC	385 e	850 e @ 200ns	520 e	482 e @ 180ns
Waveform Sampler	ADC	SCA	ADC	ADC
Sampling frequency	10 MSPS	1-100 MSPS	40 MSPS	20 MSPS
Dynamic range	10 bit	12 bit(external)	10 bit	10 bit
Power consumption	32 mW/ch	10.0 mW/ch	47.3 mW/ch	8 mW/ch
CMOS Process	250 nm	350 nm	130 nm	130 nm

No current chips can meet the readout requirement for the CEPC TPC

- More advanced 65nm process
- Adopt simplified circuit structure such as SAR-ADC,CR-RC shaper

Architecture and Specifications of FEE



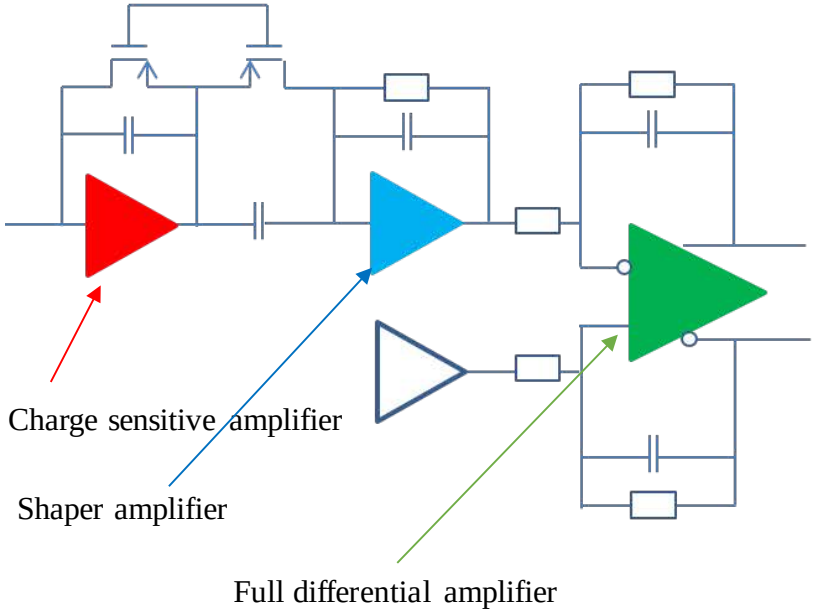
AFE(Analog Front-End)	
Signal Polarity	Negative
Detector Capacitance	5-20 pF
Shaper	CR-RC
Shaping Time	160 ns
ENC (Equivalent Noise Charge)	<500 e @ 10pF
Dynamic Range	120 fC
Gain	10 mV/fC
INL (Integrated Non-Linearity)	<1%
Crosstalk	<1%
Power Consumption (AFE)	<2.5 mW/ch

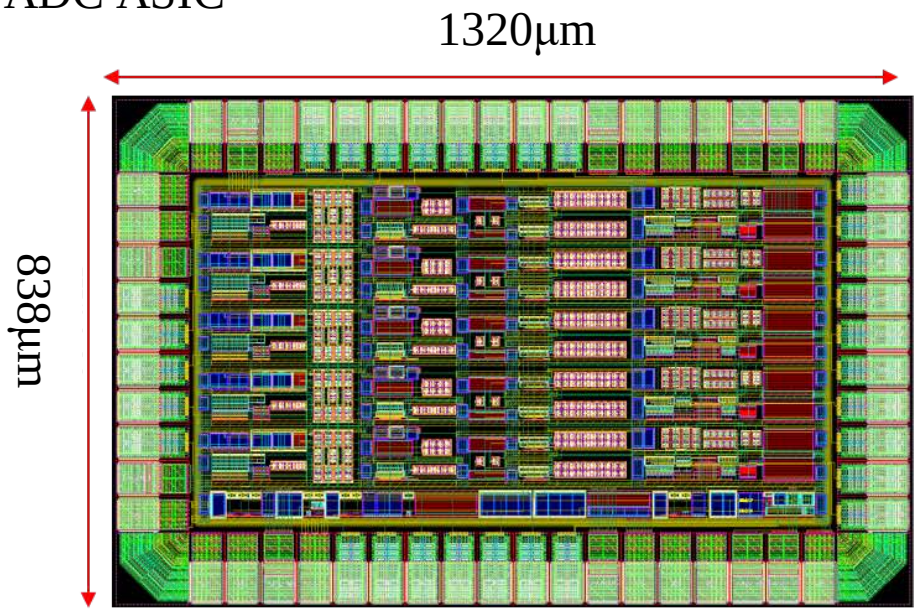
SAR-ADC	
Input Range	-0.6 V ~ 0.6 V diff.
Resolution	10 bit
Sampling Rate	40 MS/s
DNL	<0.6 LSB
INL	<0.6 LSB
SFDR @ 2MHz, 40MSPS	68 dBc
SINAD	57 dB
ENOB	>9.2 bit @ 2MHz
Power Consumption (ADC)	<2.5 mW/ch

Current Status : Analog Front-End ASIC

Three prototype chips have been taped out and evaluated during 2017→ 2018

- 5 channel Analog Front-End ASIC
- Single channel SAR-ADC ASIC
- Single channel Analog Front-End +SAR-ADC ASIC





The test results of main specifications of 5 channel Analog Front-End ASIC：

- Power consumption： 2.02 mW/channel
- Gain： 9.8 mV/fC
- ENC(equivalent noise charge)： 589 e @10pF

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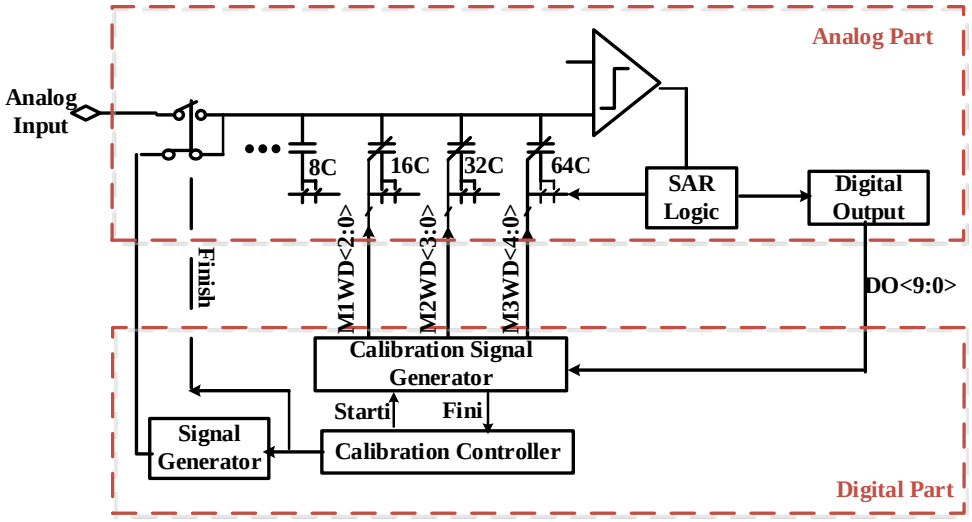
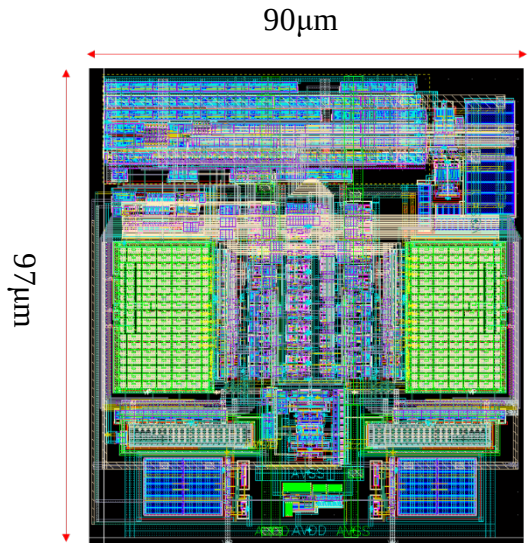
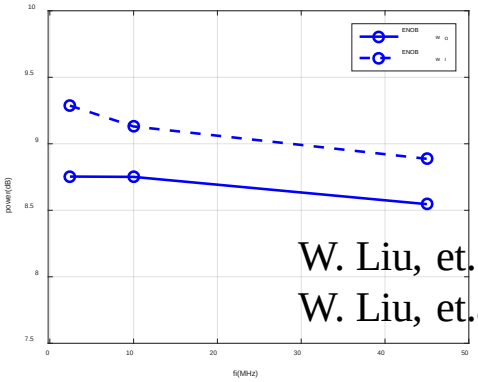
Current Status : SAR ADC





Module Name	Power(mW)
Chip	4.0
Referred Buffer Module	0.25
SAR ADC Core Module	1.0
Clock Generation Module , etc	2.75



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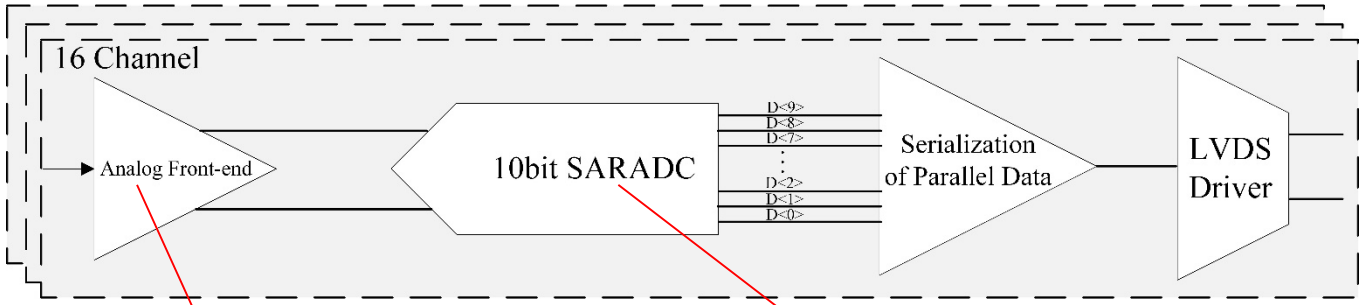
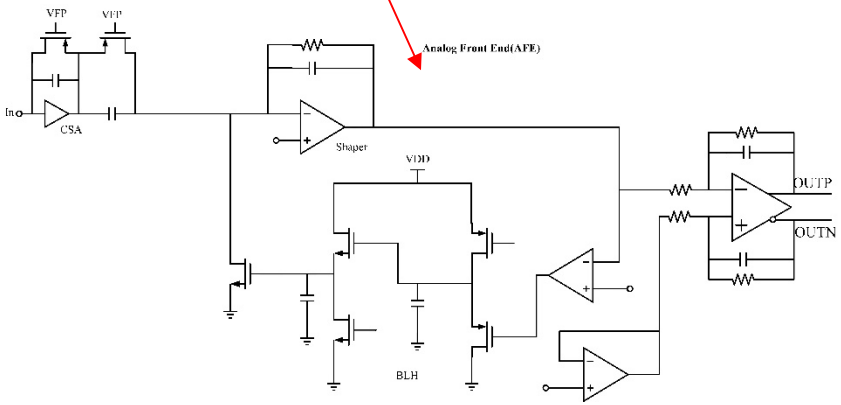
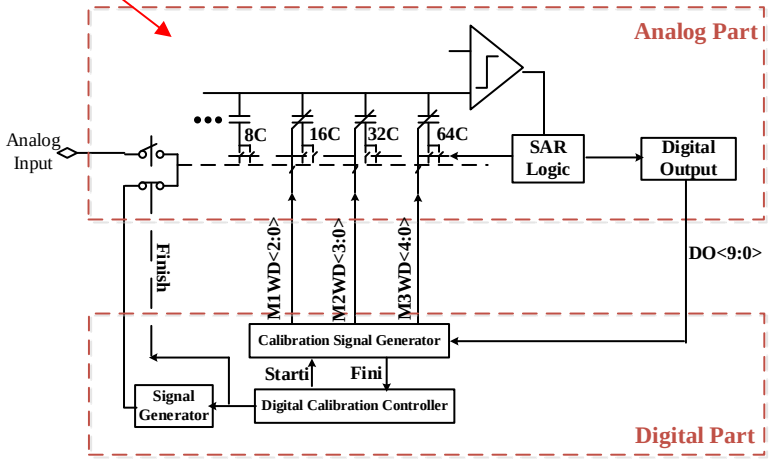
The test results of main specifications of single SAR ADC

- The core power consumption of SAR ADC:1 mW
- Maximum INL(integral non-linearity),DNL(differential nonlinearity)=0.6 LSB
- ENOB=9.15 bit under 50 MS/s sampling rate with 2.4 MHz differential sinewave input

Current Status : The 16-ch TPC Readout ASIC



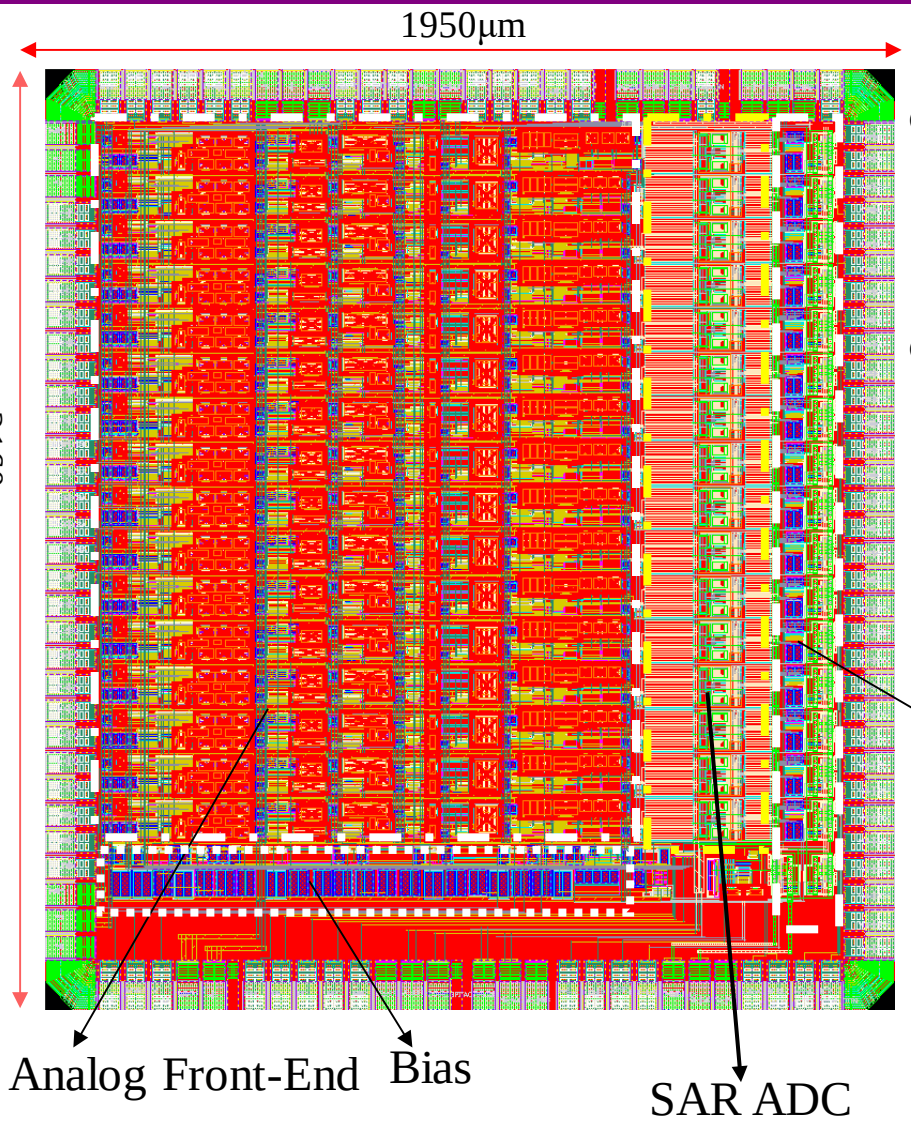




Design highlights:

- 16 channel
- Power consumption of Analog Front-end : from 2.02 mW/channel to 1.4 mW/channel
- ENC : from 589 e to 303 e @10 pF

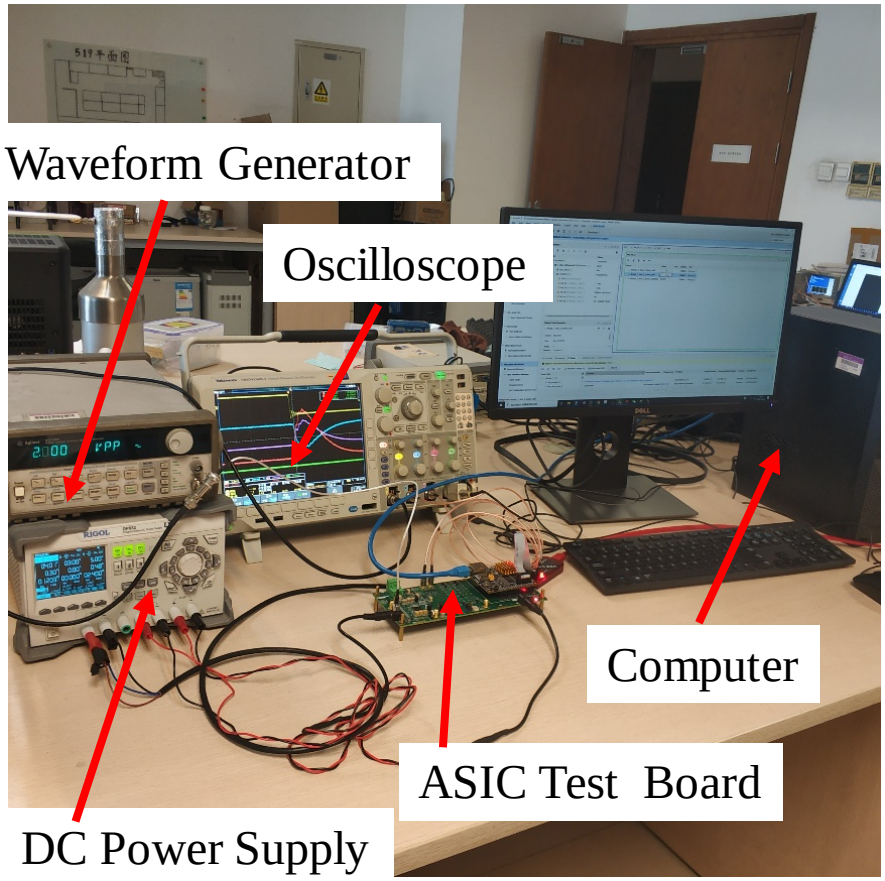
Current Status : Layout of 16-ch TPC Readout ASIC



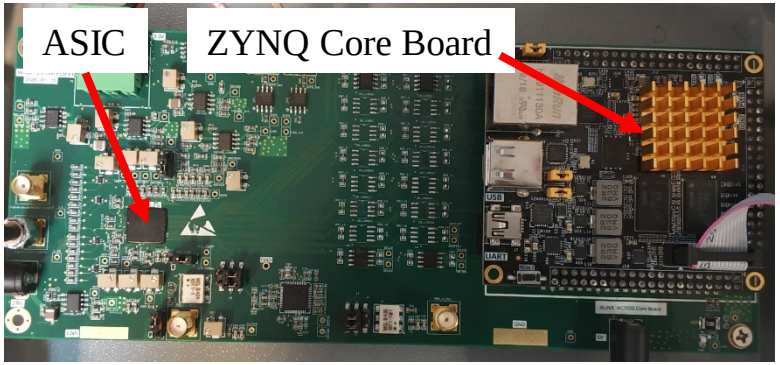
- The floor plan in layout：
  - The die size of 1950 μm x 2160 μm
  - Analog Front-End , SPI, SAR ADC, LVDS driver are supplied by separate power
- The ASIC have been taped out in November 6 ,2019 and is being evaluated.

Test Setup

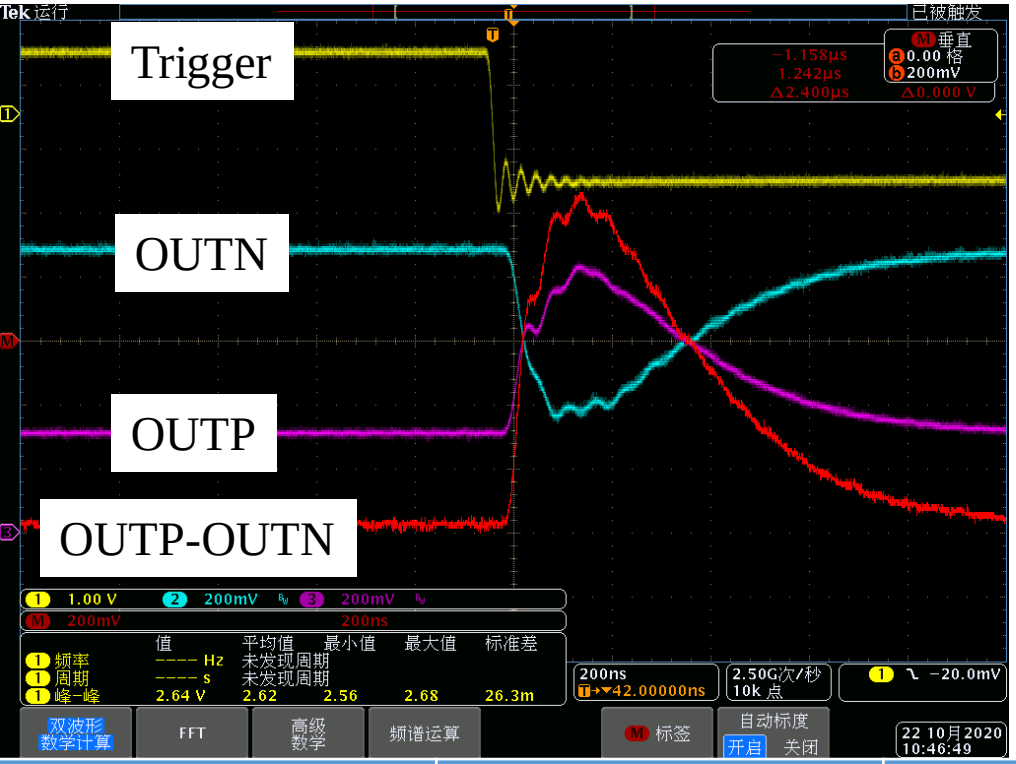
- Test Setup



- ASIC Test Board



Transient Output and Power Consumption



- The test power consumption of Analog Front-end： **1.42 mW/channel** (the simulation: 1.40 mW/channel)
- The static power consumption of SAR ADC: **0.68 mW/channel**

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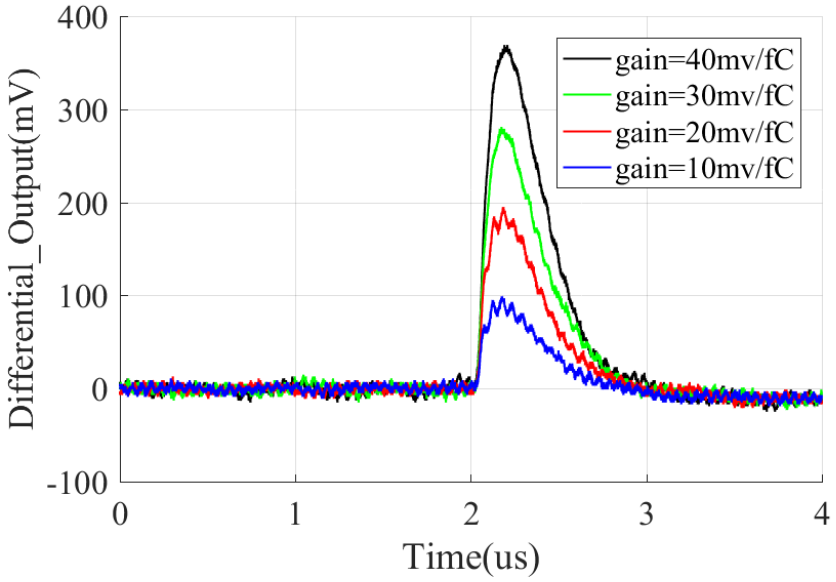
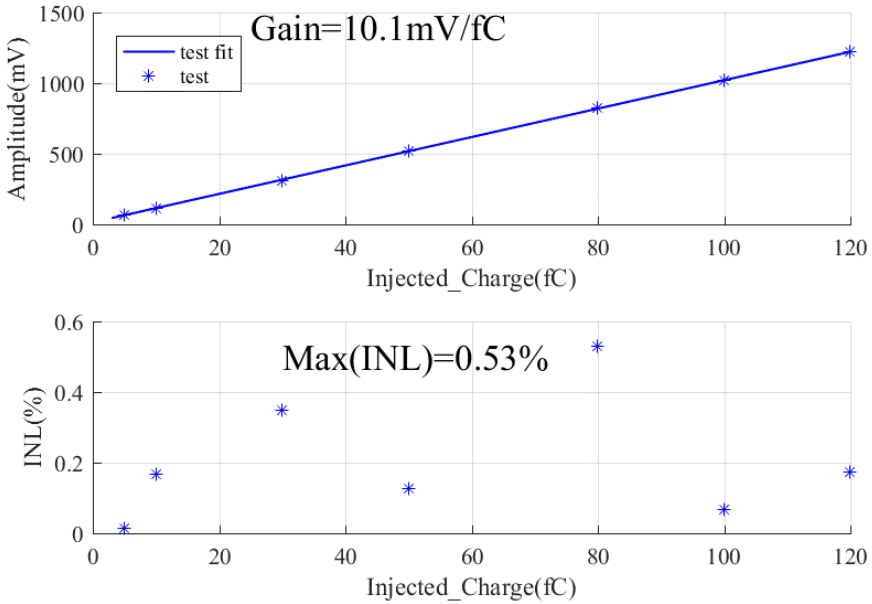
	AFE	ADC	Total
MPW1 Simulation MPW1 Test	1.93 mW/channel 2.02 mW/channel	1.0 mW/channel 1.0 mW/channel	2.93 mW/channel 3.02 mW/channel
MPW2 Simulation MPW2 Test	1.40 mW/channel 1.42 mW/channel	1.0 mW/channel	2.40mW/channel
SAMPA			8 mW/channel

Linearity

- Transient outputs of different gain modes

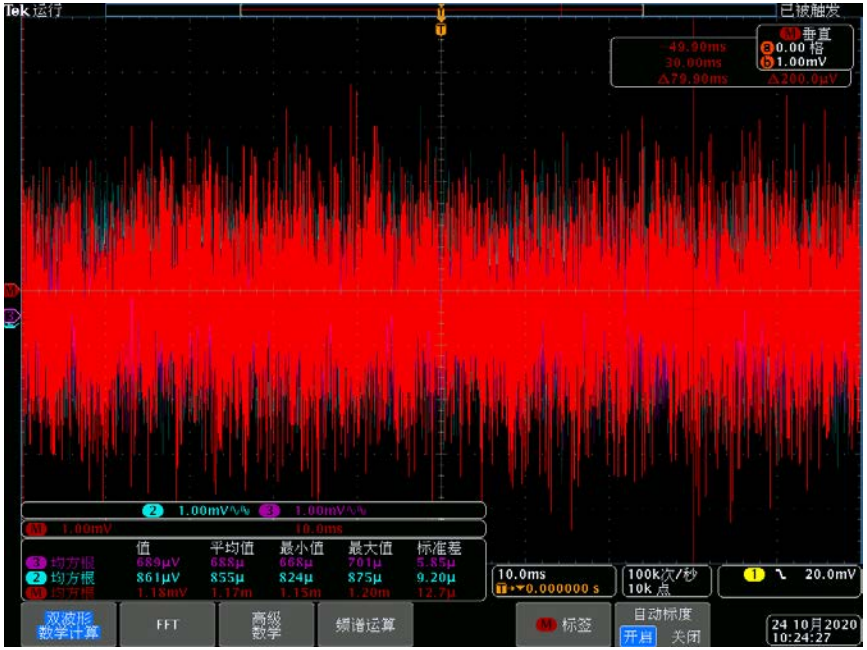


- The linearity (the gain is set to 10 mV/fC)

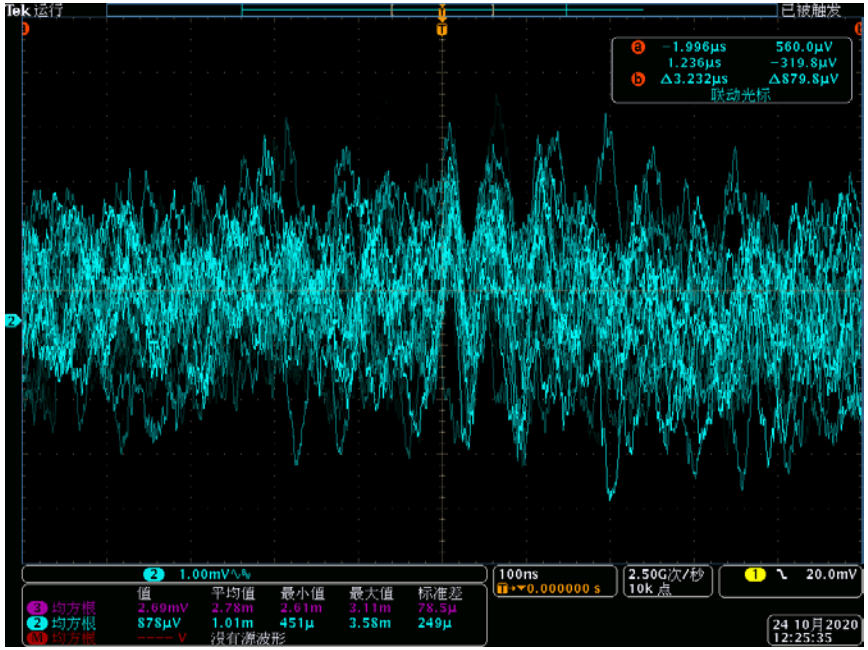


Noise

- The differential output without injected charge



- The periodic interference



- The Equivalent Noise Charge:724 electron @ 2pF input capacitance
- The periodic interference was observed and test board need to be shielded better

Summary

- 16 channel low power consumption and high integration ASIC for TPC readout have been developed and is being evaluated. The preliminary test results of the ASIC show very promising .
  - The power consumption of AFE is 1.42 mW/channel
  - The gain is 10.1 mV/fC
- Future Plan
  - Redesign a new test board ,continue to evaluate ASIC
  - Low power digital filter and data compression in FPGA

Thank You