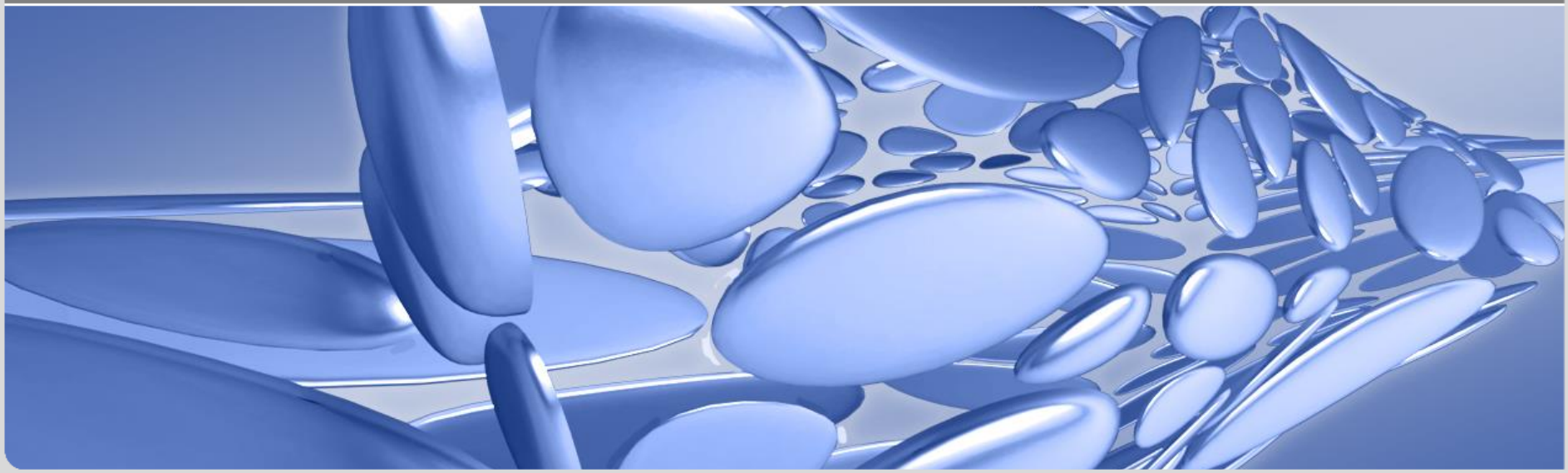
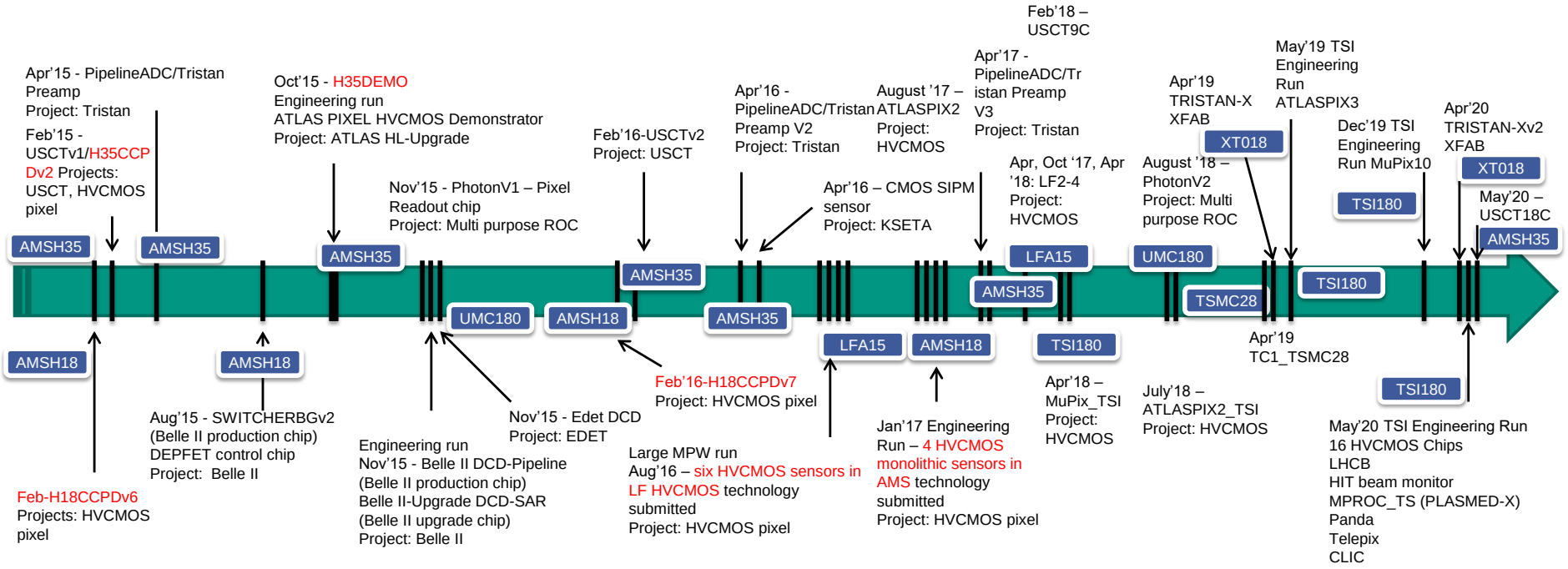
From ATLASPix3 to CEPCPix1

Hui Zhang, Rudolf Schimassek, Richard Leys, Ivan Peric

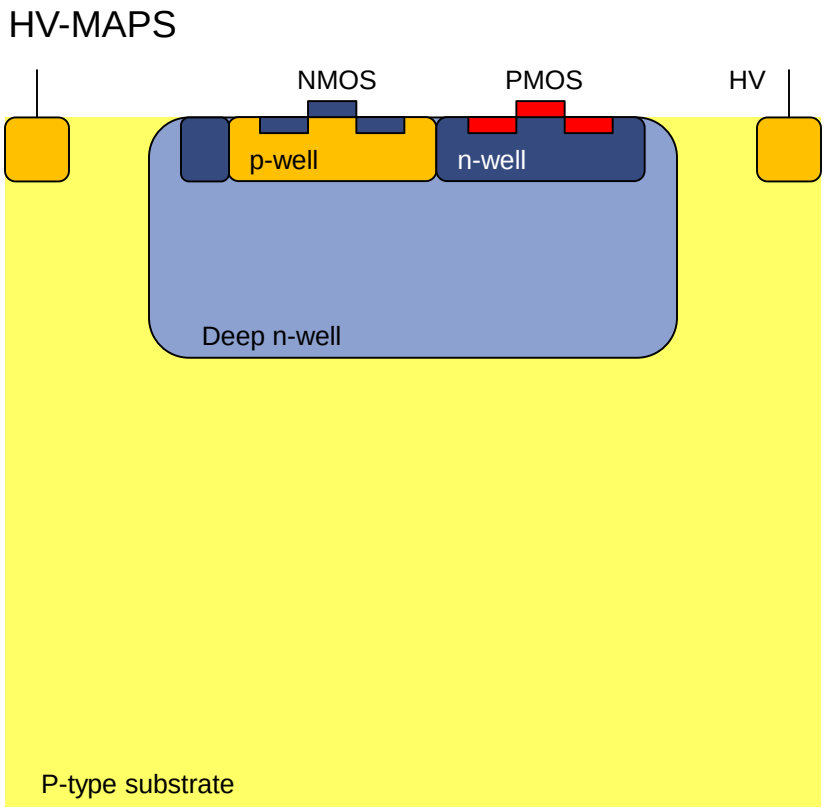


- ASIC and Detector Lab (ADL) develops integrated electronics and sensors for particle physics experiments and medicine (https://adl.ipe.kit.edu/english/)
- Contribution to
- ATALS: Design of FEI3, CMOS R&D
- Belle II: Pixel detector readout electronics
- CLIC: CCPD and monolithic CMOS Sensor development R&D
- Mu3e: HVCMOS pixel sensor development. The detector will be built in 2022/23, commissioning planned for 2023/24
- COMPASS and P2: Pixel detector development
- **CEPC: CMOS detector R&D**
- Member of Belle II, CLIC, COMPASS, Mu3e, LHCb, P2 collaborations
- Developments for medical applications
- Beam monitor based on HVCMOS sensors for ion therapy
- 3D ultrasound tomography – ASIC development
- General purpose ICs (ADCs) and pixel readout ASICs
- Team: 3 scientists, 5 PhD students
- Karlsruhe Institute of Technology – KIT (https://www.kit.edu/english/)

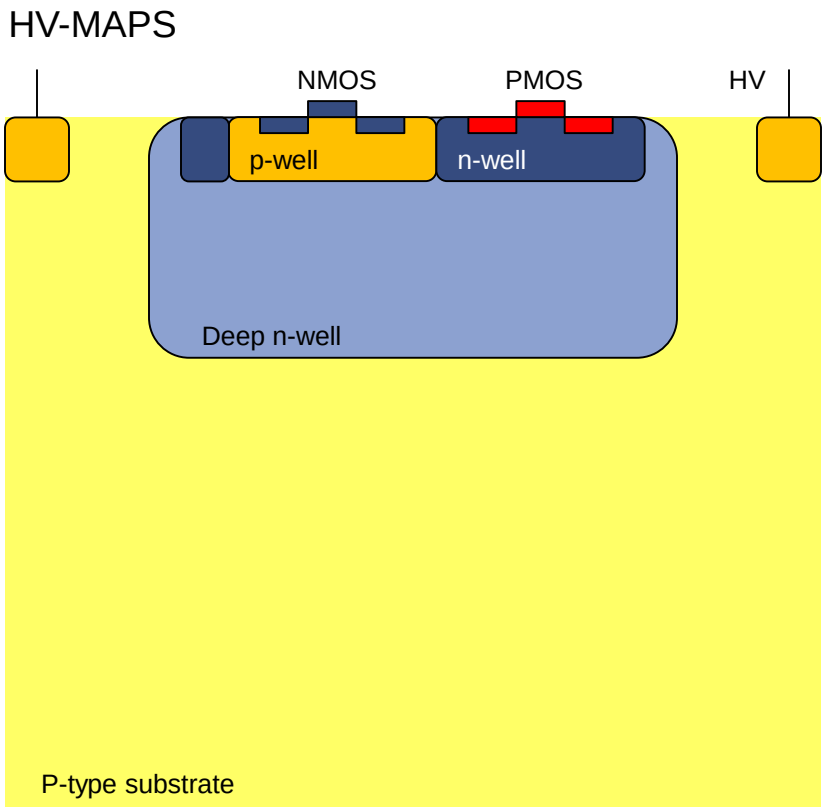
- In last 5 years we have submitted 50 chip designs in in 21 MPW- and 7 engineering runs. We used 9 semiconductor processes



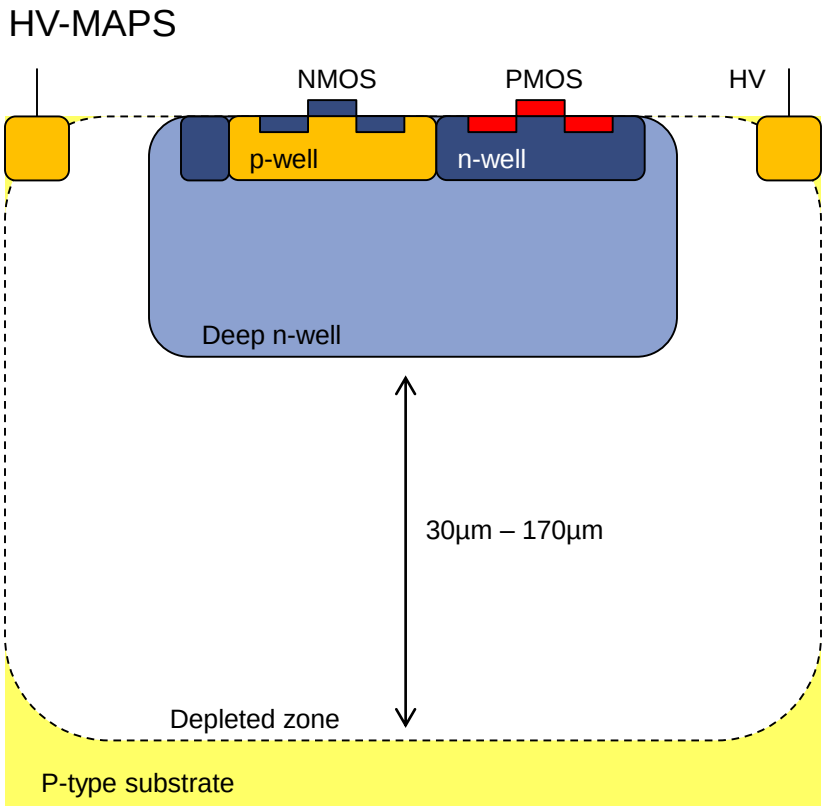
- Our Idea are HVCMOS pixel sensors [1]
- Implemented in standard (HV)CMOS bulk process with triple well structure
- Pixels consist of large electrode with embedded readout electronics



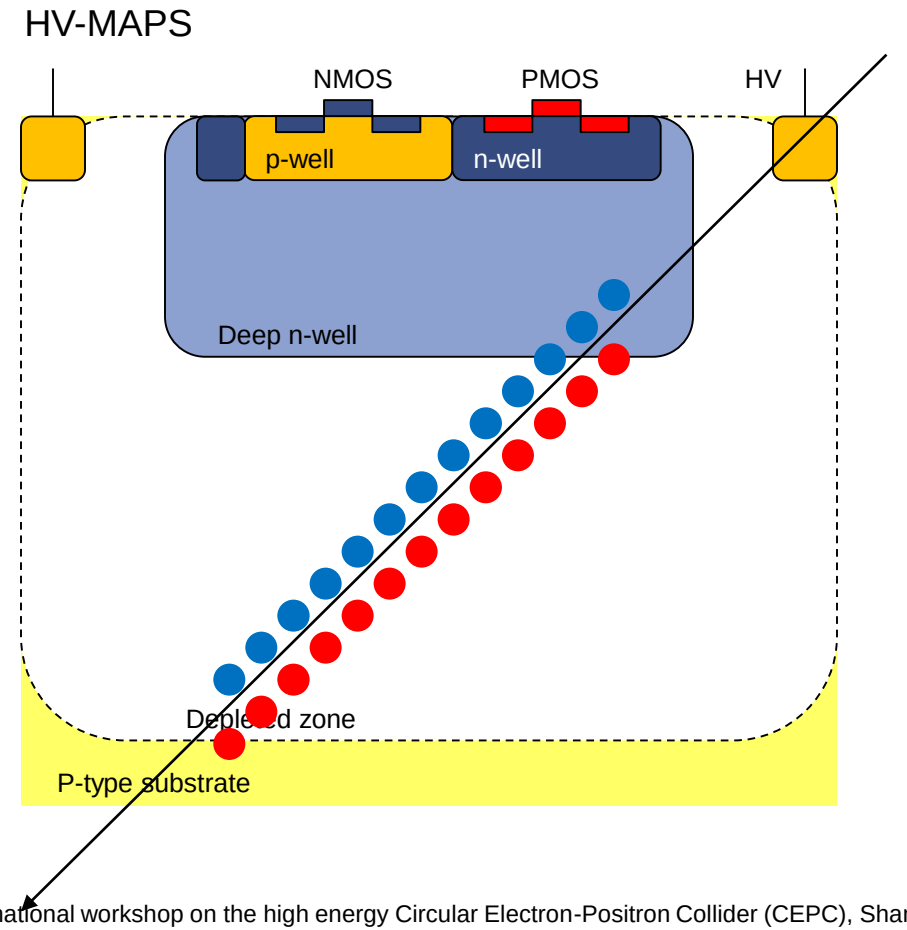
- The deep-n-well fulfils two tasks:
- 1. Local substrate for electronics (isolated from p-substrate)
- 2. Charge collecting electrode



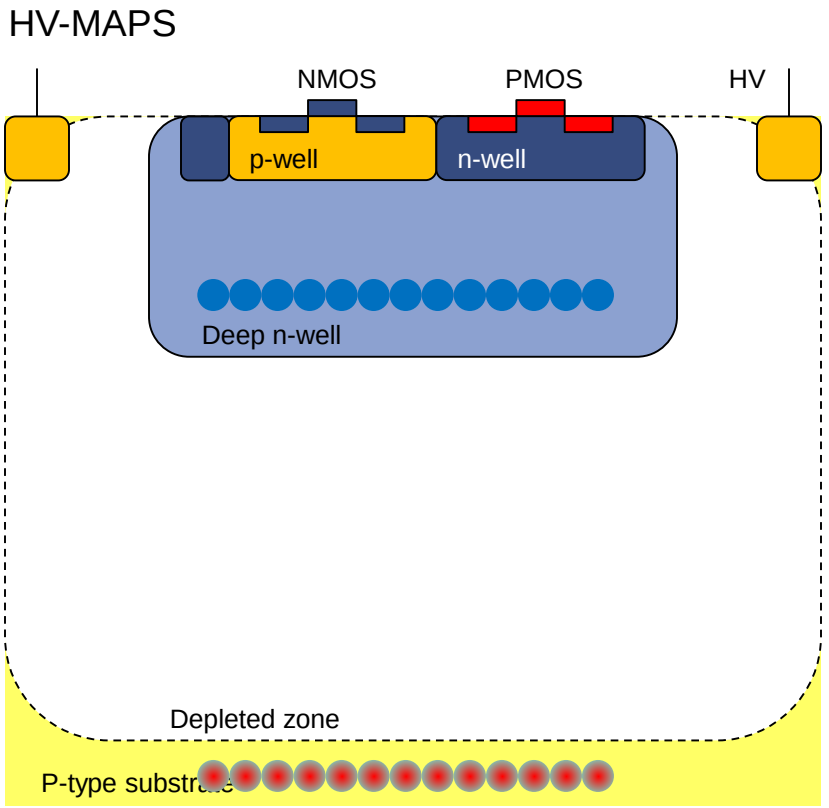
- Deep n-well isolates electronics from substrate
- Biasing of substrate with high voltage possible (typically |V| >= 50V)
  - Example: 300Ωcm substrate and 50V bias => 30µm depletion
  - Much larger depletion is possible with >2kΩcm substrates and higher bias voltages
  - Depletion depth of 166µm was measured for a HVCMOS sensor in [2]



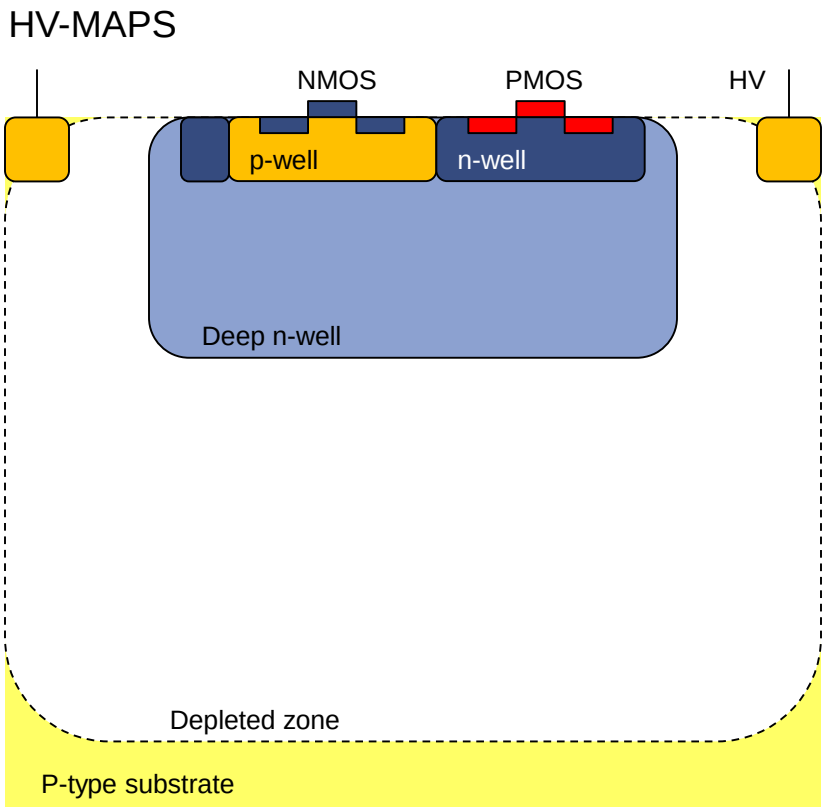
- Average MIP signals are >5000e



- Electron-hole pairs generated by particles are separated quickly in strong E-field.
- => Strong and fast signals when compared to standard MAPS



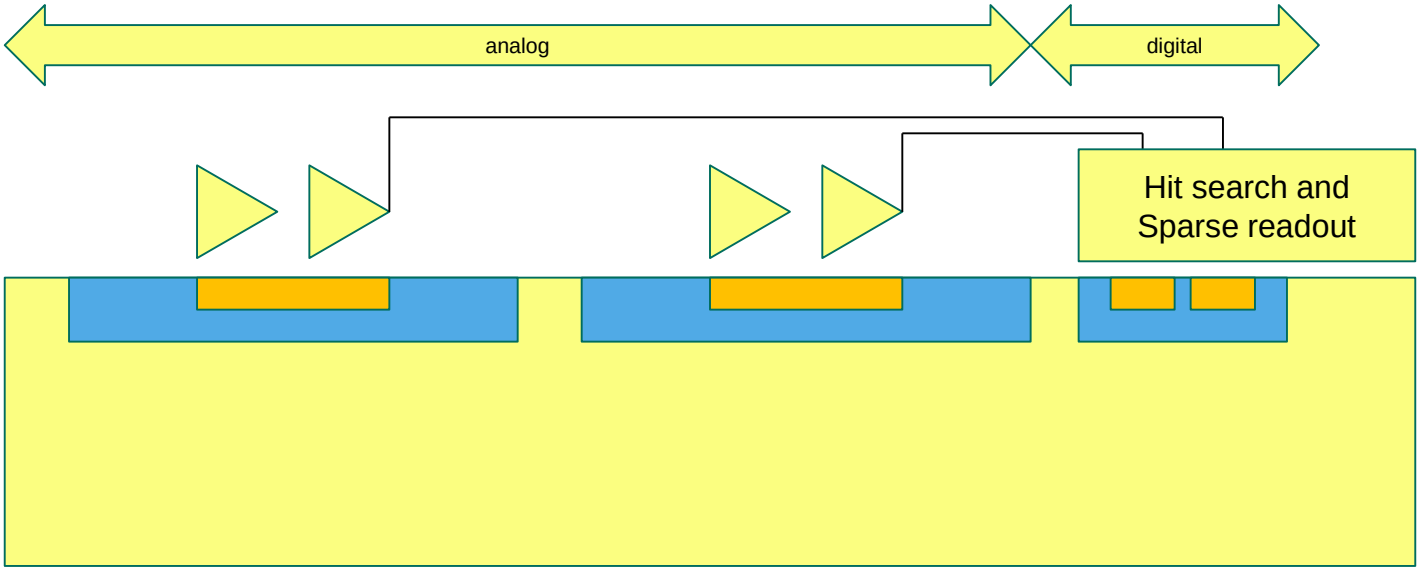
- Radiation tolerant
- Can be implemented in standard IC-processes -> not expensive
- Can be thin
- Can have a high time resolution



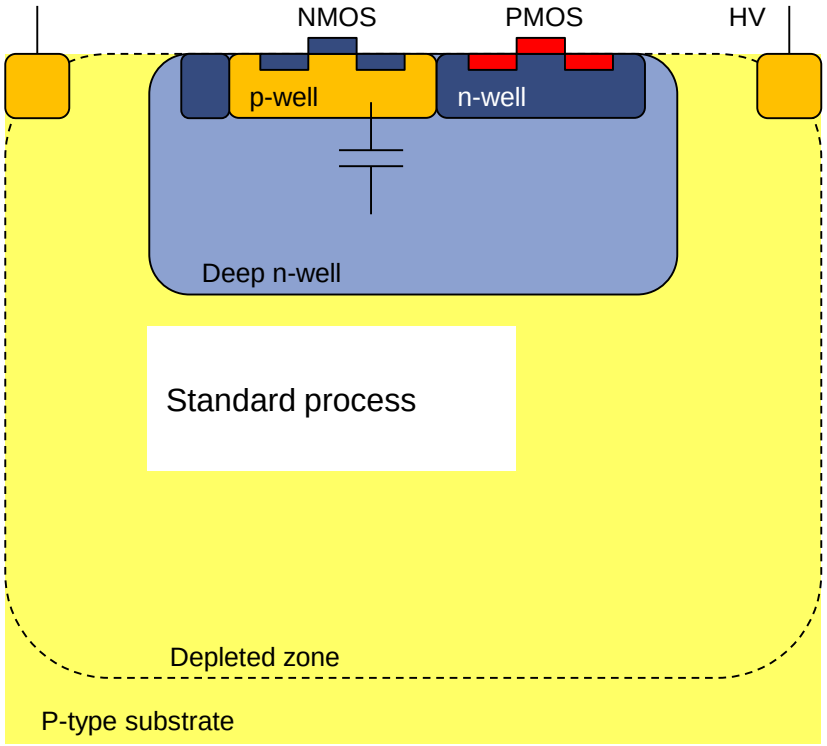
Our sensors: HVCMOS

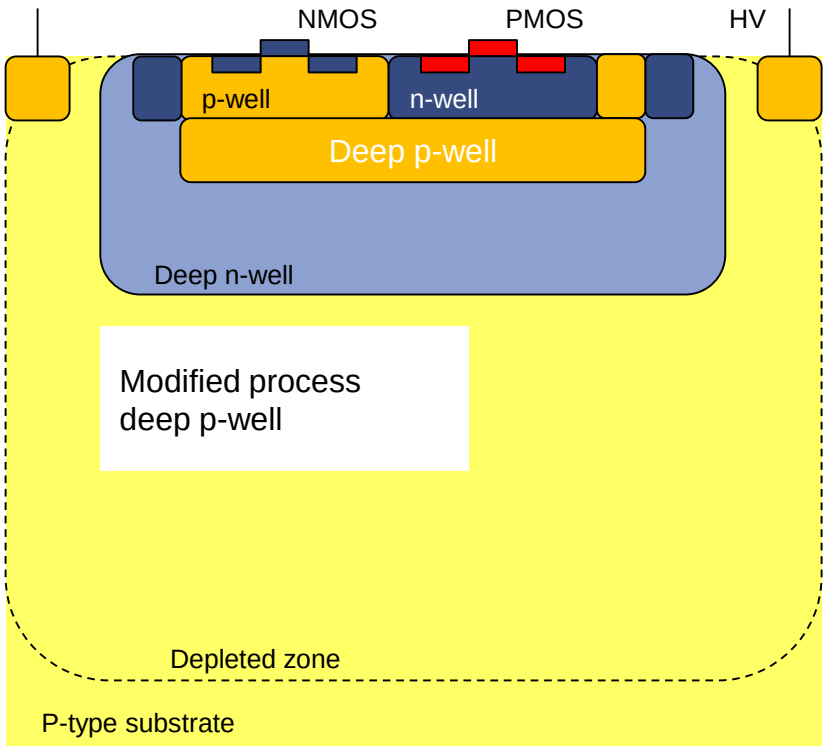
- HVCMOS sensors are compatible with many standard processes
- Implemented in following 8 processes: UMC 65nm, AMS 350nm and 180nm, TSI 180nm, Globalfoundries 130nm, Lfoundry 150nm, IHP SG13S 130nm
- Uniformly doped substrates with resistivity >=10Ωcm have been successfully used
- Since the bias voltage can be very high (some designs achieve ~200V), sensors work even with relatively low res substrates

- Issue crosstalk from PMOS transistors to sensor
- Several solutions used so far:
- 1) Implement NMOS differential logic
  - Drawback: power consumption
- 2) Implement in pixel only amplifier and comparator. Connect every pixel with digital periphery by point to point connections
  - Advantage: Digital circuits are limited to periphery

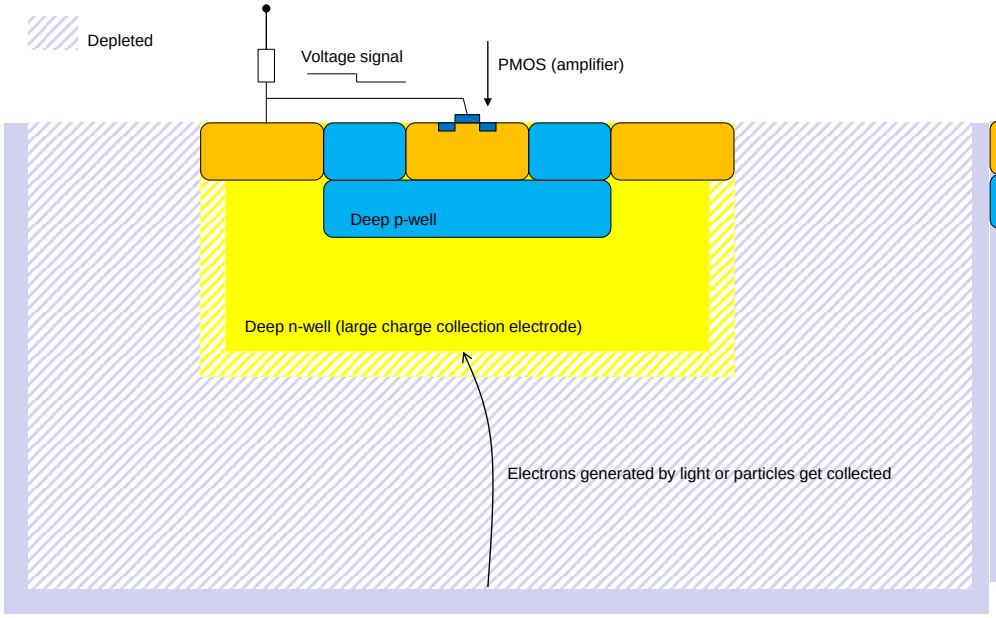


- 3) Use additional deep p-well
  - Drawback non standard process

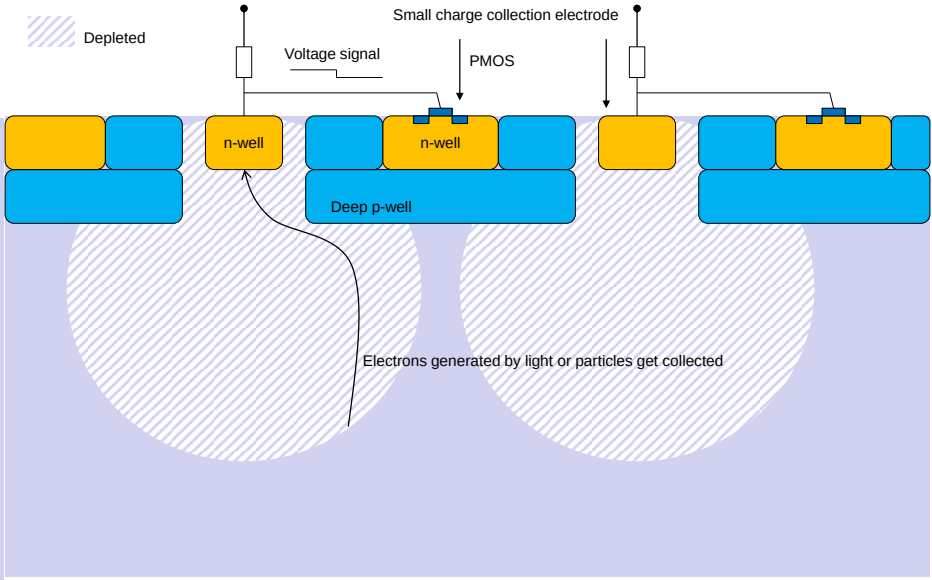




- Alternative DMAPS structure (low fill factor)
- Example: TJ developments
- The structure requires high resistivity substrate and deep p-well
  - Drawback: non standard process

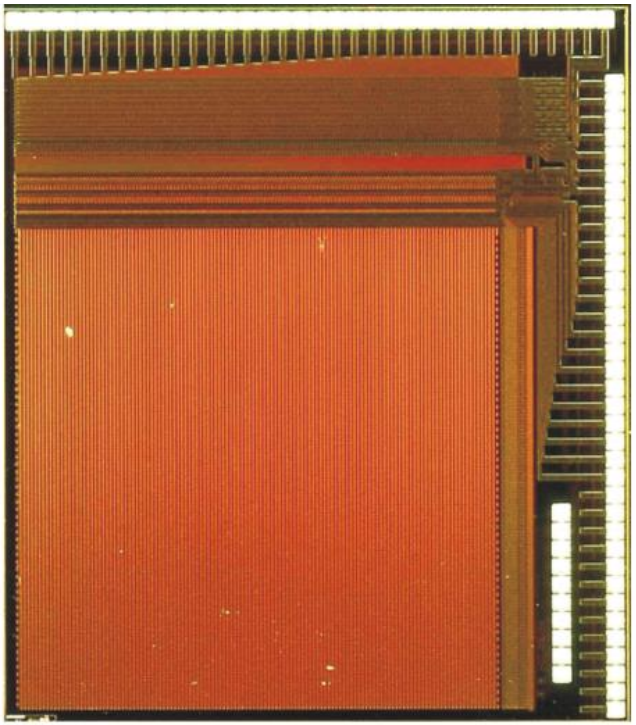


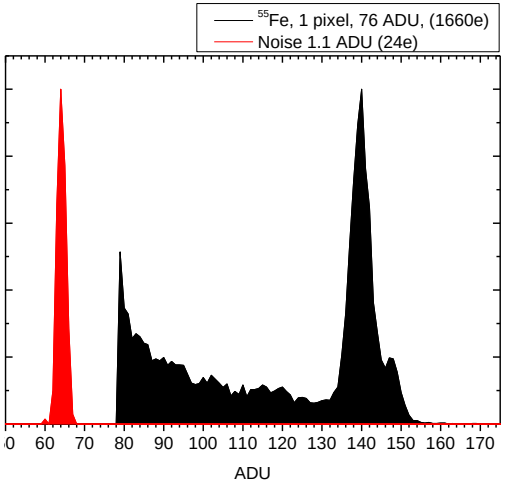
HVCMOS



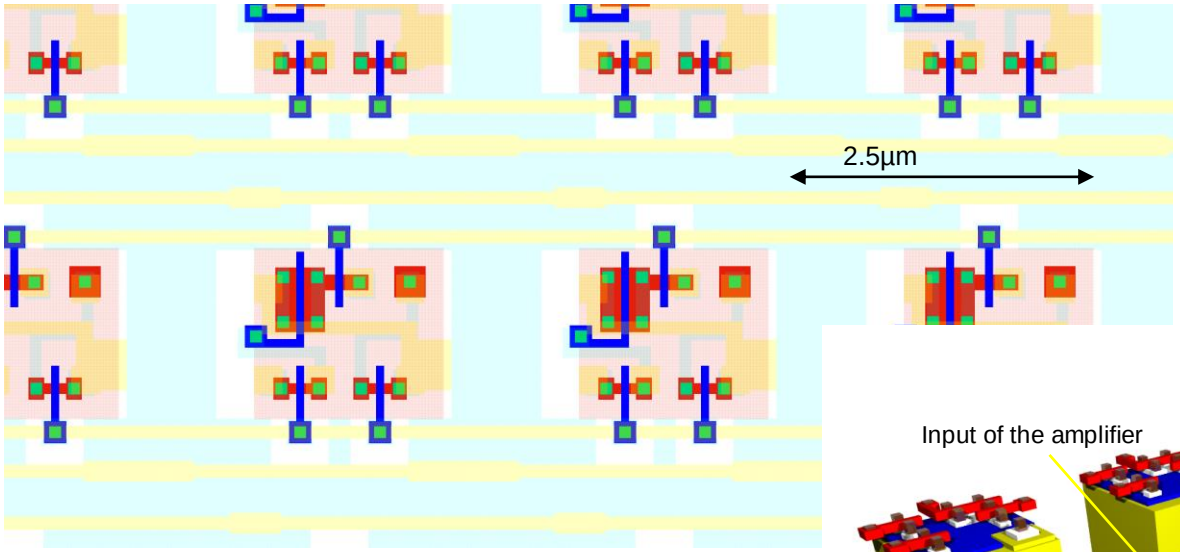
DMAPS

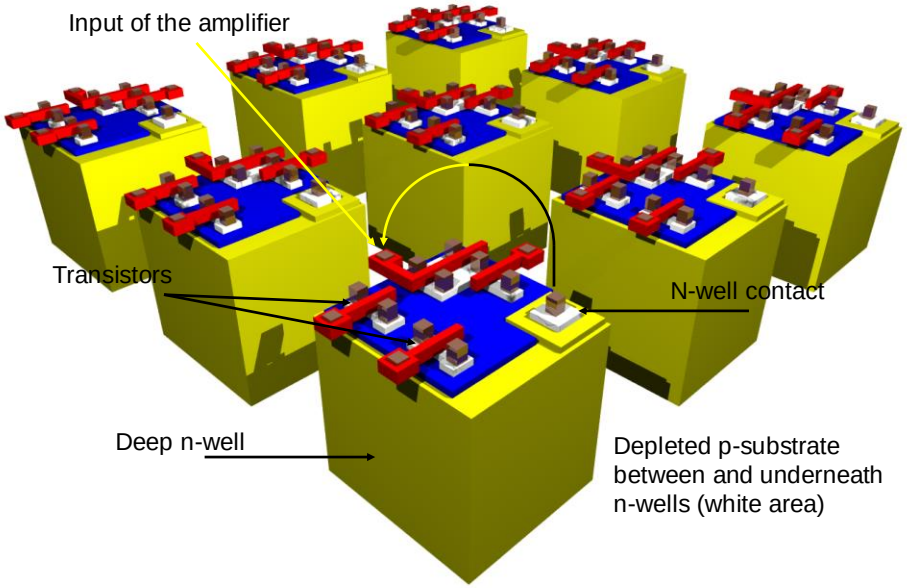
- Development started in 2006 with a R&D phase:
- Some highlights
- HVpixM was implemented in 350nm AMS process on standard substrate of 20 Ωcm
- It is a chip with 128 x 128 pixels of 21µm x 21µm size
- Test beam results: Spatial resolution of 3.1µm after correction for telescope uncertainty [3]





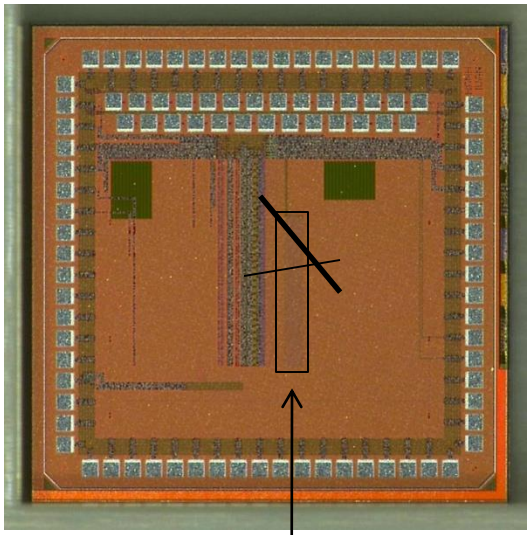
- SDS is the chip with 2.5µm-pixels implemented in UMC 65nm [3]



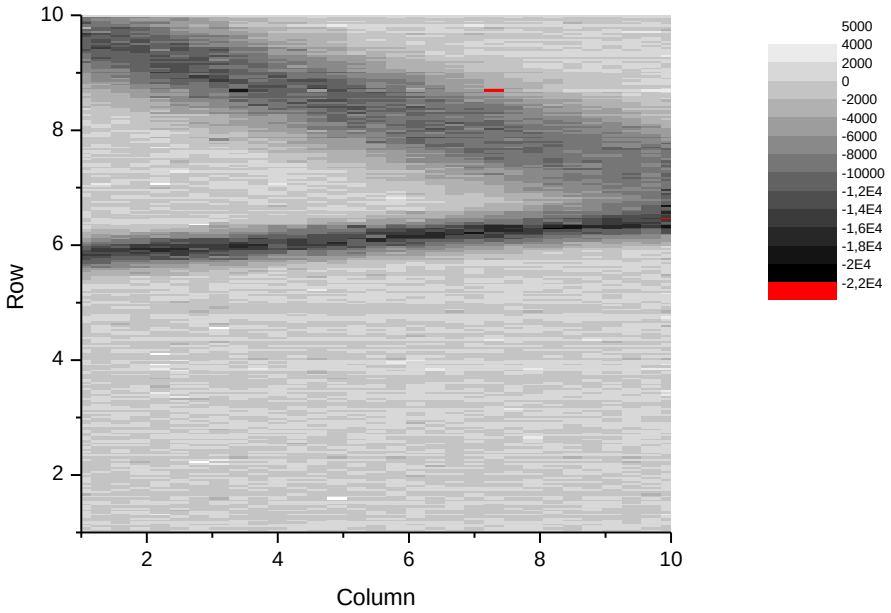


SDS – the detector in 65nm technology - 2.5 µm pixels

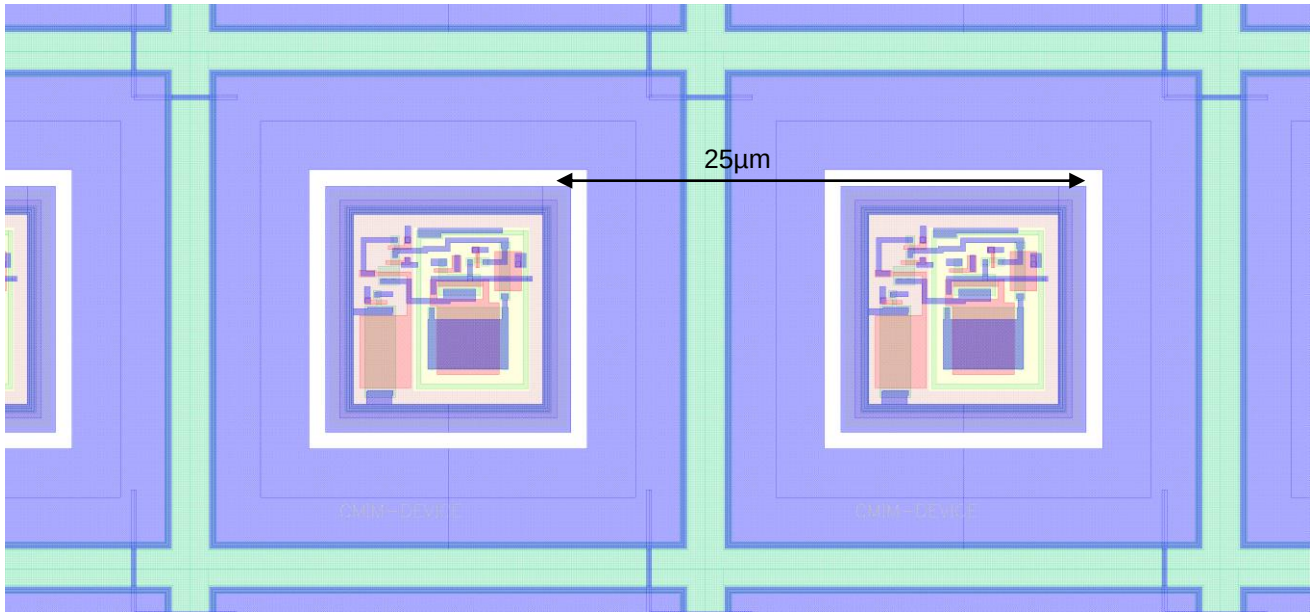
- ^{55}Fe measurement with SDS
- Shadow of 16µm thick golden bonding wire



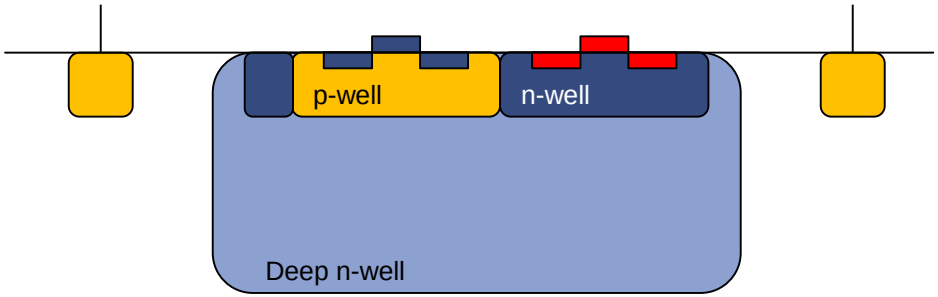
Pixel matrix (32 x 256)

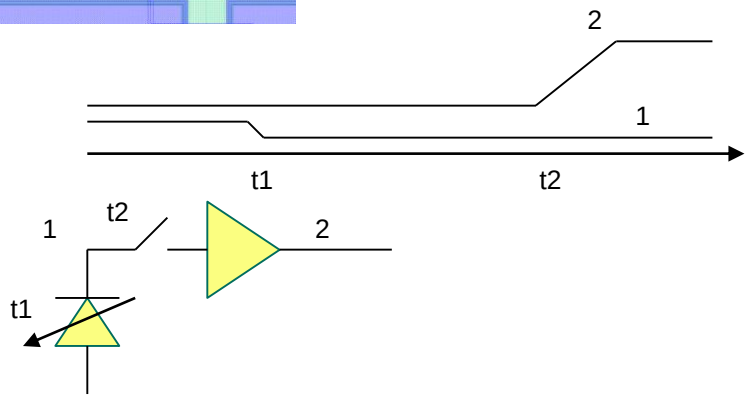


- Hpix (180nm AMS technology): A rolling shutter matrix with 25µm x 25µm pixels, switched charge sensitive amplifiers and correlated double sampling in pixels [4]

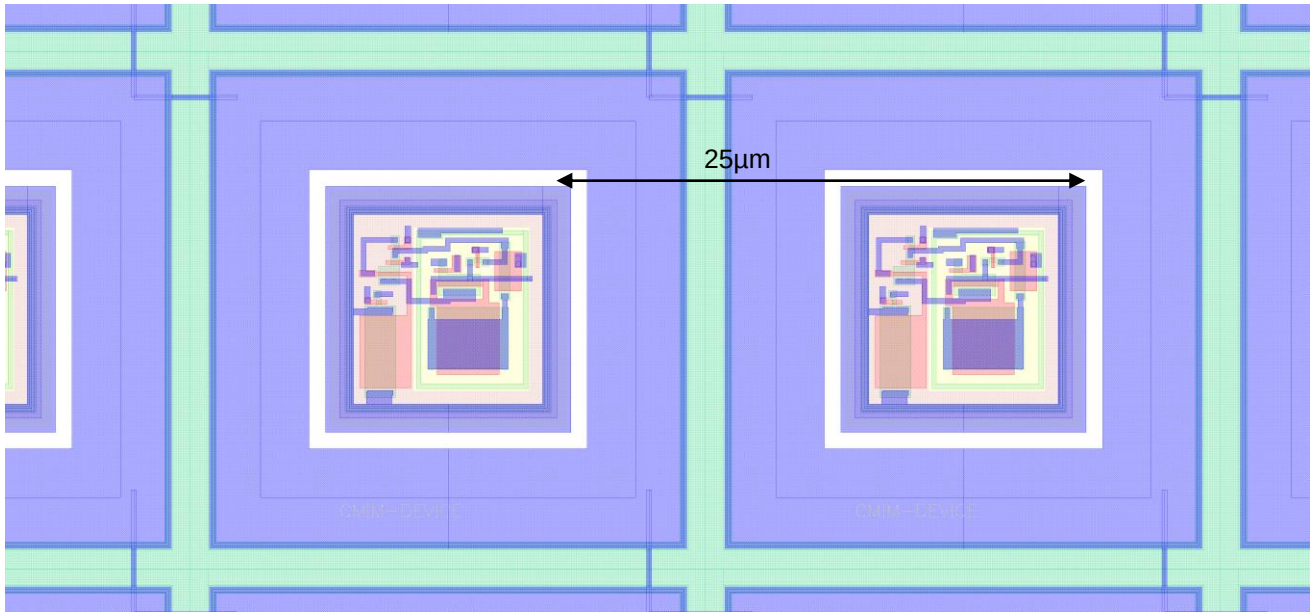


- Rolling shutter readout:
- Pixels integrate charge
- Amplifiers are the most of time inactive
- The output voltage is readout row by row
- The time resolution is the frame time

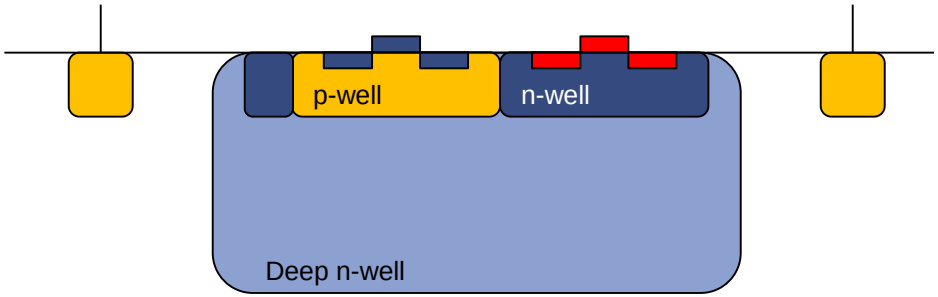


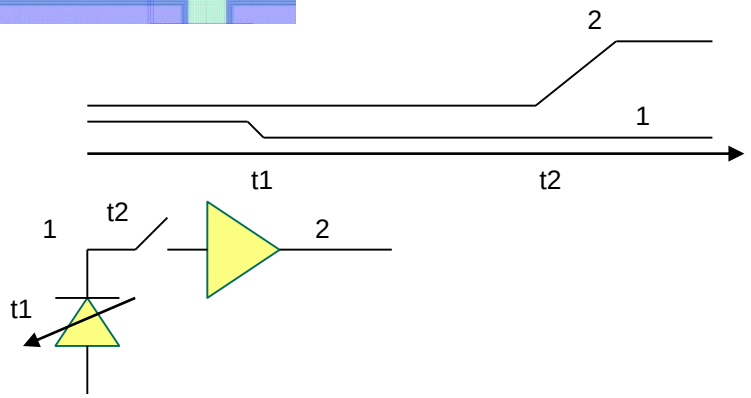


- Hpix (180nm AMS technology): A rolling shutter matrix with 25µm x 25µm pixels, switched charge sensitive amplifiers and correlated double sampling in pixels [4]

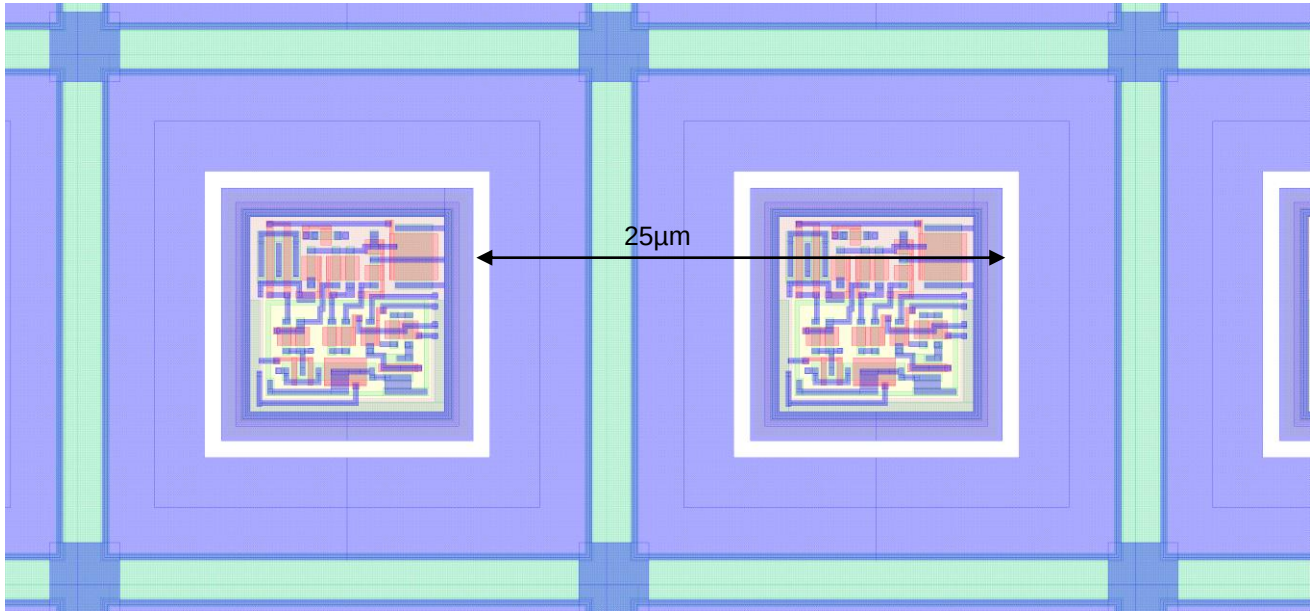


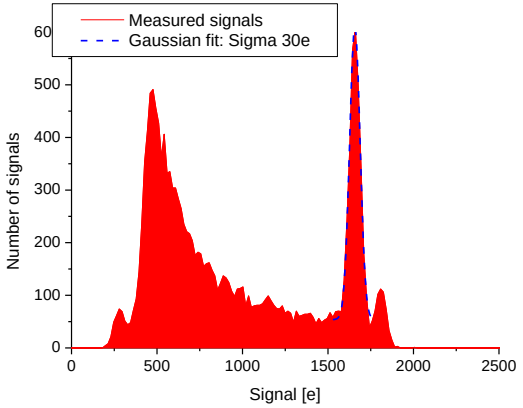
- Rolling shutter readout is slow
- It does not implement smart hit search
- It has advantage that it is immune to digital crosstalk because of pulsed reset

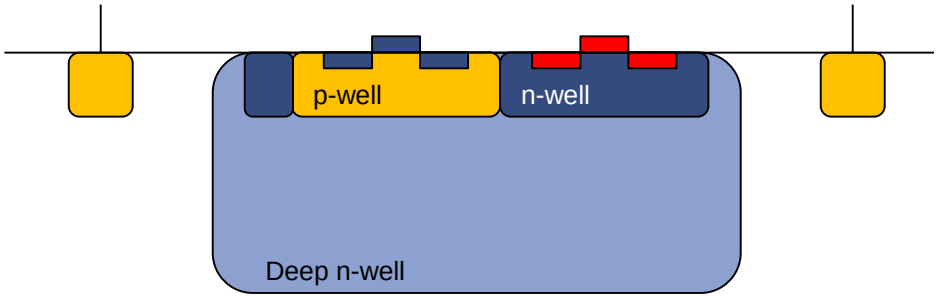


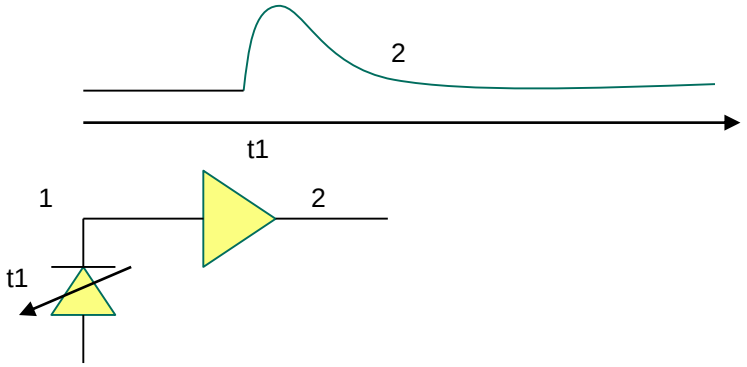


- CLICpix (180nm AMS technology): pixel size 25µm x 25µm, 10Ωcm substrate
- Pixels contain charge sensitive amplifiers and comparators

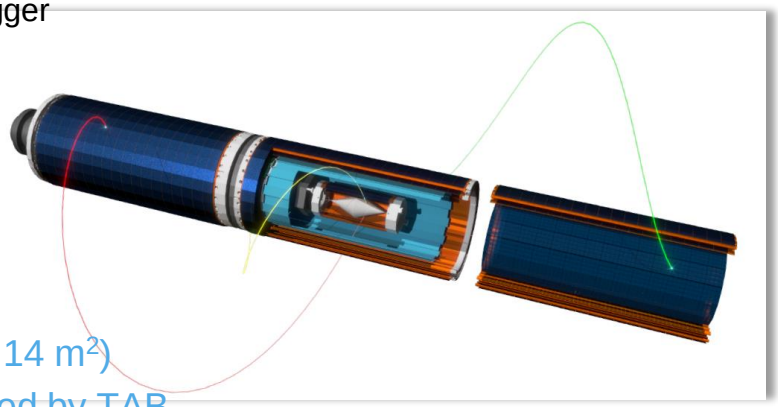




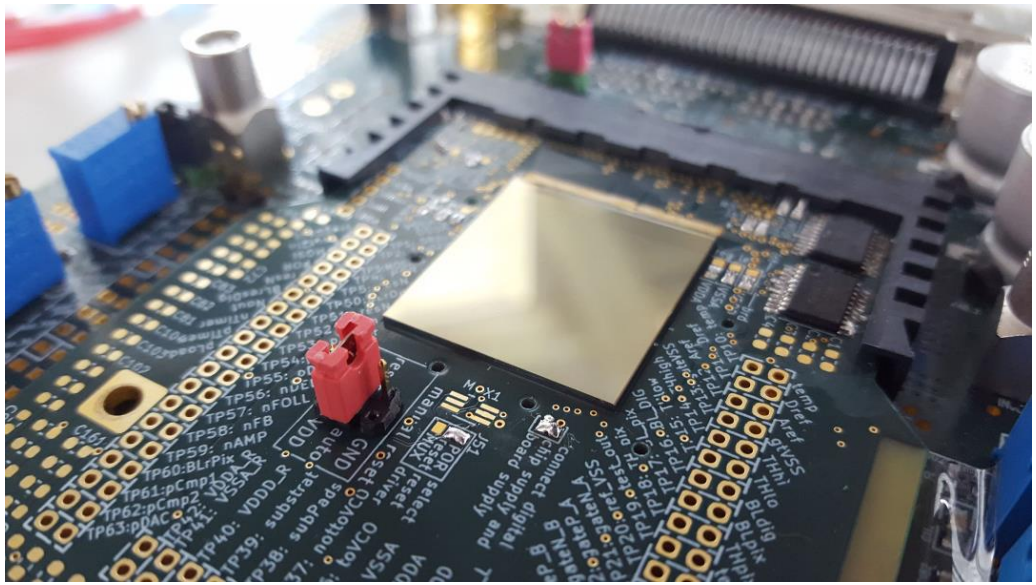




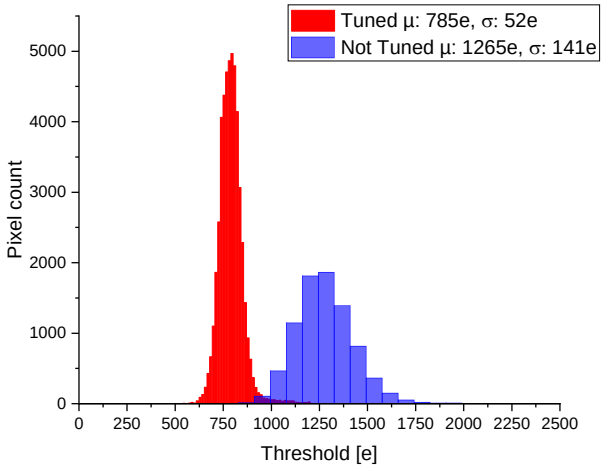
- Mu3e [5] is an experiment at PSI/Switzerland with the goal to search for lepton flavour violating decay
- Fixed target in a high intensity muon beam O(10^8 μ/s)
- Tracking detector (2 inner pixel layers, 2 outer pixel layer, 2 recurl pixel layers)
- Timing detector (scintillating fibres, scintillator tiles)
- Magnet (1T)
- Helium gas cooling
- General requirements
  - Momentum resolution 0.5Mev/c (low momentum particles < 53MeV/c)
  - Vertex resolution ~ 100μm
  - Particle flux 10^9 muon decays/s all hits are readout, no trigger
- Sensor requirements
  - Time resolution below 20ns
  - Detector thickness limited to 50μm
  - High efficiency (> 99 %) and low noise
  - Cooling with helium -> power consumption < 200mW/cm^2
- Detector will use HVCMOS sensors
- 2844 sensor chips of 4cm^2 will be used (total Si area 1.14 m^2)
- The sensors will be glued on flexible PCB and connected by TAB
- The construction of the detector is planned for 2022/23
- Commissioning is planned for 23/24

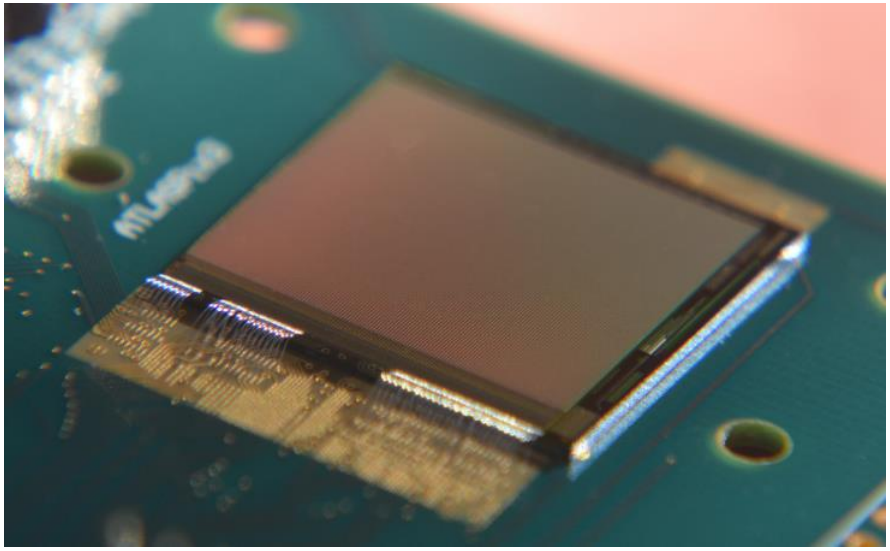


- MUpix10 [6] is a reticle size sensor produced in TSI 180nm HVCMOS process on 200-400Ωcm substrates.
  - 256 x 250 pixels of 80x80µm^2 size. The chip area is 20.66mm x 23.18mm.
  - Pixels contain charge sensitive amplifiers
  - Connected to hit digitizers
  - Two comparators one for time- and one for hit-detection
  - The hit digitizers receive time stamp signal with variable frequencies. Hit time and amplitude can be measured. The chip contains power supply voltage generators that can be used for serial powering scheme. 4 data links (4 x 1.28GBit/s), possible to process 120MHits/s
- The was tested in beam with very good results



- The development for ATLAS started in 2011. After ~20 test chips in 2019 we designed ATLASpix3
- ATLASpix3 [7] is a reticle size HVCMOS sensor implemented in 180nm HVCMOS process of TSI.
- The chip is designed for quad module construction
  - High resistivity substrates of 200-400Ωcm used.
  - 19.8mm x 18.6mm pixel matrix.
  - Chip size 20.2mm x 21mm.
  - Pixel size is 150µm x 50µm.
  - Pixel contains amplifier, comparator and DAC for threshold tuning. The digital part supports triggered and continuous readout. The digital interface uses only two lines command in and data out. Only 3 external voltages are required
- ATLASpix3 is currently being characterised with excellent results. Detection efficiencies of 99.5% have been measured in beam (DESY and PSI). The time resolution after time-walk and binning corrections is 4.5ns sigma. The production yield is about 85% and the power consumption is of the order of 140mW/cm^2

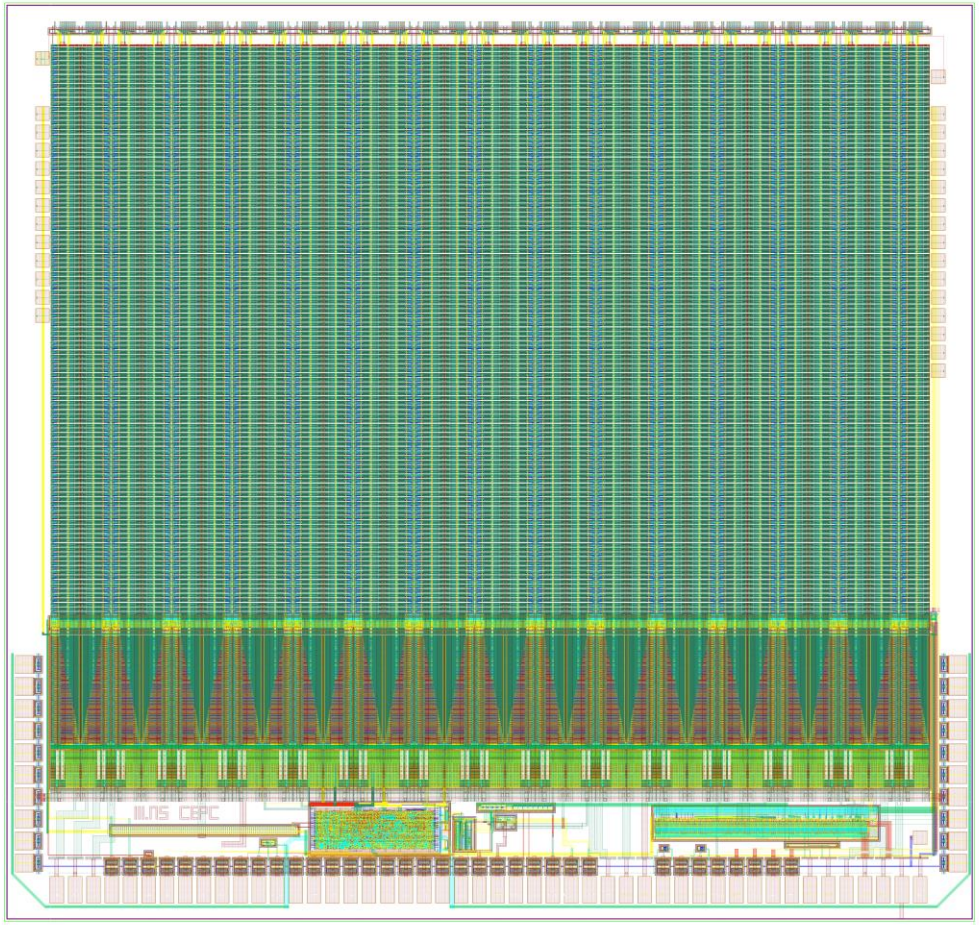




- The KIT group collaborates with the University of Geneva on the development of HV-CMOS sensors in SiGe BiCMOS technology SG13S of IHP
- The technology SG13S allows production of SiGe heterojunction bipolar transistors (HBTs) and CMOS transistors on the same substrate
- Time resolutions ~ 50ps RMS are possible with particle sensors implemented in the IHP process [8]

- Since 2019 we collaborate with CEPC-groups
- Team: Ivan Peric, Rudolf Schimassek, Richard Leys, Hui Zhang
- ATLASpix3, PCB design and test software
- We started CEPC tracking sensor development

- 1) CEPCpix: A test matrix with 25µm x 160µm HVCMOS pixels (high fill factor) for tracking sensor
- The pixels use low-power amplifiers and comparators
- A daisy chain readout scheme implemented. It reduces the number of data links in the case of low occupancy. The chip passes the data to its neighbour. The last chip in the chain sends all the data via fast link. The scheme uses handshake protocol and FIFO



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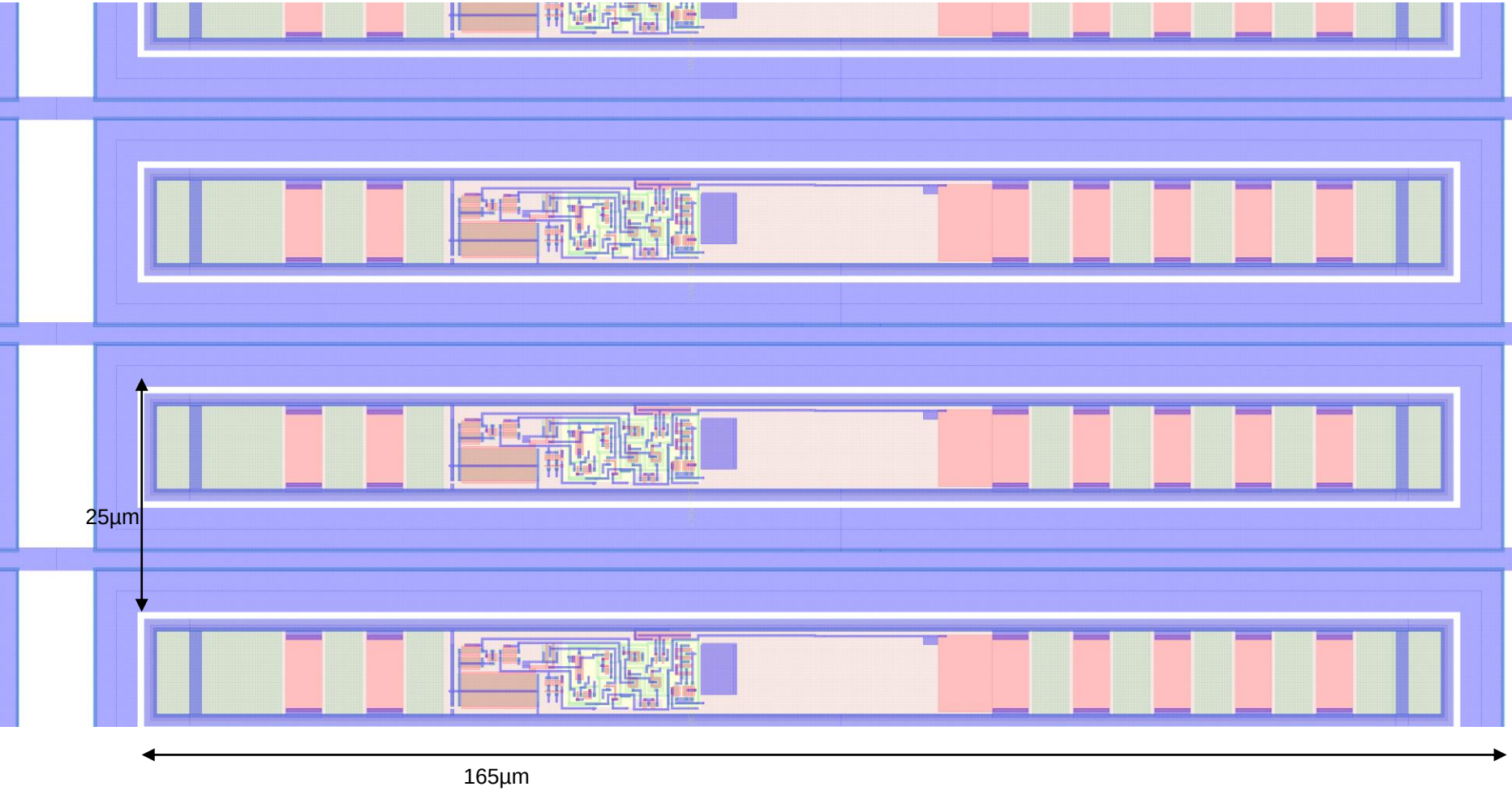
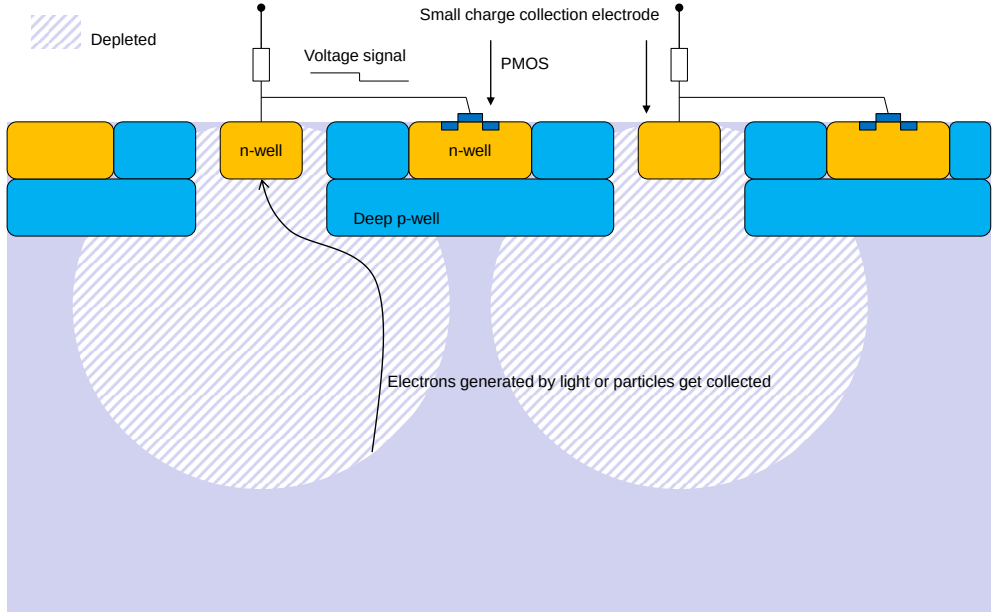


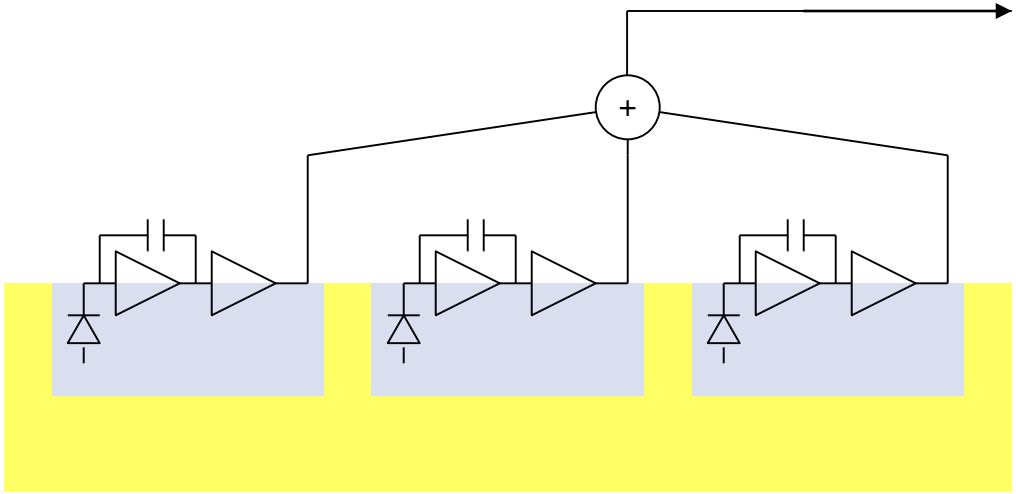
- H25: A test matrix with DMAPS-like pixels (low fill factor) that use deep p-well. The pixel size is 35µm x 25µm



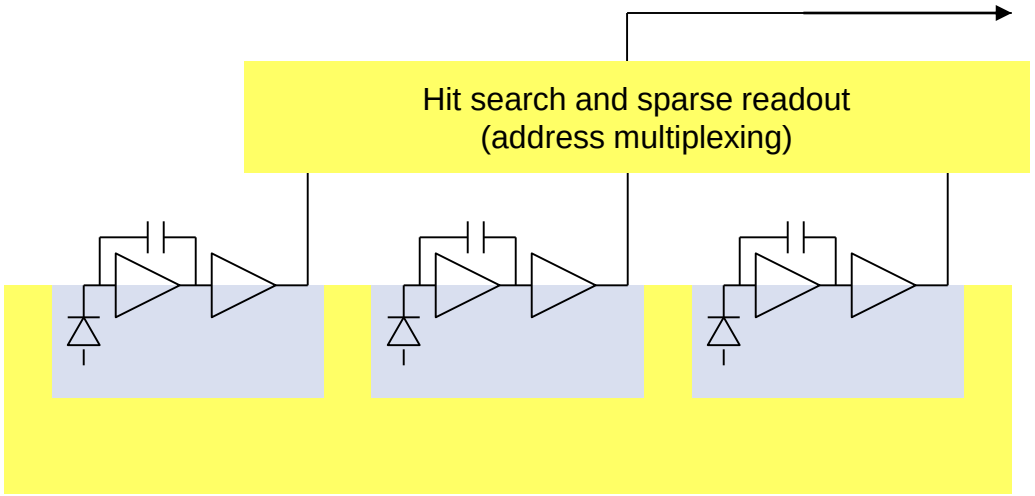
- CEPC pixel detector requirements: high spatial resolution and low power consumption. The rate is low and high time resolution is not required
- Spatial resolution 2.8µm => for vertex sensor 16µm x 16µm pixels, (20µm x 20µm should be fine if charge sharing and analog information is available) a readout time of less than 10µs, power consumption better than 50mW/cm^2, rate 4.2 particles/680ns/cm^2
- These requirements are different than in the case of hadron colliders and Mu3e
- ATLAS requirements: high time resolution, high rate capability high radiation hardness
- Mu3e requirements: high rate capability, high time resolution and low power consumption

- Vertex sensor
- Possibility 1: Sensor with rolling shutter readout, switched amplifier and in-pixel CDS
  - Example: HPixel in 180nm AMS
  - Challenge: Reduce pedestal dispersion
- Possibility 2: Sensor with continuous (low power) amplifier
- Possibility 2A: High fill factor design with “analog” pixels (contain amplifier and comparator). Digital circuits (hit digitizers) placed on the chip periphery
- Problem: Difficult to connect small pixels
- Estimated minimum pixel sizes that can be 1-1 connected to periphery
  - 180nm TSI: 55x55µm
  - 150nm Lfoundry: 60x60µm
  - 130nm IHP: 55x55µm
  - 65nm UMC: 30x30µm
  - These numbers assume a matrix height of 1.8cm and readout on one side (M1, M2 and 0.5 M3 reserved)
- A solution is to add pixel outputs
  - Example: 31 pixel outputs multiplexed to 5 address lines
- Disadvantages of 2A:
  - 1) Ghost hits - probably not a problem because of low occupancy
  - 2) Comparator implementation without p-well a bit tricky
- Sensor example that use address adding: CCPD53 [10]
- 20µm x 20µm pixel size with cont. readout is possible in 180nm HVCMOS technology of TSI (3.5 routing layers) when address adding is used

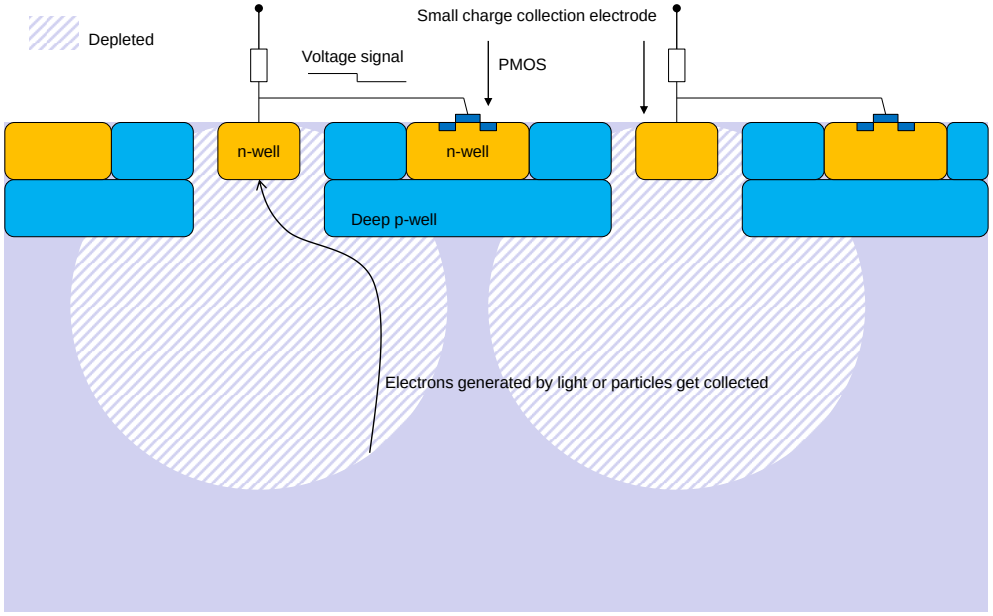
- Address adding



- Address multiplexing (hit search) would avoid problem of ghost hits
- Problem to solve: crosstalk from digital circuits to pixels
- One solution: pulse reset and pulsed filtering/zero suppression



- Possibility 2B: Low fill factor sensor (DMAPS) with digital circuits in pixel (sparse readout)
- 20µm x 20µm is possible in 180nm technology as well
- Disadvantages: DMAPS require deep p-well and a high resistivity substrate because the bias voltage is limited to ~20V. Reduced technology choice



- Next steps:
- Characterize CEPCpix
- Characterize H25
- Determine the spatial resolution achieved with 25µm pixels
- Measure power consumption
- Test daisy chain readout
- Evaluate rolling shutter readout

Summary

- ADL (KIT, Karlsruhe, Germany) develops CMOS monolithic sensors and ICs for particle physics, since 2019 also for CEPC
- In 2020 we designed and submitted a few sensor designs
- 1. HVCMOS matrix CEPCpix for tracking detector with 25µm x 165µm pixels
  - Optimized for low power consumption
  - Daisy chain readout
- 2. DMAPS matrix H25 with 25µm x 35µm pixels
- Planned work:
- Design of larger CEPCpix sensor for tracker
- We will investigate several possibilities
- 1. Using HVCMOS structure (high fill factor) with/without deep p-well
- 2. Using DMAPS structure (low fill factor)
- Our designs can be implemented in different CMOS-technologies

- Thank you!

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