Requirements of TPC to TDAQ

Preliminary estimation

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Overview of TPC concept

TPC detector concept:

- **Under 2-3 Tesla magnetic field (Momentum resolution: ~10^{-4}/GeV/c with TPC standalone)**

- **Large number of 3D space points(~220 along the diameter)**

- **dE/dx resolution: <5%**

- **~100 μm position resolution in rφ**

    - **~60μm for zero drift, <100μm overall**

    - **Systematics precision (<20μm internal)**

- **TPC material budget**

    - **<1X_0 including outer field cage**

- **Tracker efficiency: >97% for pT>1GeV**

- **2-hit resolution in rφ : ~2mm**

- **Module design: ~200mm×170mm**

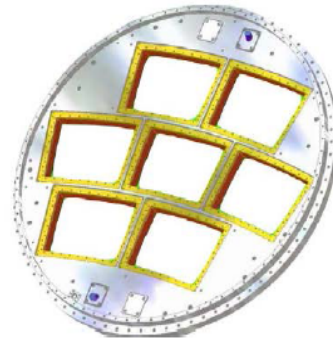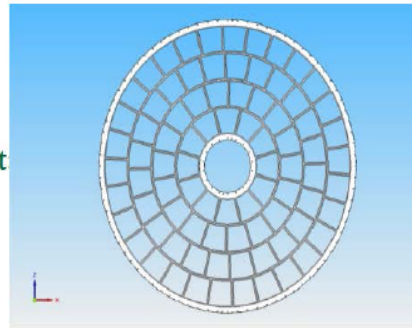- **Minimizes dead space between the modules: 1-2mm**
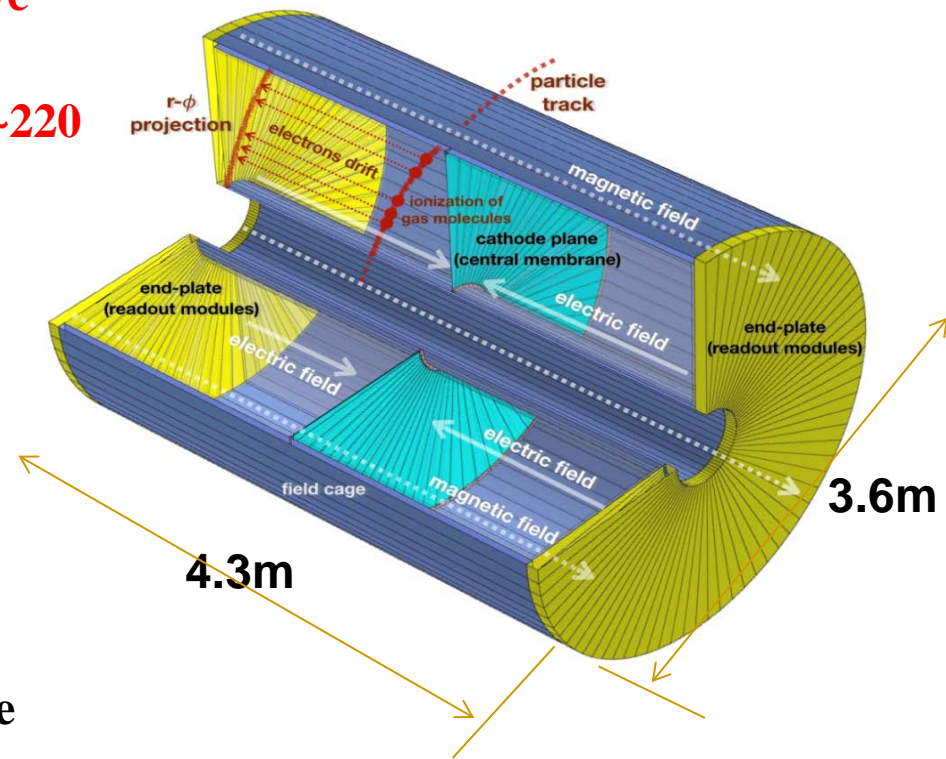
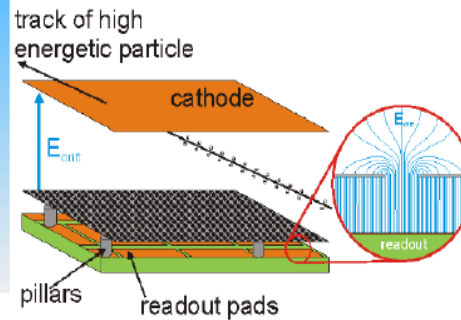TPC detector concept

Overview of two readout options

Pad TPC and Pixel TPC

Pad TPC for collider

- Active area: $2 \times 10m^2$
- One option for endplate readout
  - GEM or Micromegas
  - 1×6 mm^2 pads
  - 10^6 Pads
  - 84 modules
  - Module size: 200×170mm^2
  - Readout: Super ALTRO
  - CO_2 cooling

Pixel TPC for collider

track of high energetic particle

cathode

E_{drift}

pillars   readout pads

E_{ave}

readout

For Collider @cost:
But to readout the TPC with
GridPixes:
→100-120 chips/module
240 modules/endcap (10 m^2)
→50k-60k GridPixes
→ 10^9 pixel pads

Benefits of Pixel readout:

- Lower occupancy

→ 300 k Hits/s at small radii.

→ This gives < 12 single pixels hit/s.

→ With a read out speed of 0.1 msec (that matches a 10 kHz Z rate)

→ the occupancy is less than 0.0012

- Improved dE/dx

  → primary e- counting

  - Smaller pads/pixels could result in better resolution!
  - Gain <2000
  - Low IBF*Gain<2
  - CO_2 cooling

Requirements of TPC to TDAQ - I

Reference info from ALICE TPC(in operation), STAR TPC(in operation) and ILD TPC(future)

Pads TPC (example)

- ❑ There is full size TPC detector with the outer radius of 1.8m and inner radius of 0.3m. All of the two endplate mounted in two sides.

- ❑ Every channel will be connected in the small pad(1mm*6mm), thus the total number of channels is 5000/module*84/endplate*2=840K channels.

- ❑ Each ASIC has 128 channels and there is 6.5K ASIC chips integrated with the FEE and DAQ.

- ❑ The bunch crossing (BX) rate is 40 MHz and we need to deal with every BX at one IP in circular collider.

- ❑ Requirements of FEE readout

Parameter	Specification
Noise	<200e
Conversion gain	>15mV/fC
Peaking time (defaul)	100ns
Non lineartiy	<1%
Cross talk	<0.3%
Dynamic range	>2000
Power consumption	<5mW/ch

Requirements of TPC to TDAQ - II

Reference info from ALICE TPC(in operation), STAR TPC(in operation) and ILD TPC(future)

Pads TPC (example)

- There are average 80 particles/ BX. Each particle produces 600 channels of signal. The noise rate is 10^{-4}/ BX / channel. Thus the number of channels with hit (signal & noise) = $80*600 + (840K-80*600) *10^{-4}$= 48K/ BX.

- Preliminary estimation of raw data size : Data will be zero-suppressed at each ASIC. There are some initial information of 2-byte header whether or not the ASIC has any hit. For each hit we use a 7-bit channel ID, and 9-bit ADC, i.e. 2 bytes / hit. So the useful data rate is $6.5K*2 + 48K*2 = 22K$ bytes/BX. All of the total raw data rate is 13.8GB/s.

- Some additional information of raw data should be included. (Example: Slot number, crate number, board number, gas flow, temperature and humidity…)

- Trigger and triggerless options