Requirements from the Vertex Detector for TDAQ

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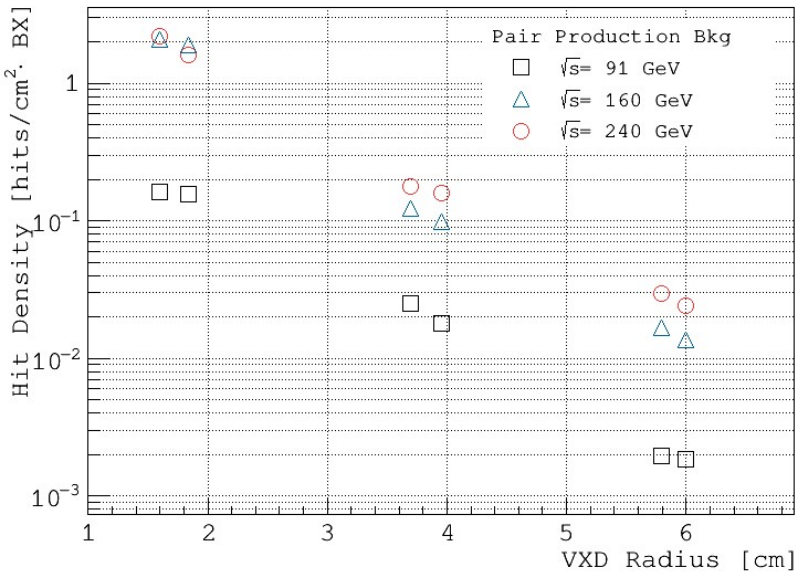
Hit rate Calculation for the CEPC vertex

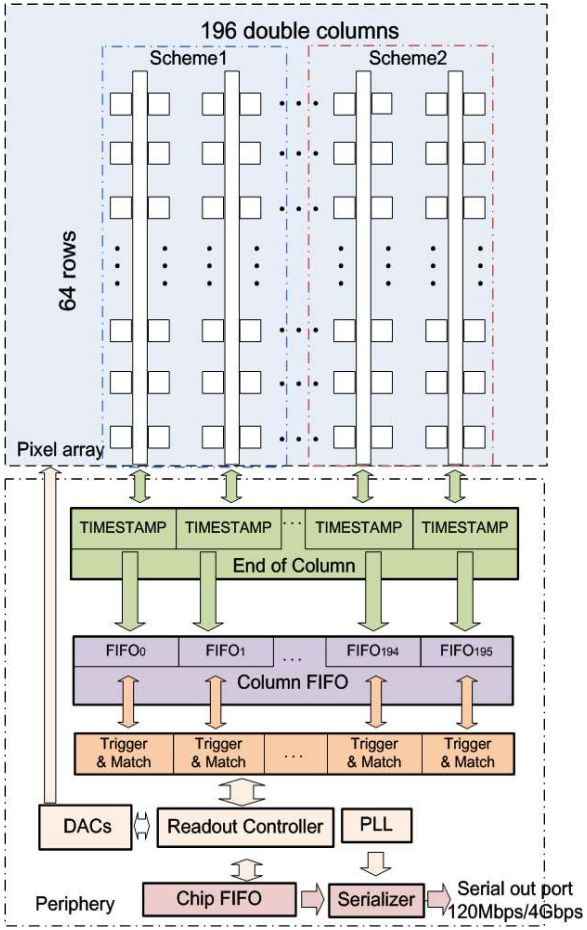
- **Bunch spacing**
  - **Higgs: 680ns; W: 210ns; Z: 25ns**
  - **Meaning 40M/s bunches (same as the ATLAS Vertex)**
- **Hit density @ different radius**
  - **Higgs: 2.5/0.2/0.03 hits/bunch/cm^2**
  - **W: 2.5/0.13/0.02 hits/bunch/cm^2**
  - **Z: 0.2/0.03/0.002 hits/bunch/cm^2**
- **Cluster size: 3pixels/hit**
  - **Epi- layer thickness：~18μm**
  - **Pixel size：25μm×25μm**

Background Hit Density From the CDR of CEPC



- **The (highest) hit rate: Higgs 11 MHz/cm^2, W 36MHz/cm^2, Z 24 MHz/cm^2**
  - **Outter layers have much less (background) hit rate**
- **Pixel array: 1024 rows×512 cols, full size chip sensitive area: 1.28cm×2.56cm (~3.28cm^2)**
  - **Minimum address width: 19bits**
- **(Highest) Hit rate: 120MHz/chip @W**

Event driven readout: architecture of the TaichuPix



- **Simplified column-drain readout:**
  - **Each double column shares a common Fast-Or bus for hit indication**
  - **Common 8bit- time stamp register @40MHz will record the hit arrival time**
  - **Hit pixels in the same cluster will share a common time stamp as the Trigger ID**
- **Event-driven readout in TaichuPix**
  - **Priority based data driven readout**
  - **Modification: time stamp is added at EOC whenever a new fast-or busy signal is received**
  - **Dead time: 2 clk for each pixel (50ns @40MHz clk), negligible compared to the average hit rate**
  - **32bits/event with ignorable data loss (@CEPC's hit rate)**
  - **Trigger/Triggerless compatible by configuration**
- **Concerning the TDAQ**
  - **Intrinsically zero-suppression**
  - **in trigger mode, a ±3LSB trigger error window was given, the output data can be further suppressed by higher level trigger**

TaichuPix of the vertex detector for TDAQ

- **Readout bandwidth**
  - **Note: all calculated at the W running mode with the highest hit rate (~120MHz/chip), other modes generate less data volume**

Mode	Data rate	Interface	Power @full speed	Trigger latency
Trigger	160Mbps/chip	LVDS	100mW/cm2	3us @chip level
Triggerless /continuous	4Gbps/chip	CML	150mW/cm2	Continuous

- **Total area of the CEPC vertex detector: ~1.5m^2 (about 5000 chips)**
  - **Total data volume of the vertex detector depends on the final layout of the ladder and chips/ladder**
  - **4Gbps/208Mbps/32Mbps @Triggerless mode at different radius**
- **Expected extra expense with backend electronics**
  - **Longer trigger latency is expected**
    - **Chip data may be sent at triggerless/continuous mode to be registered in backend**
    - **The real trigger decision may happen at the backend electronics**
  - **Longer time stamp bits for longer FIFO for possible longer**
    - **Longer data width for each event/Trigger ID**
  - **Necessary communication expense with DAQ**

TaichuPix's preference for the trigger

- **TaichuPix will not output information to help for trigger decision, but only receive trigger from other detectors**
- **Concerning data speed, power consumption, and complexity of the frontend flex cable, trigger mode is much more preferred than triggerless**
  - **Tcpx still keeps compatible for both trigger/triggerless, up to now**
- **Requirement for high level signals**
  - **System clock should be synchronized with bunch crossing clock (e.g. 40MHz @ Z pole)**
  - **Trigger from trigger decision, ~ 3us trigger latency**
    - **Larger trigger latency will result in larger data volume**
- **Note： for rolling shutter readout(e.g. Jadepix @MOST1), it is hard to estimate the data volume at the current stage**
  - **Depends on the final pixel size, zero suppression strategy, trigger mode…**

Backup information for useful calculation

Table. 1 The hit density of CEPC

Parameter	Unit	Higgs	W	Z
Bunch spacing	**ns**	**680**	**210**	**25**
Hit density	**hits/bunch/cm^2**	**2.5**	**2.5**	**0.2**
	hits/bunch	8.2	8.2	0.66
	pixels/bunch	25	25	2
Hit pixel rate	MHz/cm^2	11	36	24
	MHz/chip	36	120	80
Chip data rate (triggerless)	Gbps	1.15	3.84	2.56
	MHz/32bit	36	120	80

- **The hit rate: Higgs 11 MHz/cm^2, W 36MHz/cm^2, Z 24 MHz/cm^2**
- **Suppose the pixel array size is 512rows*1024cols, 25um*25um pixel size, and 1.28cm*2.56cm pixel array area**
- **→ Hit rate: 120MHz/chip, or 225Hz/pixel (average), 120kHz/col (ave)**
- **Every hit has 27~32bits (async): col addr 9bits (512), row addr 10bits (1024), time stamp ~8bits (suppose 40MHz clock, covers 6.4us time region)**
- **If triggerless, all the raw hit data should be sent off chip (most are background events)**
  - **The data rate: ~32bits*120MHz= 3.84Gbps**
- **In trigger:**
  - **Data rate@W: ~32bit * 25pixels/bunch * 20kHz trigger rate * 7 error windows= 112Mbps ~160Mbps**
  - **Data rate@Z: ~32bit * 2pixels/bunch * 100kHz trigger rate *7 error windows= 44.8Mbps < 160Mbps**

Thank you !