Status of the Silicon Tracker demonstrator

2020 International Workshop on the High Energy Circular Electron Positron Collider
Shanghai, 26 October 2020

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For the CEPC Silicon Tracker community

(participating institutes at the end of the talk)

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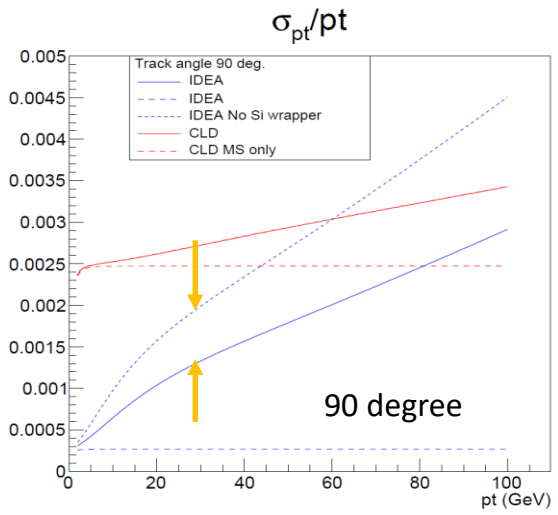
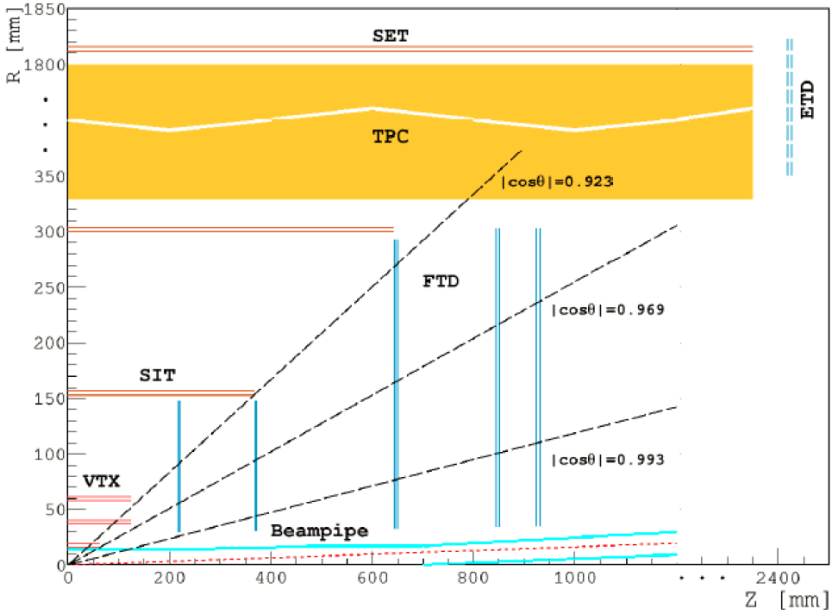
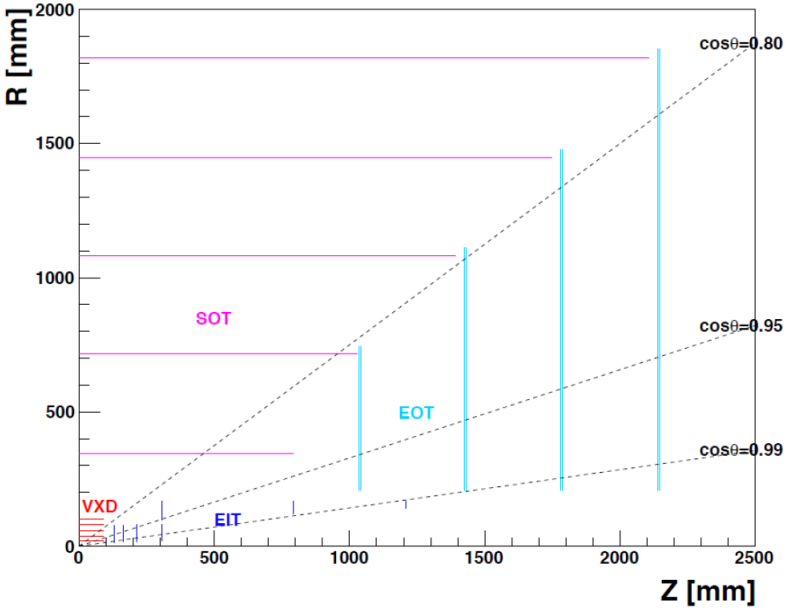
Silicon Tracker Concept

- Central tracking at CEPC require large area silicon tracking systems
  - **Silicon wrapper** (baseline TPC design, IDEA)





  - **Full silicon layout**



- Size and requirements similar to LHC Trackers
  - O(100) m^2 area
  - 25 ns bunch spacing at Z-pole
  - but lower radiation levels and per-event occupancy

Silicon Tracker Concept

CEPC Detector R&D Project
2.2 Silicon Tracker Prototype

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Revision number:	2

- Depleted CMOS Pixel Sensors
- Demonstrate the detector concept using existing sensor ATLASPIX3
  - aggregate sensors in larger area modules
  - assemble the detector in stavelets for system tests (DAQ and services)
- In parallel adapting the sensor technology to CEPC environment
  - see I. Peric's presentation

Institute of High Energy Physics
Chinese Academy of Sciences
SHANDONG UNIVERSITY
Tsinghua University
Tsung-Dao Lee Institute
SHANGHAI JIAO TONG UNIVERSITY
HARBIN INSTITUTE OF TECHNOLOGY
University of Science and Technology of China
NORTHWESTERN POLYTECHNICAL UNIVERSITY
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University of BRISTOL
UKRI Science and Technology Facilities Council
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The University Of Sheffield.
Queen Mary University of London
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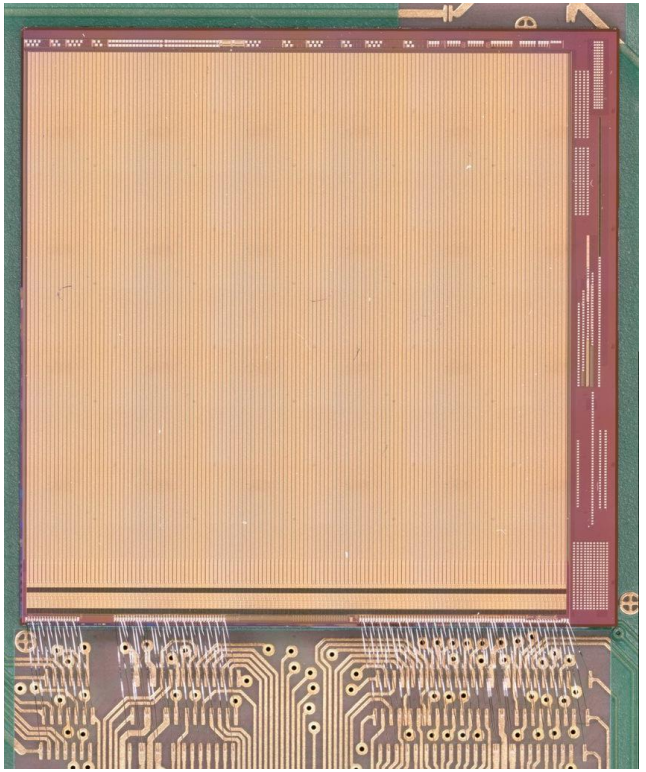
Physics Lancaster University
UNIVERSITY OF OXFORD

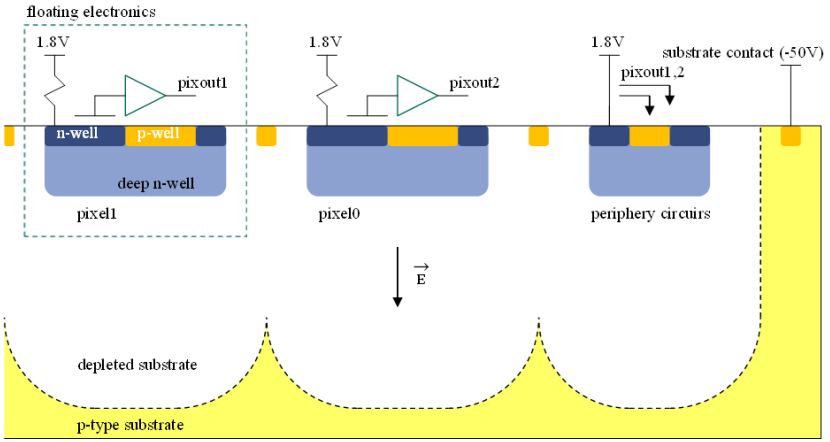
Collaboration recently joined by:

UNIVERSITY OF SOUTH CHINA

ATLASPIX3

- **Monolithic CMOS**
  - widespread process allows to produce **large areas** **fast** and **cheap**
  - **no hybridization** (bump-bonding) needed
  - **single detection layer**, can be **thinned** keeping high signal efficiency and low noise rate
- **ATLASPIX3 features**
  - pixel size $50 \times 150\ \mu m^2$ (or smaller)
  - up to 1.28 Gbps downlink
  - reticle size $20 \times 21\ mm^2$
  - TSI 180 nm process on 200 Ωcm substrate
  - 132 columns of 372 pixels
  - digital part of the matrix located on periphery
  - both **triggerless** and **triggered** readout possible:
    - two End of Column buffers
    - 372 hit buffers for triggerless readout
    - 80 trigger buffers for triggered readout

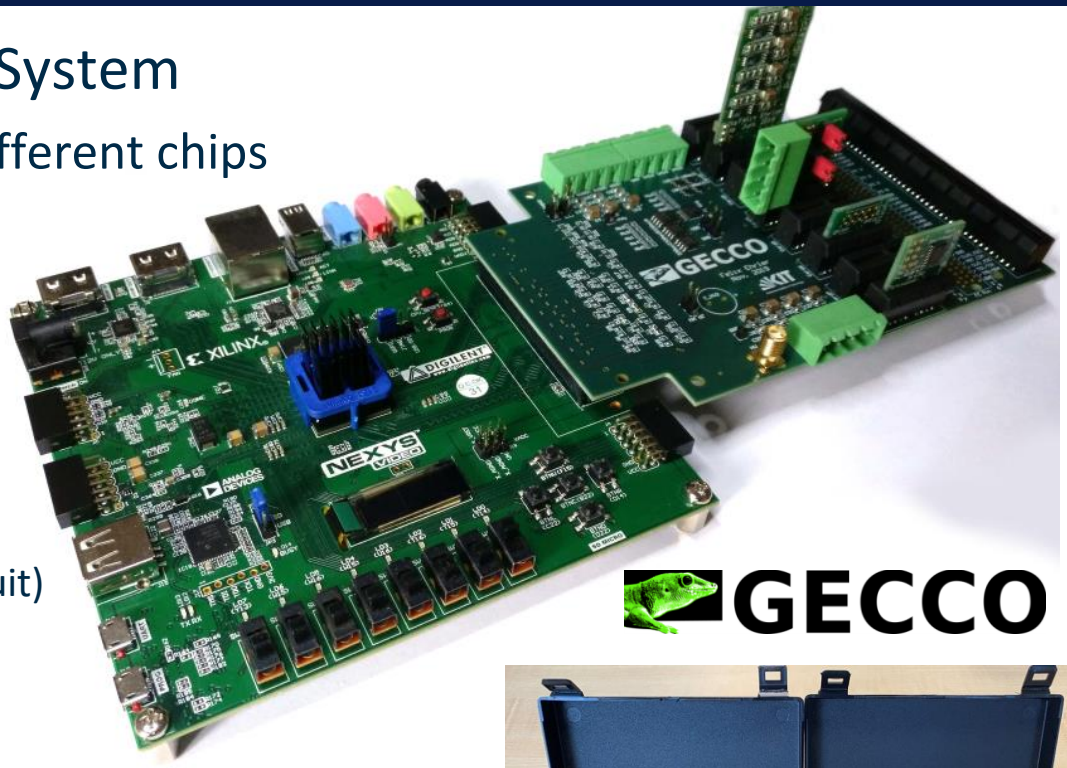




Laboratory readout systems

GEneric Configuration and COntrol System

- Versatile system for application with different chips
- GECCO board:
  - **LPC-FMC** connector (160 pins) **to FPGA** readout board (Nexys Video with Xilinx Artix-7)
  - **PCIe x16** connector (164 pins) **to DUT**
  - 10 power connection + HV
  - Expensive components (DACs, injection circuit) on reusable board
  - Test points for all pins



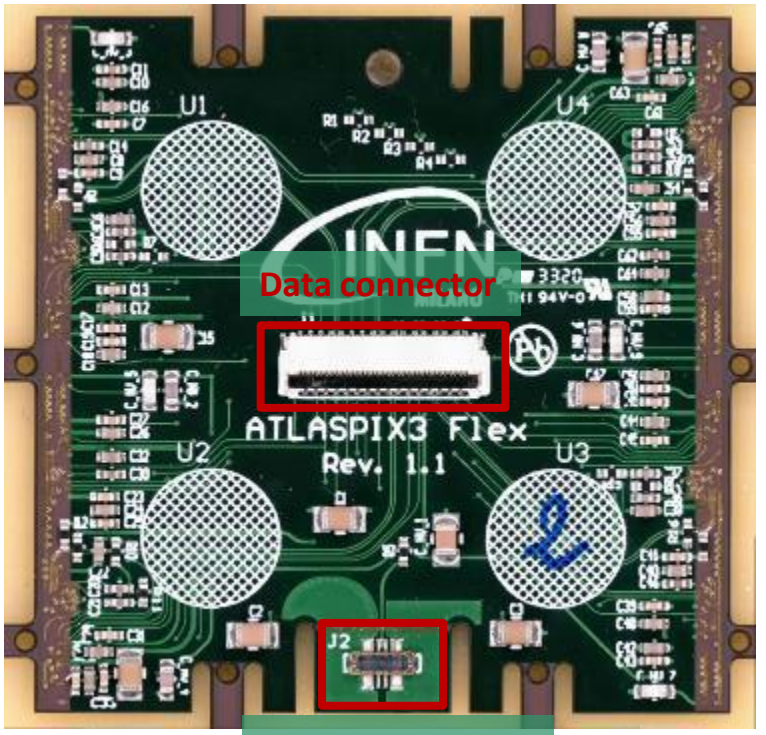
GECCO

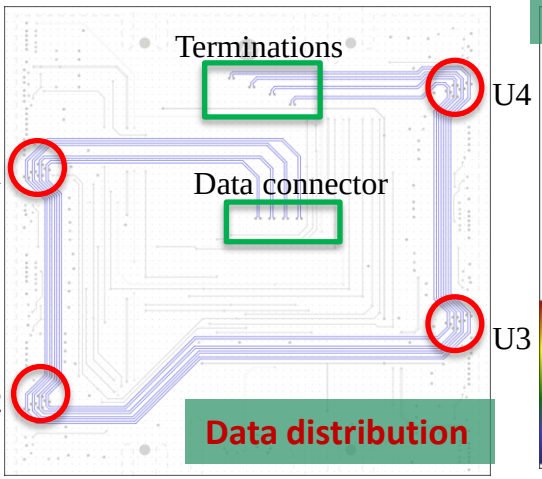
- **Devices have been distributed at participating institutes:**
  - **Common production of GECCO system cards**
  - **ATLASPIX3 chips at production thickness**
  - **1st virtual hands-on workshop held on October 22nd 2020**
- More sensors now at OPTIM (F) for thinning to 150 μm and dicing

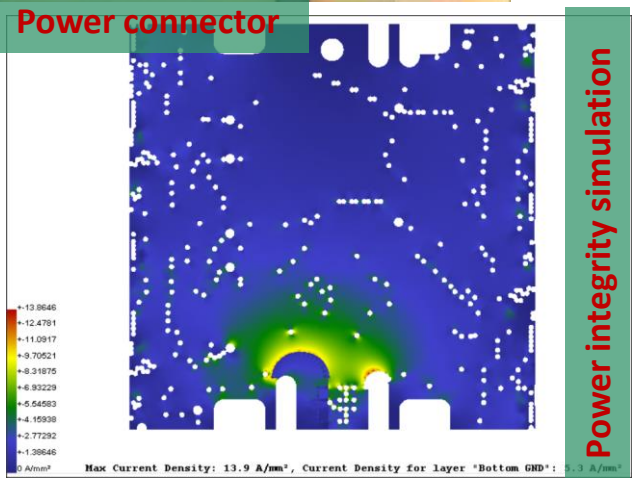
Module concept

- **Readout unit based on 4 chips**
  - shared services among 4 sensors by common power connections and configuration lines
  - benefits of in-chip regulators to reduce connections
  - avoids complications with stitching
- **Two configuration options**
  - command decoder (LVDS, default)
  - SPI (backup)
- **4-layer flex hybrid**
  - 2 power layers
  - 2 signal layers, impedance-matched lines

PCB received
now under verification

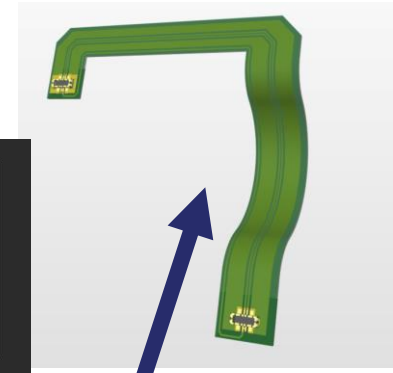


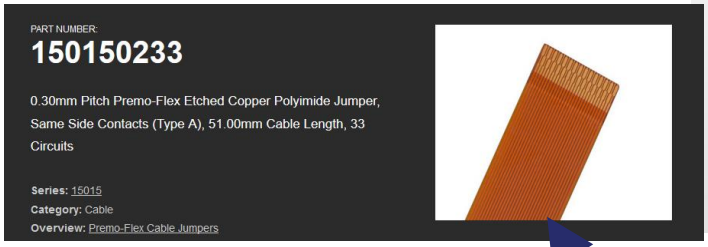


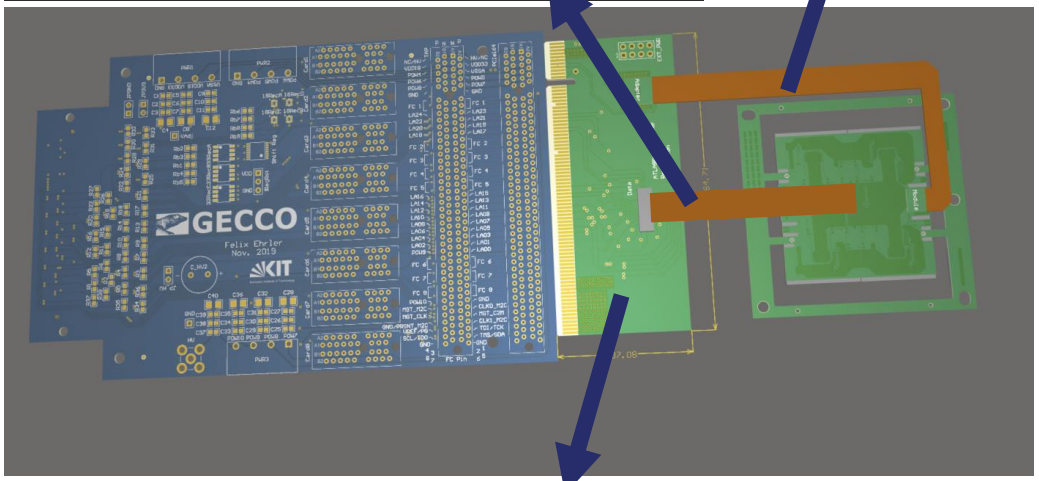


Module concept

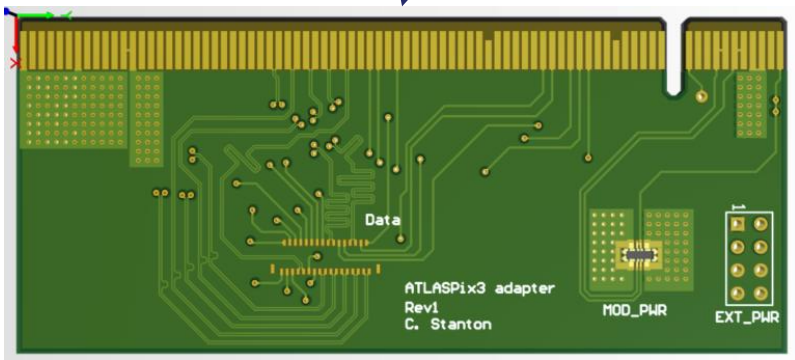
- **Adapter card for connection to GECCO system**
  - Routing of connections (100 Ω impedance-controlled lines, matched length data-out lines)
  - Option for providing external power connections
- **Commercial data pigtail**
  - 4 LVDS data-in lines
  - 4 LVDS data-out lines
  - 10 SPI configuration lines
  - 7 configuration pins
- **Custom power pigtail**
  - VDD power
  - LVDS and Gate additional biases
  - HV (max. 60 V) line







Design completed



System considerations

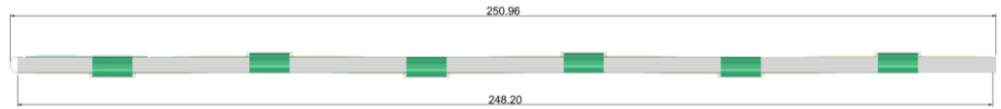
- Complete system consists of ~50k modules
  - aggregation of several modules for data and services distribution is essential
- System design constrained by the innermost layer
  - average rate 10^{-4} particles cm^{-2} $event^{-1}$ at Z peak
  - assuming 2 hits/particle, 96 bits/hit for ATLASPIX3
  - **640 Mbps link/module** (assuming local module aggregation) provides ample operational margin
  - modules can be arranged into **10 Gbps fast links**: **4k links**
  - **triggerless readout** will fit the data transmission budget but requires off-chip re-ordering of data
  - **triggered readout** will be **simpler** and would also reduce the bandwidth occupancy
- ATLASPIX3 power consumption **150 mW/cm²**
  - 600 mW/chip → 2.4 W/module → **total FE power ~100 kW**
  - additional power for on detector aggregation and de-randomizations **~2W/link**

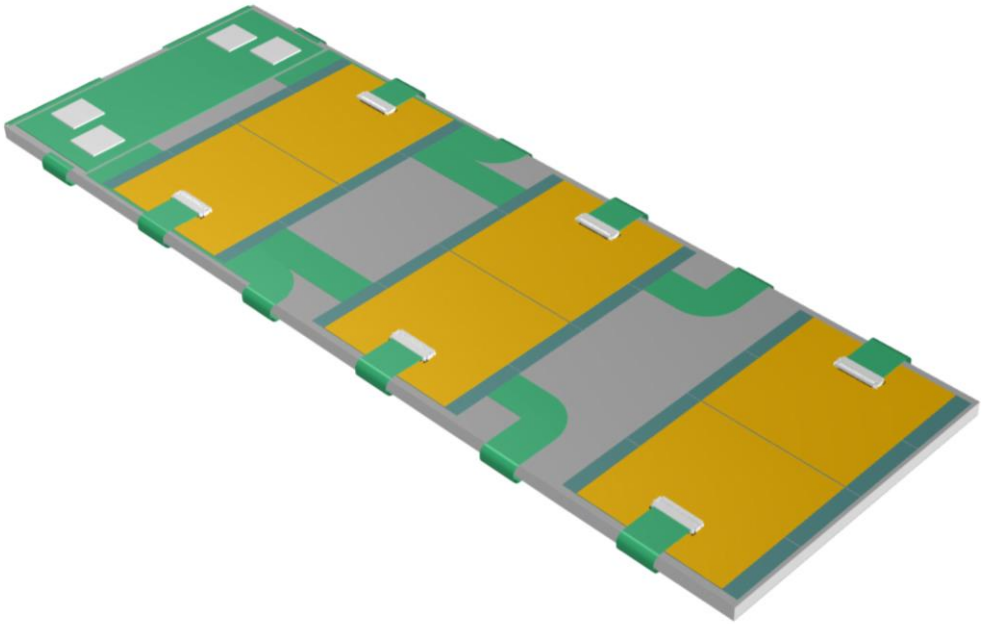
Stavelet layout

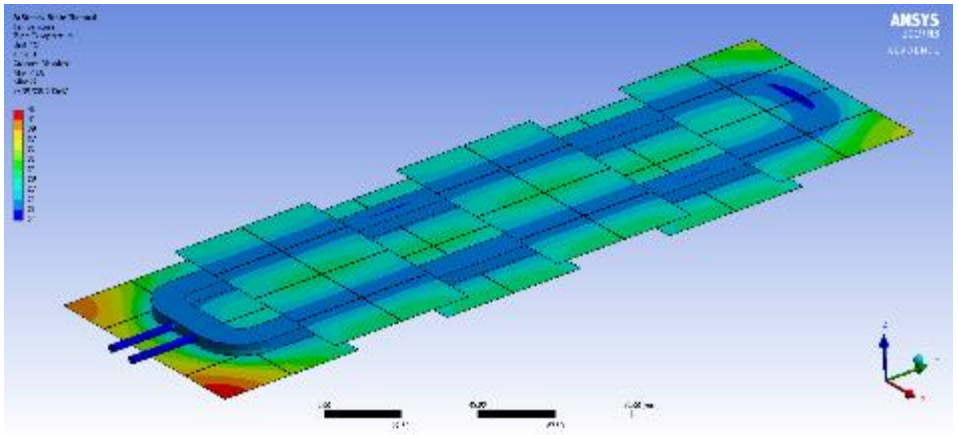
- Detector element consisting of multiple modules on light composite support
  - alternate tile pattern for hermeticity
  - aggregation of data/optical conversion at end-of-stave
  - use serial powering

- Different options available
  - pipes in Ti, steel, C, microchannel
  - CO_2 or water cooling
  - alternative cooling of supports

- **Stavelet demonstrator** (12 modules) **design under optimization**
- Populated by **2nd generation ATLASPIX3 modules** configured for serial powering







Summary and outlook

- **CMOS Pixel Detector are a viable option** not only for the vertex region (see this morning session), but also **for the large area tracker system**.
- While improving the detector prototypes, a **demonstrator effort** is developing based on **ATLASPIX3**:
  - A first module design is available, and components are under preparation
  - DAQ components and devices at production thickness have been distributed to the involved institutes
  - Devices thinned to 150 μm will become available soon
  - Preparation ongoing towards a demonstrator stavelet
  - Planning to procure additional wafers to populate ≥ 2 stavelets
- Work on **integration** with the other systems is ongoing:
  - Assume data and power aggregation at stavelet: ~4k connections
  - Most efficient readout is triggered
  - Starting optimization of detector design with simulation

Thanks for your attention!

on behalf of the Silicon Tracker community

- **China**
  - Institute of High Energy Physics, CAS
  - Shangdong University
  - Tsinghua University
  - University of Science and Technology of China
  - Northwestern Polytechnical University
  - T.D. Lee Institute – Shanghai Jiao Tong University
  - Harbin Institute of Technology
  - University of South China
- **Italy**
  - INFN Sezione di Milano, Università di Milano e Università dell'Insubria
  - INFN Sezione di Pisa e Università di Pisa
  - INFN Sezione di Torino e Università di Torino
- **Germany**
  - Karlsruhe Institute of Technology
- **UK**
  - University of Bristol
  - STFC – Daresbury Laboratory
  - University of Edinburgh
  - Lancaster University
  - University of Liverpool
  - Queen Mary University of London
  - University of Oxford
  - University of Sheffield
  - University of Warwick

BACKUP

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