TDAQ requirements for Dual-Readout Calorimeter

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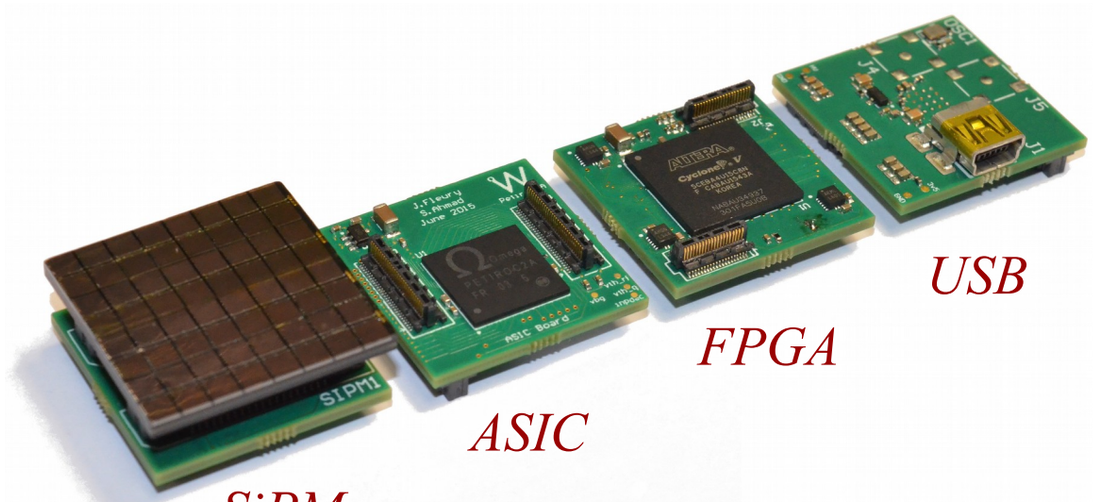
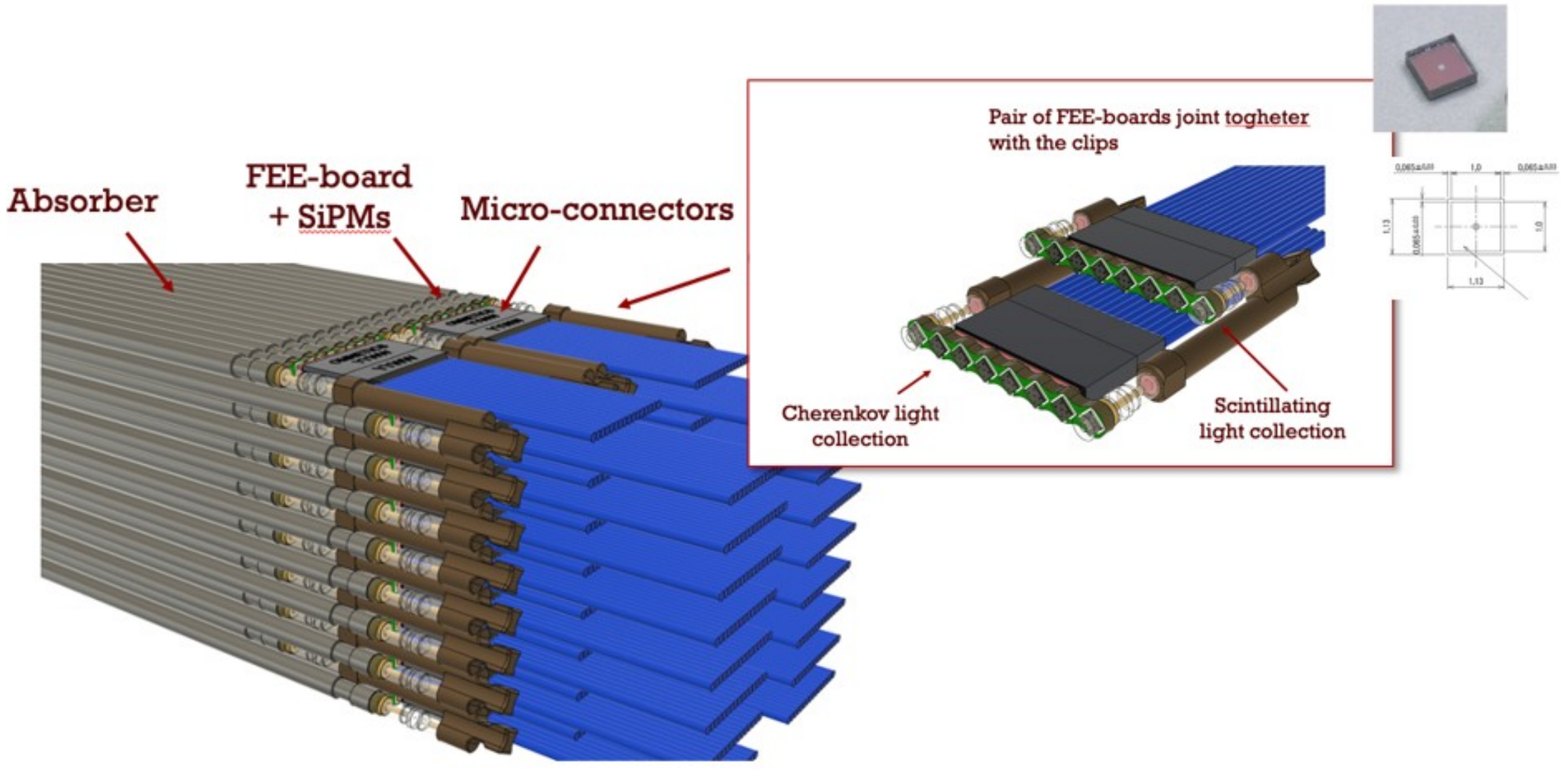
DR calo - readout structure

Target:



new scalable frontend solution



implementation of 8-channel grouping (on FEE board) straightforward

ASIC (charge integrator)

weeroc catalogue:

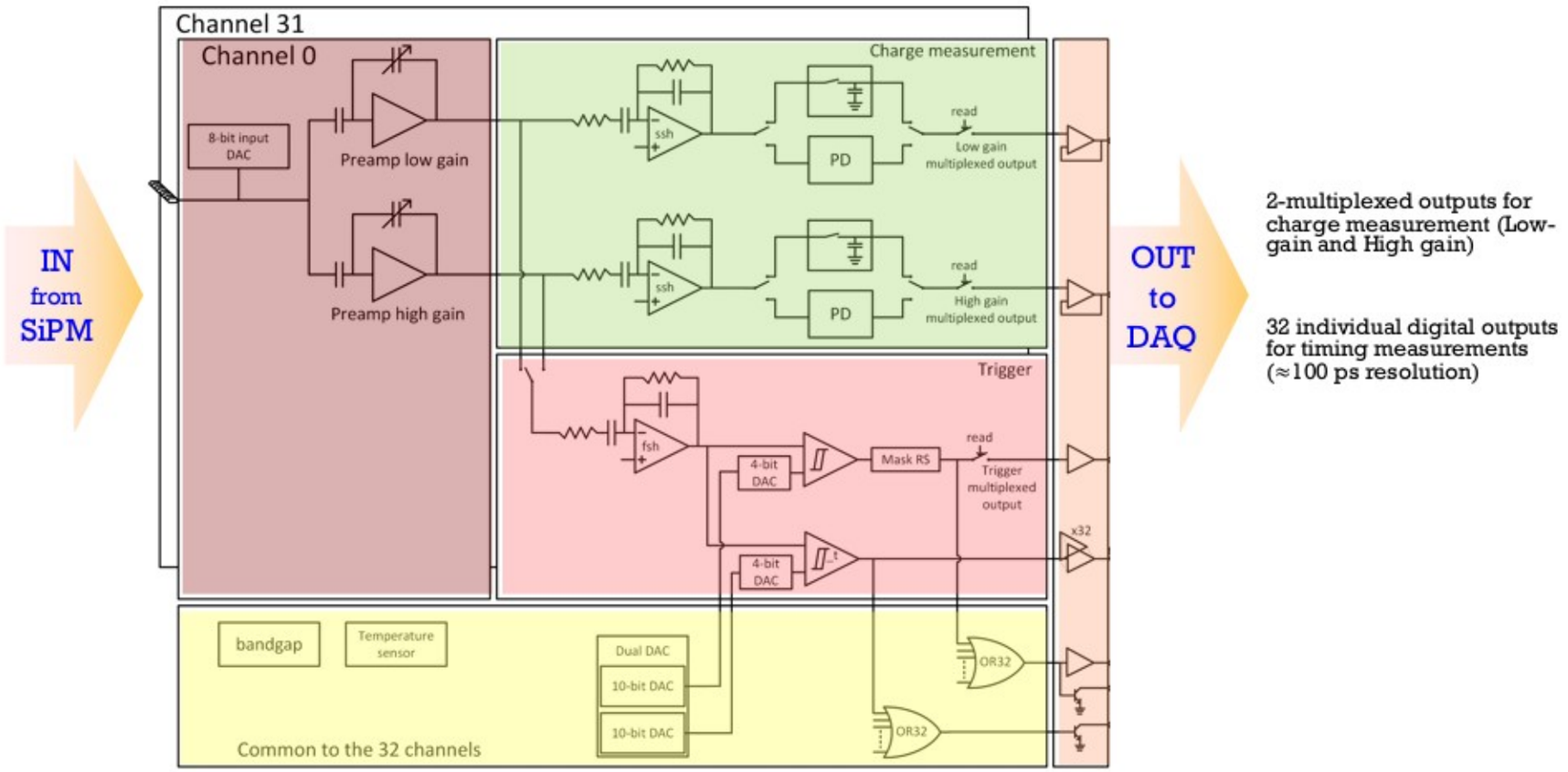
Chip	Detector	Ch	Polarity	Dyn Range	Specificities
SPIROC	SiPM	36	>0	10 fC - 300 pC	36 HV SiPM tuning (8 bits), Internal 12-bit ADC for charge and time measurement
EASIROC	SiPM	32	>0	10 fC - 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
CITIROC	SiPM	32	>0	10 fC - 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs
PETIROC	SiPM	32	<0	100fC – 300 pC	32 HV SiPM tuning (8 bits), 32 trigger outputs, Internal 10-bit ADC for charge and time measurement (25 ps)
TRIROC	SiPM	64	Both	100 fC- 300 pC	64 HV SiPM tuning (8 bits), 64 trigger outputs, Internal 10-bit ADC for charge and time measurement (25 ps)

Citiroc 1A:

Detector Read-Out	SiPM, SiPM array
Number of Channels	**32**
Signal Polarity	Positive
Sensitivity	Trigger on **1/3 of photo-electron**
Timing Resolution	Better than **100 ps RMS** on single photo-electron
Dynamic Range	0-400 pC i.e. 2500 photo-electrons @ 10^6 SIPM gain
Packaging & Dimension	TQFP160-TFBGA353
Power Consumption	225mW - Supply voltage: 3.3V
Inputs	32 voltage **inputs with independent SiPM HV adjustments**
Outputs	**32 digital outputs (for timing)** **2** multiplexed **charge output, 1** multiplexed **hit register and 2 trigger outputs**
Internal Program. Features	32 HV adjustment for SiPM (32x8bits), Trigger Threshold Adjustment, channel by channel gain tuning, 32 Trigger Masks, Trigger Latch, internal temperature sensor

weeroc

Citiroc – block diagram



https://www.weeroc.com/my-weeroc/download-center/citiroc-1a/16-citiroc1a-datasheet-v2-5/file

Numbers and Power Budget

	#	U.P.(W)	Power (kW)
SiPM	130M	15 μW	2
	grouping factor = 8 # ch / ASIC = 32		
→ ASIC	510k	(32×2.5 mW) = 0.08	41
	# ASIC / FPGA = 16		
→ FPGA	32k	10	320

throughput – very conservative estimate

Very conservative approach:

# of p.e. < O(10^3)/GeV → <~ 100 k p.e./evt @ Z pole

at most 3-4 Bytes / p.e.:

12 bits → time (60 ps within 250 ns)
5 bits → SiPM group number
4 bits → ASIC number

→ 400 kB/evt

total throughput @ 100 kHz trigger rate <~ 40 GB/s

throughput – conservative estimate

Z→jj events: 4100 S + 2000 Č fibres per event (no B field)

Q_T, ToA, ToT, T_{Pk}, V_{Pk}, Channel Identifier

< ~ 12-16 Bytes / SiPM (no grouping)

→ 16 B × (4100 + 2000) ≈ 100 kB/evt

total throughput @ 100 kHz trigger rate < ~ 10 GB/s

with 8 channel-grouping:

total throughput <~ 1.3 GB/s

even including B field no way to diverge !

dark counts

Number of channels ~ 130 M

a) assuming <dark count rate> ~ 250 kcps / SiPM

b) assuming readout time window ~ 250 ns

→ <noise> = 0.06 / SiPM / evt

→ noise occupancy ~ 130 M × 0.06 / evt

= ~ 8 M/evt

→ ~ 10^3 × signal rate

need suppression for isolated counts … if not :

total throughput ~ TB / s

****** totally dominated by noise ******

conclusions

1) Signal throughput looks to be “not-an-issue”

2) Noise needs suppression

Not yet considered:

3) Beam-gas interactions ?

4) Triggering/calibration issues ?

5) Dead time ? Expected to be marginal ...