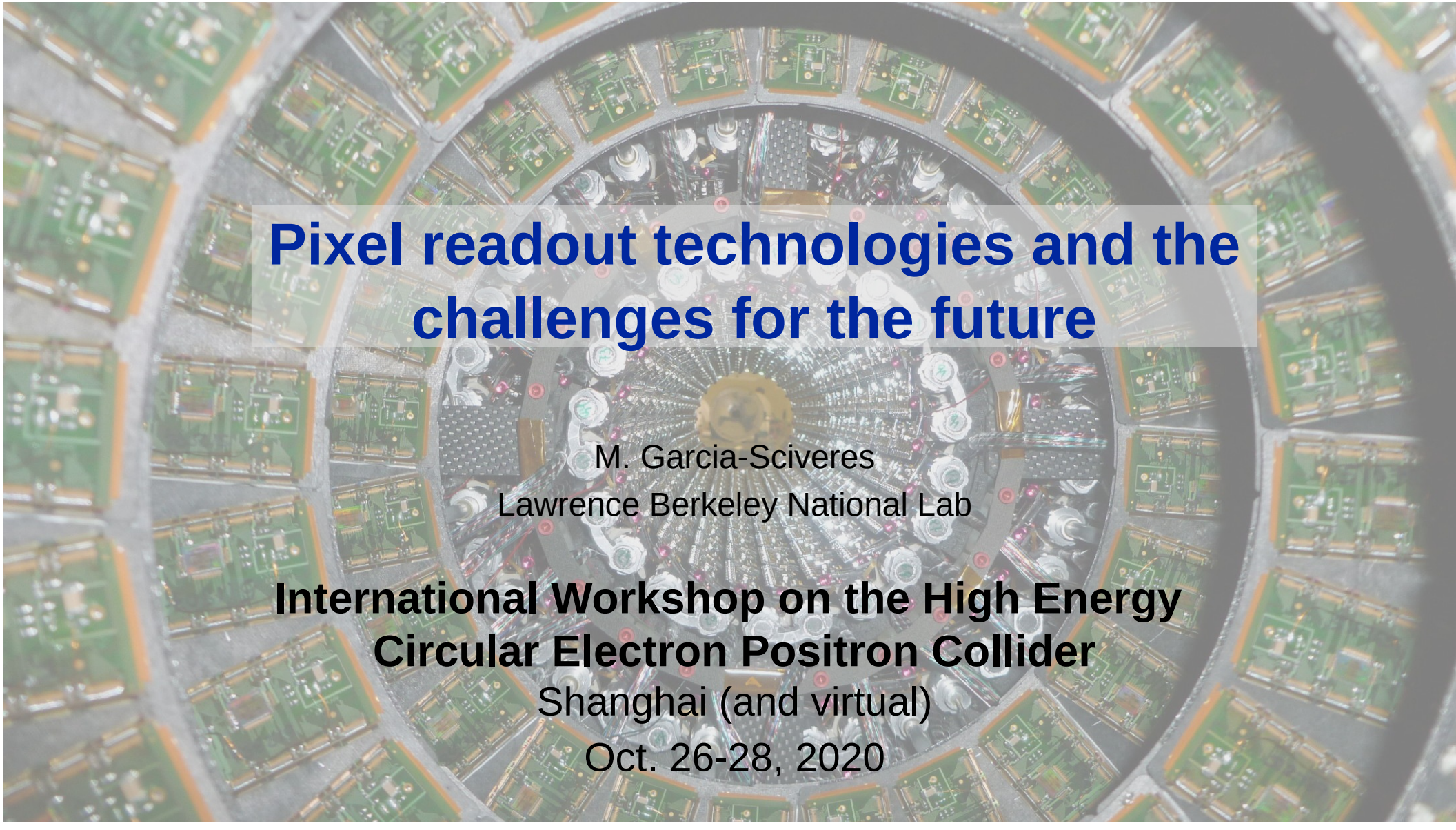
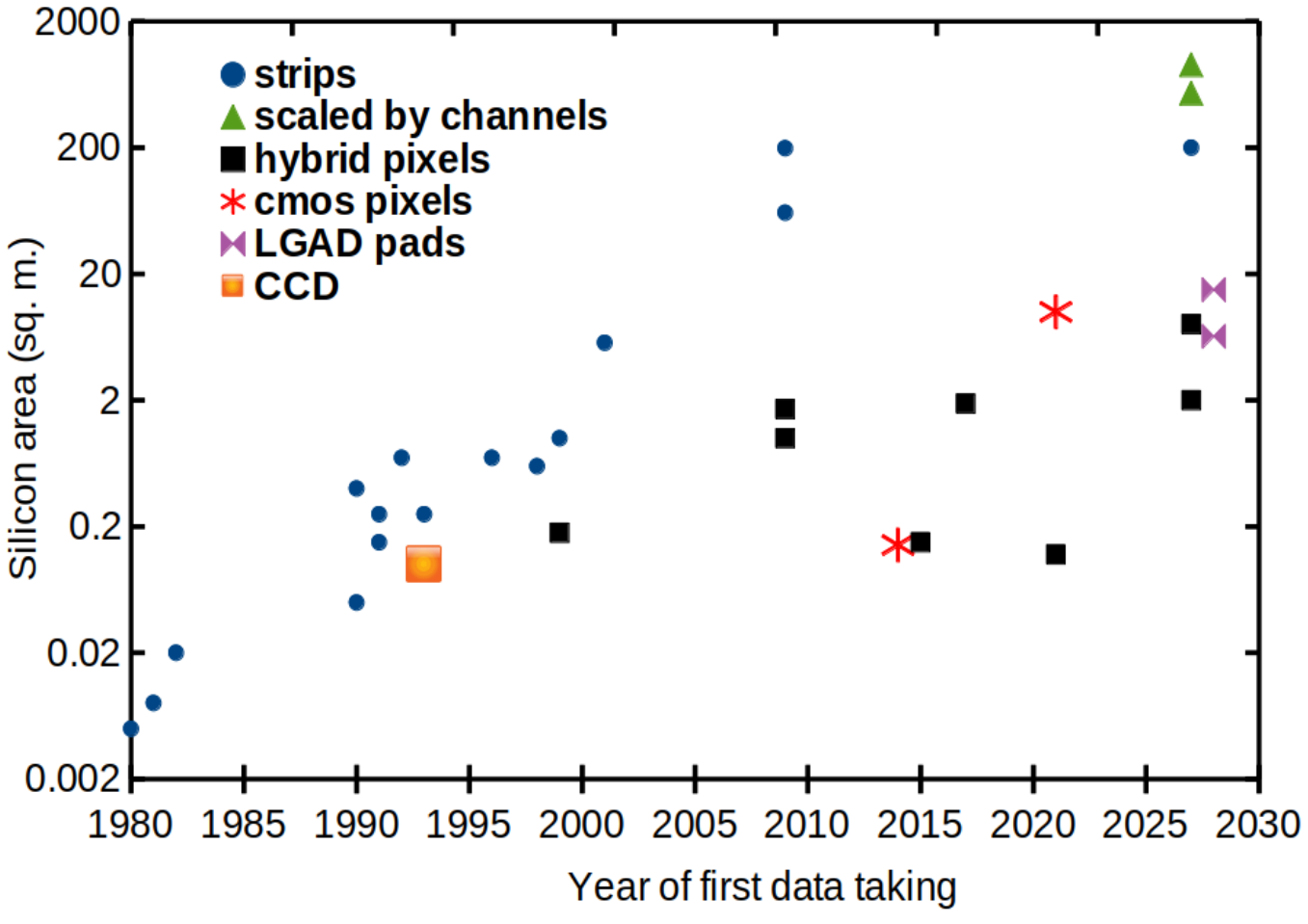


# Pixel readout technologies and the challenges for the future

M. Garcia-Sciveres
Lawrence Berkeley National Lab

**International Workshop on the High Energy Circular Electron Positron Collider**
Shanghai (and virtual)
Oct. 26-28, 2020

# Silicon Detector Evolution




**Strip Detectors**

| | |
|---|---|
| 1980 | NA1 |
| 1981 | NA11 |
| 1982 | NA14 |
| 1990 | MarkII |
| 1990 | DELPHI |
| 1991 | ALEPH |
| 1991 | OPAL |
| 1992 | CDF SVX |
| 1993 | L3 |
| 1996 | CDF SVX' |
| 1998 | CLEO III |
| 1999 | BaBar |
| 2001 | CDF SVXII+ISL |
| 2009 | ATLAS SCT |
| 2009 | CMS tracker |
| 2027 | ATLAS ITK |
| 2027 | CMS upgrade |

**CCDs**

| | |
|---|---|
| 1993 | VXD |

**Hybrid Pixels**

| | |
|---|---|
| 1999 | Delphi |
| 2009 | ATLAS |
| 2009 | CMS |
| 2015 | ATLAS IBL |
| 2017 | CMS |
| 2021 | velopix |
| 2025 | ATLAS |
| 2025 | CMS |

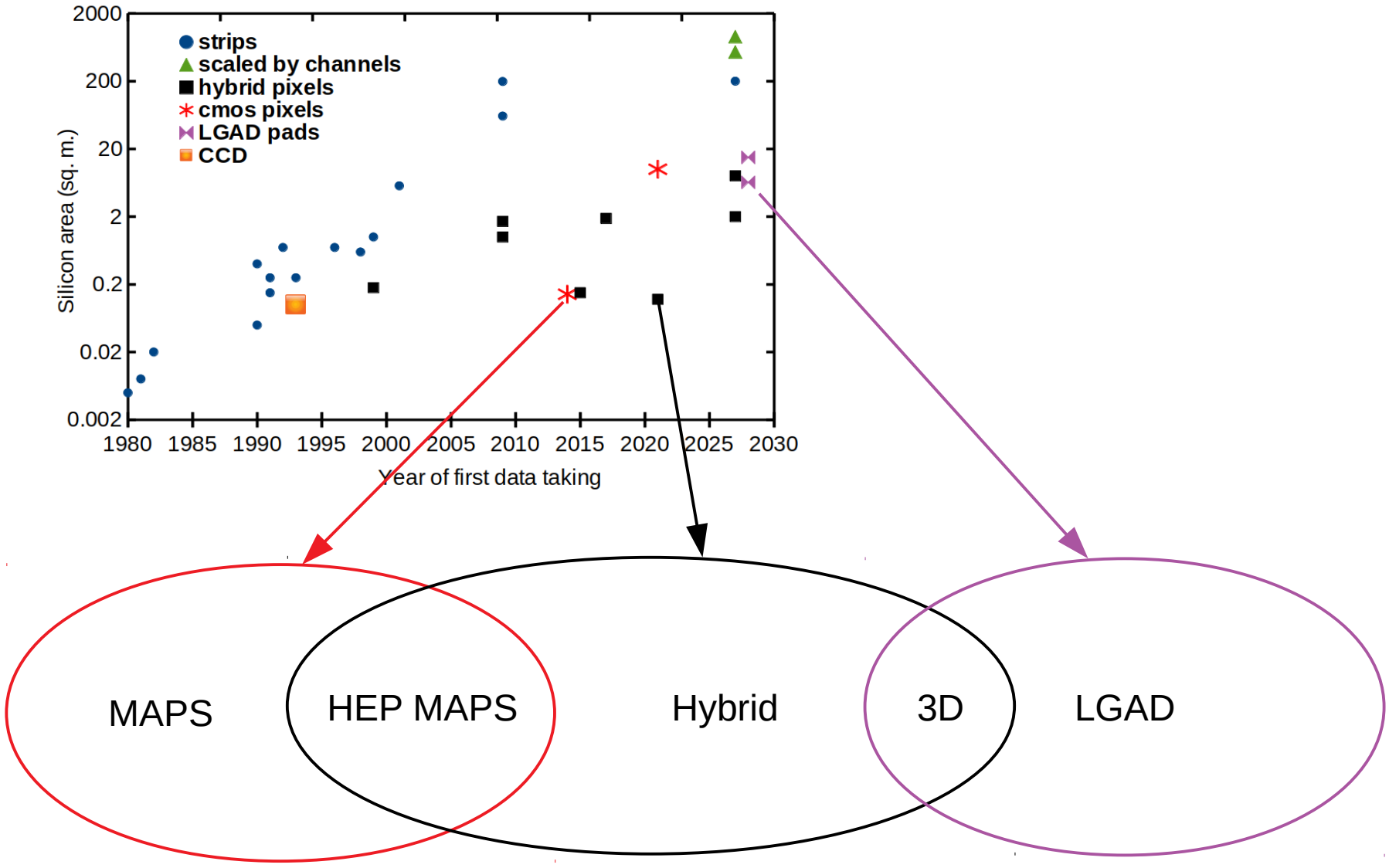
**CMOS Pixels**

| | |
|---|---|
| 2014 | STAR |
| 2021 | ALICE |

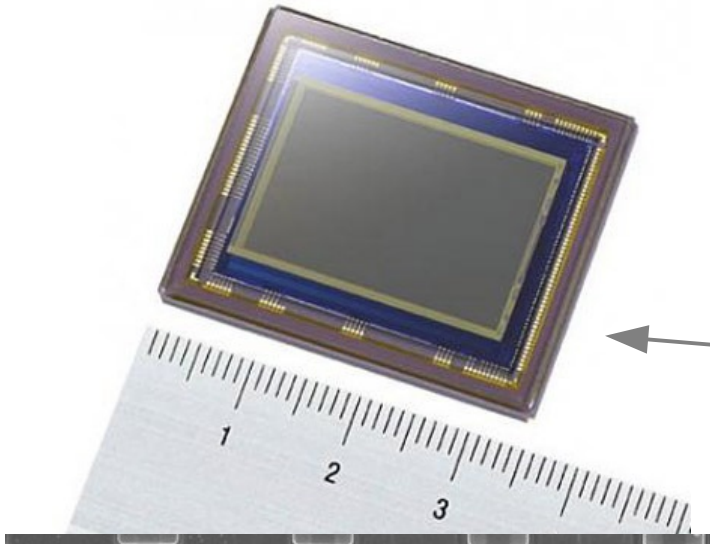
**LGAD pads**

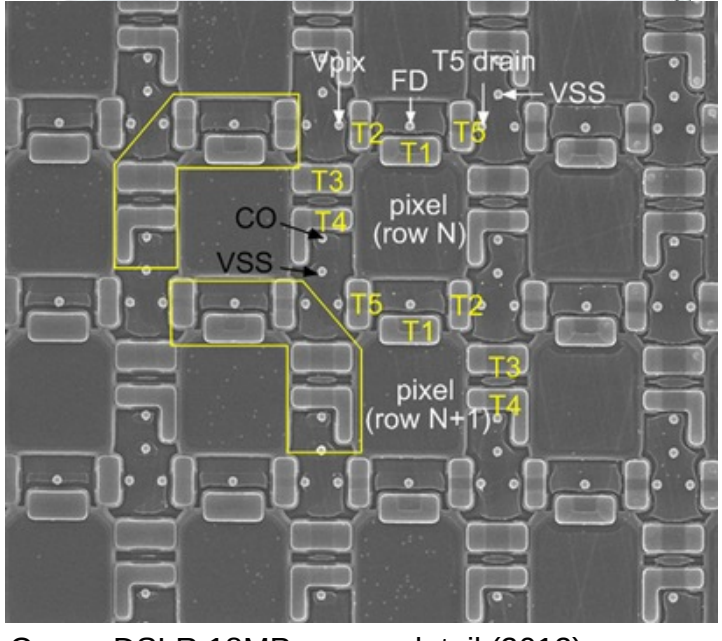
| | |
|---|---|
| 2027 | ATLAS |
| 2027 | CMS |

# Pixel Readout Varieties



# Classic MAPS readout

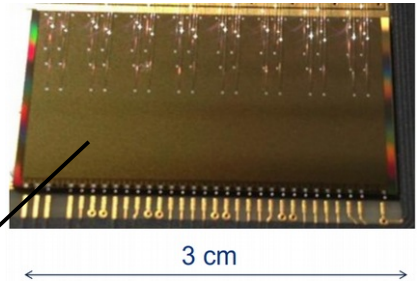


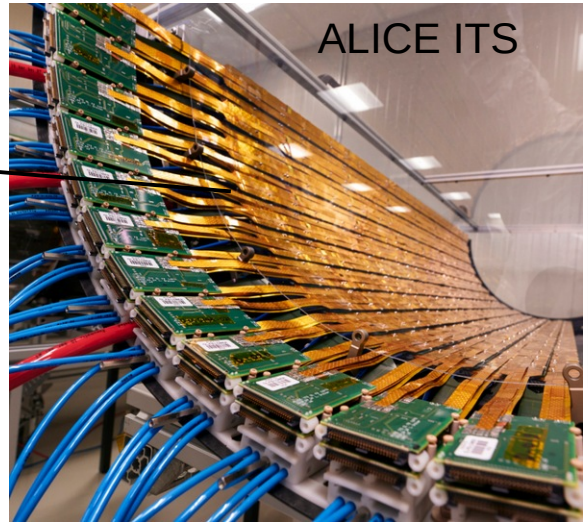



Canon DSLR 18MP sensor detail (2012)
8x8 um pixels

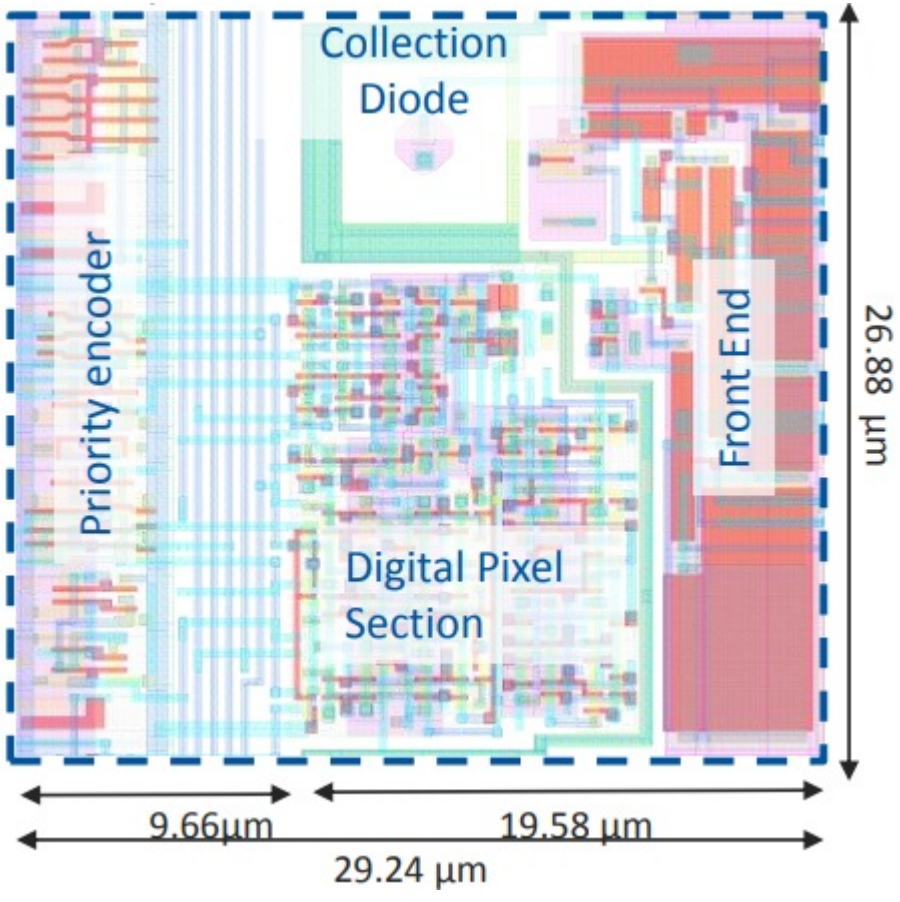
- For light- front illuminated
- Very few transistors per pixel sharing active area with sensor
- Very small pixels and very low power
- Slow
- Minimal rate capability
- No timing information

# HEP MAPS



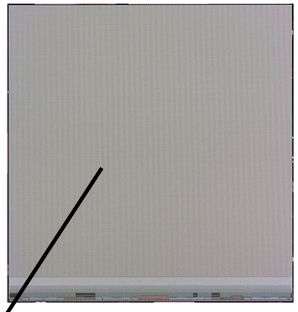



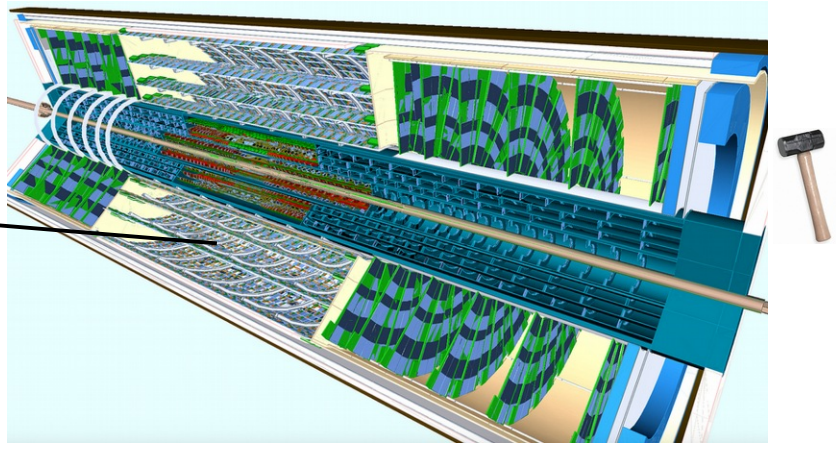

Alpide chip pixel layout



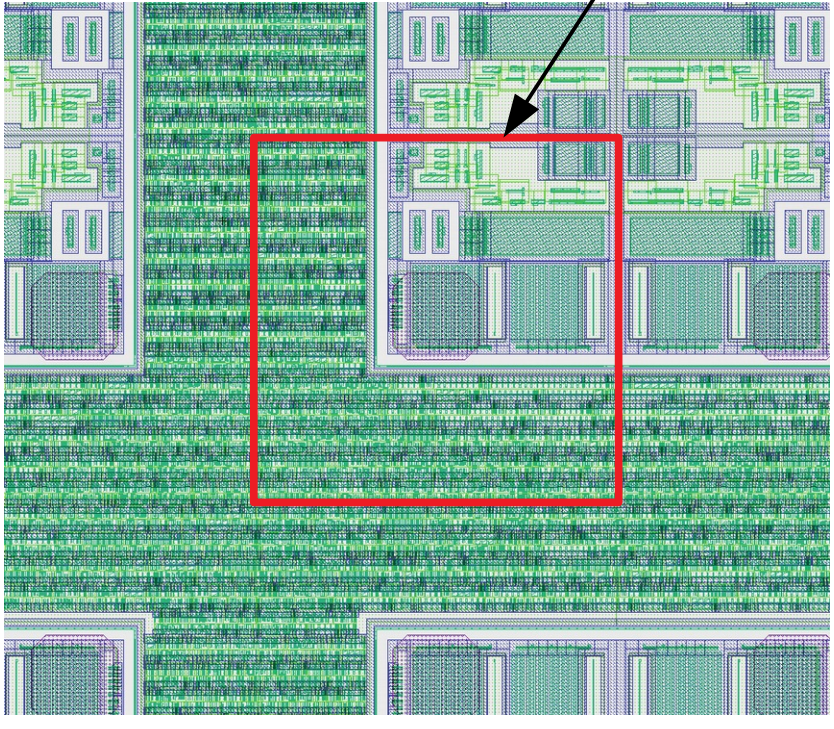

- For particles- active bulk BELOW circuitry.
- 100's of transistors per pixel
- Significantly bigger pixels
- More power
- Some timing information
- Intermediate rate capability
- Co-design of readout and sensing places many constraints on both and on fabrication process

# Hybrid



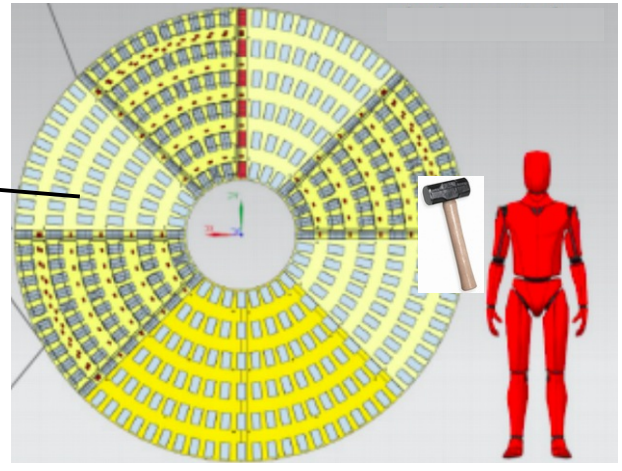


RD53B pixel layout

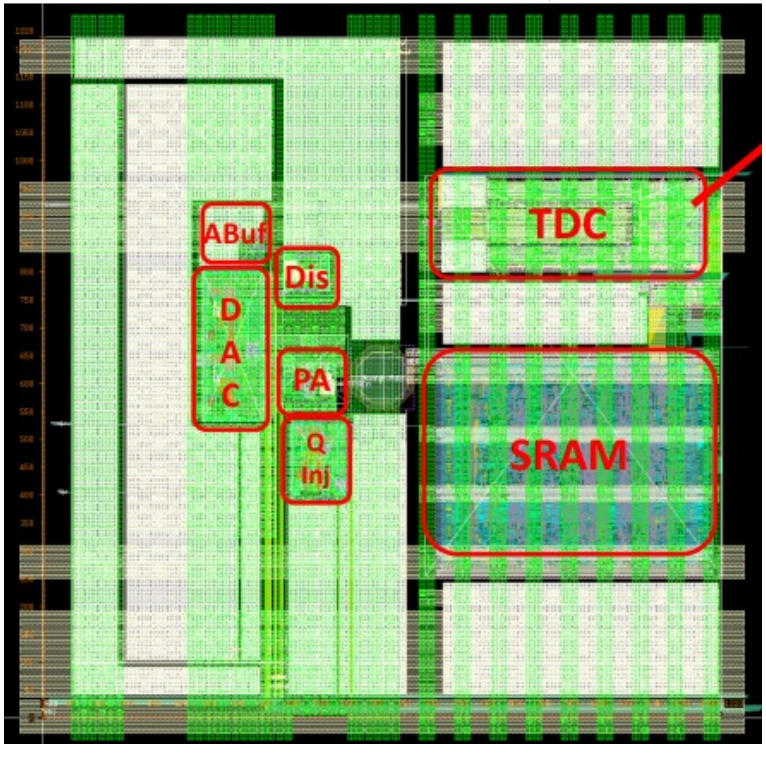


- Readout decoupled from sensor
- 1000's of transistors per pixel
- Same or a little bigger pixels than HEP MAPS
- Still more power
- ~10ns timing information
- Ultimate hit rate capability
- Free to use commercial CMOS processes

# LGAD Readout



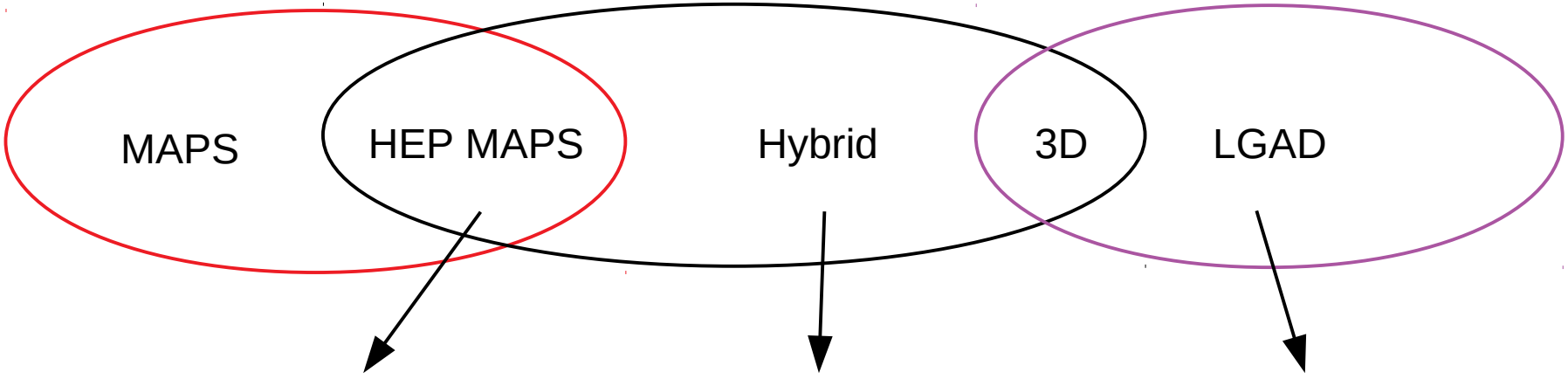
CMS ETROC “pixel” layout




1mm

- Readout decoupled from sensor
- 10,000’s of transistors per pixel
- Very large pixels today
- Precision time measurement in pixel and precision time reference distribution
- Still more power
- ~30ps timing information
- High hit rate capability
- Huge amount of data due to precision timing

# Challenges




- Customization
- Speed, Timing
- Rate
- Radiation hardness

- Access to and design in deep submicron CMOS
- Power
- Mass

- Pixel size with precision timing
- Data volume with precision timing
- Power and mass with precision timing

Specialized processes used for HEP MAPS are not highly scaled

Can't compete in functionality with deep submicron CMOS

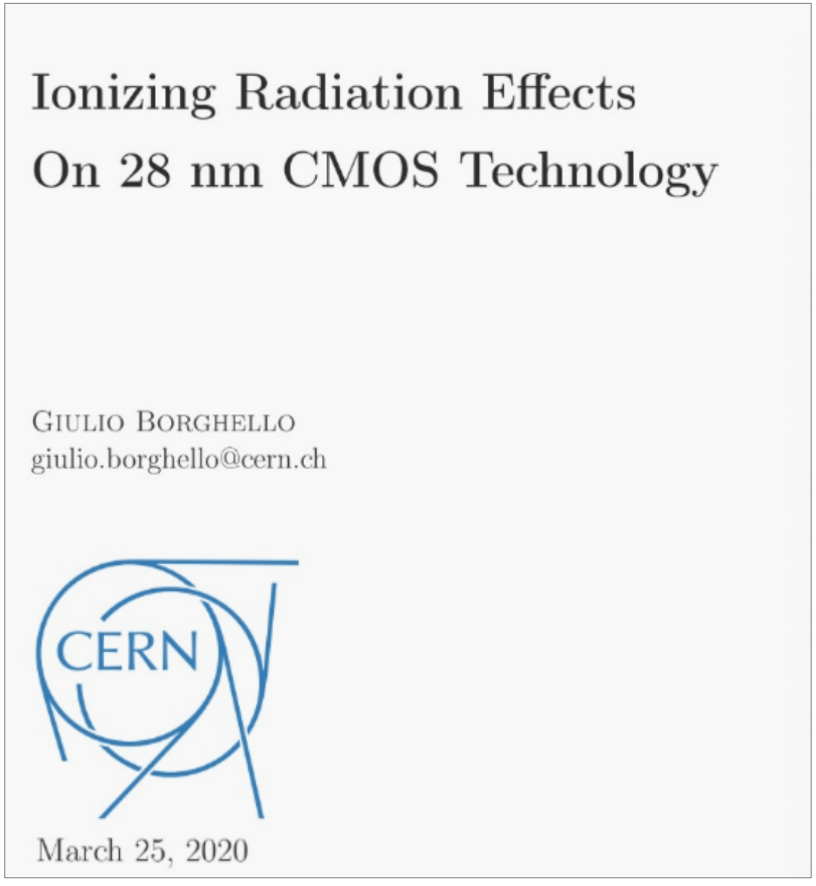
Lots of functionality requires lots of transistors.

Enabled by scaling in high volume commercial CMOS

lower ⟷ Rate, radiation, timing ⟷ higher

# Readout ASIC New Directions

- 65nm CMOS is current workhorse node for readout chips
- More functionality (like precision timing in small pixels) requires even higher logic density
- 28nm CMOS is the next favored node for HEP ASIC design



Ionizing Radiation Effects
On 28 nm CMOS Technology

GIULIO BORGHELLO
giulio.borghello@cern.ch

CERN

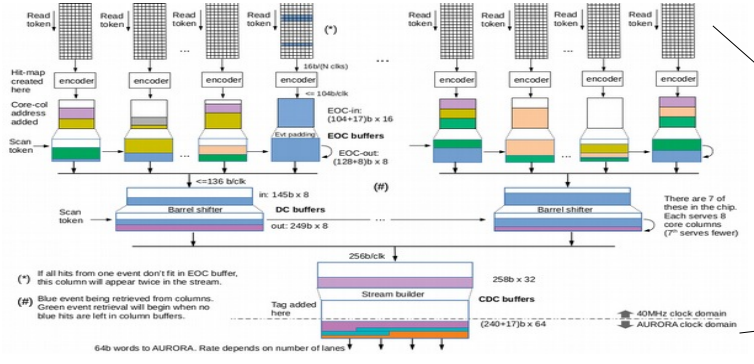
March 25, 2020

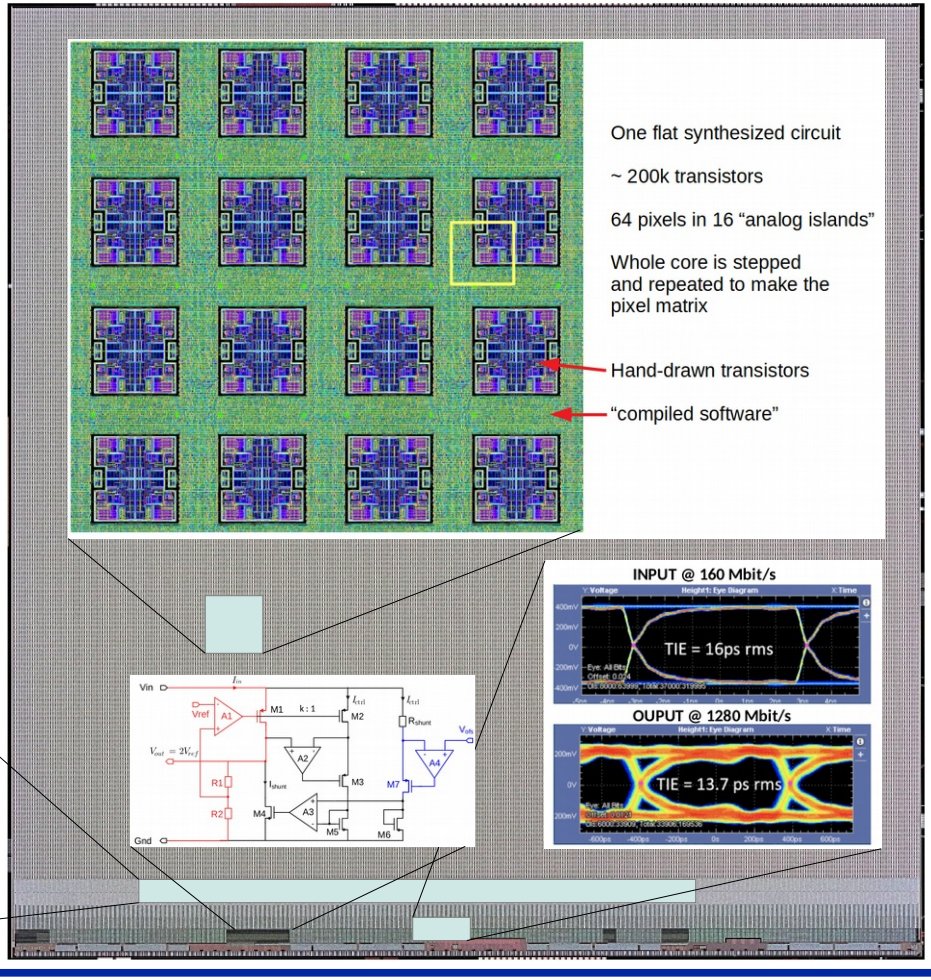
Contents

Executive Summary . . . 3
1 Introduction 11
2 Pre-Irradiation Characteristics 13
2.1 Process comparison . . . 13
2.2 device-to-device variability . . . 17
3 Radiation Response of 28 nm CMOS technology 19
3.1 Gate Oxide-Related Effects . . . 20
3.2 Channel Length-Dependent Effects . . . 21
3.2.1 Radiation-induced short channel effects . . . 22
3.2.2 Leakage current . . . 28
3.3 Channel Width-Dependent Effects . . . 36
3.4 Comparison Minimum Size Devices . . . 44
3.5 Radiation-Induced Variability . . . 48
3.6 Bias-Dependent Effects . . . 51
3.7 Temperature-Dependent Effects . . . 53
3.8 Low- and High-$V_{TH}$ transistors . . . 53
3.9 I/O devices . . . 56
Bibliography 59
Appendices 61
A Drain-to-Source Parasitic Leakage Current 62

# Main issues with 28nm known from 65nm experience

- Access to technology is requires legal NDA's with vendors that restrict collaboration
- Large design teams are needed to carry out complex designs in scaled CMOS
- Engineers with specialized skills, like UVM digital verifcation, are essential
- Some EDA design tools needed for digital design may have high license costs

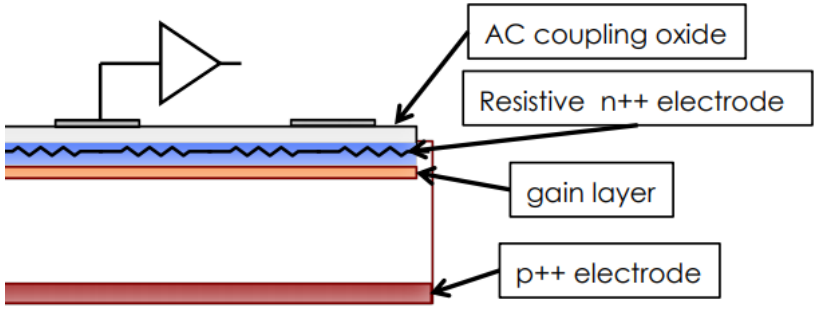



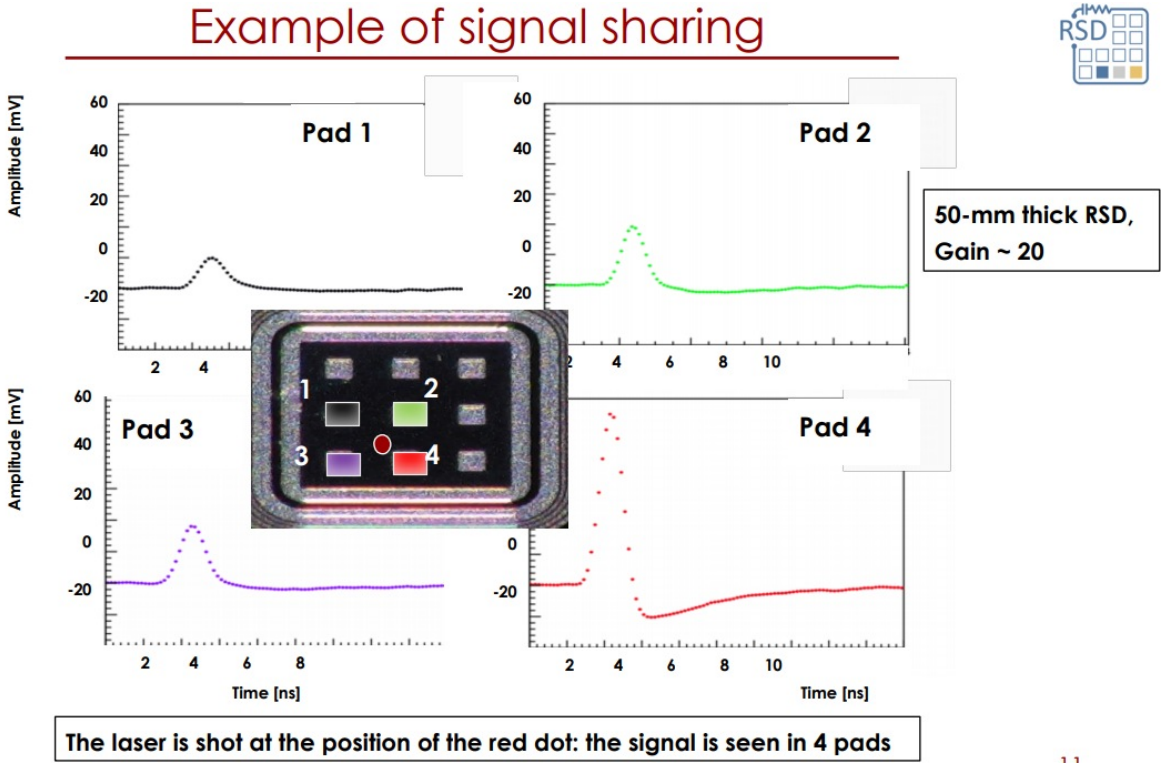




Digital pixel matrix in sophisticated SoC

# LGAD New Directions & Opportunities

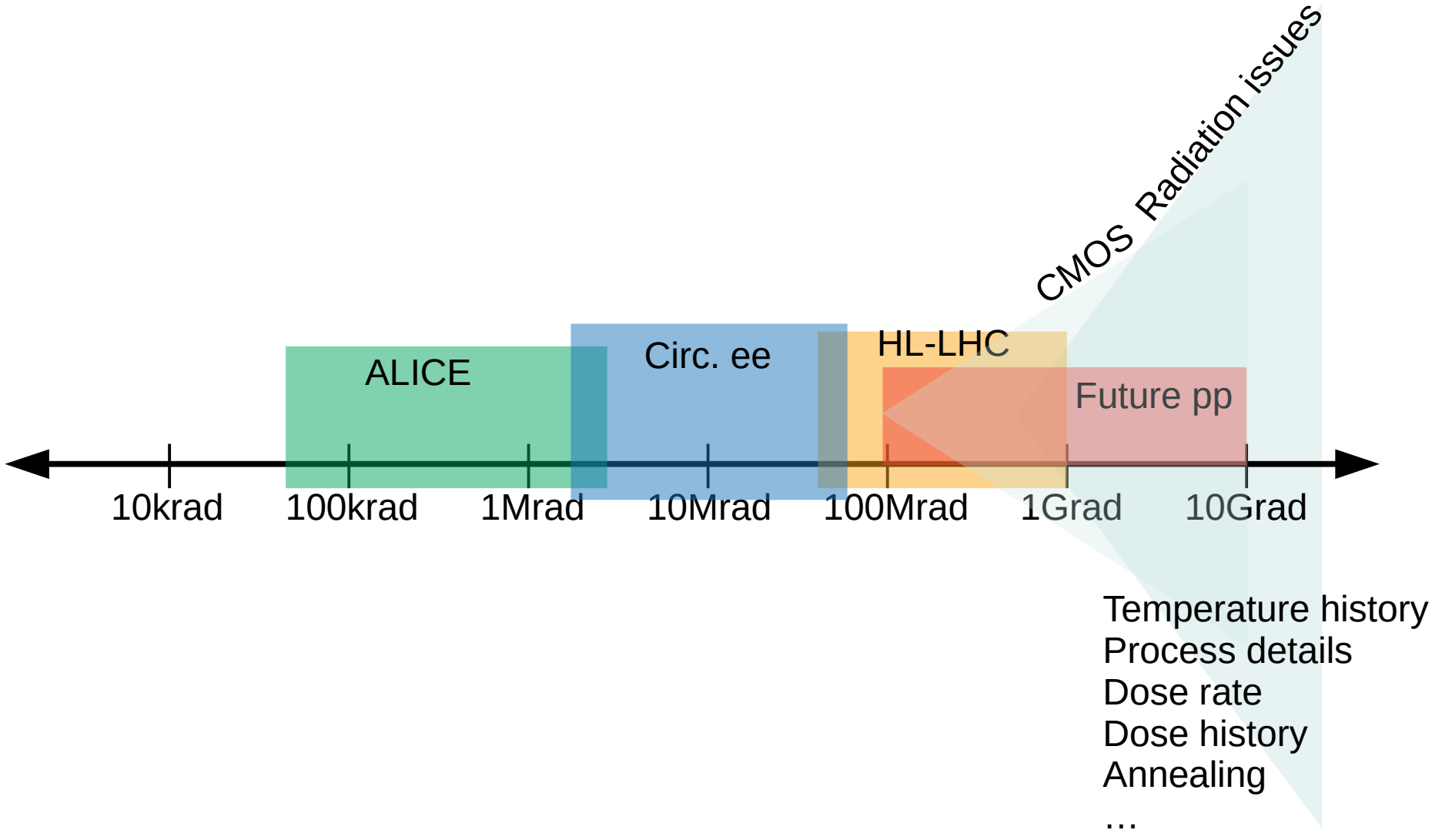
- Resistive AC-Coupled Silicon Detectors ( arXiv:2007.09528 )
- Promise high position and time resolution with low channel count and low assembly cost. Solves problem of making tiny pixels with huge functionality and low power.
- Will require new optimization of readout ASIC
- New opportunity to include Machine Learning in ASIC to learn and apply position calibration ("Application of machine learning algorithms to the position reconstruction of Resistive Silicon Detector" paper in preparation)
- => Even more complex SoS




Propose to achieve 5μm position resolution with ~100μm pitch pixels instead of 25μm pitch. 10X lower channel count => lower power

# Radiation only and issue at pp inner layers



# Data Rate

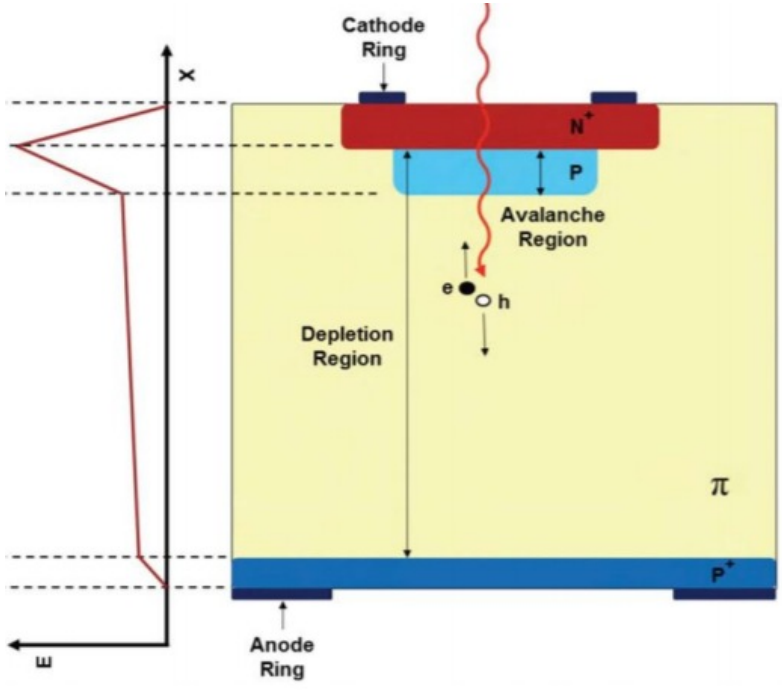
- High speed and huge capacity of scaled CMOS allows to generate enormous data rates. >>10Gbps links are feasible
- The problem is not generating the data, but getting it out of the detector
- Many development examples and options.
- My subjective list:
  - On-chip data compression. Lossless → lossy (ML)
  - Advanced protocols. 64b/66b NRZ → PAM4 → …
  - Silicon photonics, eg. WDM near chip

# Conclusions

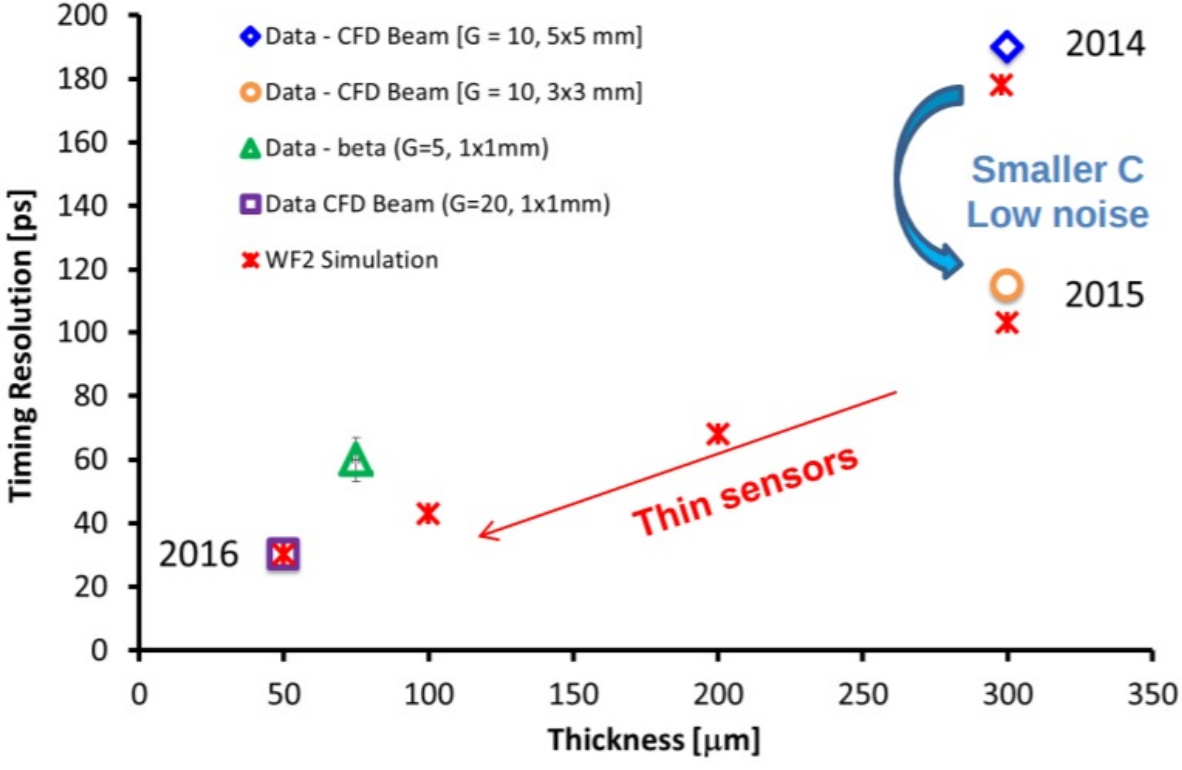
- Trade-off between monolithic and hybrid driven by functionality and power requirements.
  - Higher hit rate, precision timing, & radiation favor hybrid.
- The amount of intelligence that can be included in a hybrid pixel readout chip is not limited by technology- only by ideas on what else to do and human resources to carry out a complex design.
  - Gave examples of 28nm CMOS aimed at small pixels with precision timing and/or built in machine learning
- Challenges of 28nm CMOS design are known from 65nm experience
  - Even bigger and more expert design team will be needed and technology access is even more difficult
- ASIC radiation tolerance under control for all but future pp inner layer. But requires constant validation and vigilance- there are always surprises with radiation damage.
- A 28nm chip can generate huge data rates- the challenge is getting it off detector

# B A C K U P

# Low Gain Avalanche Devices




- Place an SiPM implant structure on a fully depleted pixel sensor
- Operate below Geiger threshold!
- Boosts rise-time of signals → fast timing



# LGAD was motivated by LHC pileup