High Performance Timing Measurement for CEPC SDHCAL

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On behalf of Shanghai-Omega-Lyon Group

CEPC Workshop

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Outline

- Why do we need timing in SDHCAL
  - Limitation of high granularity PFA Calorimeter
  - Showers separation
  - MRPC performance

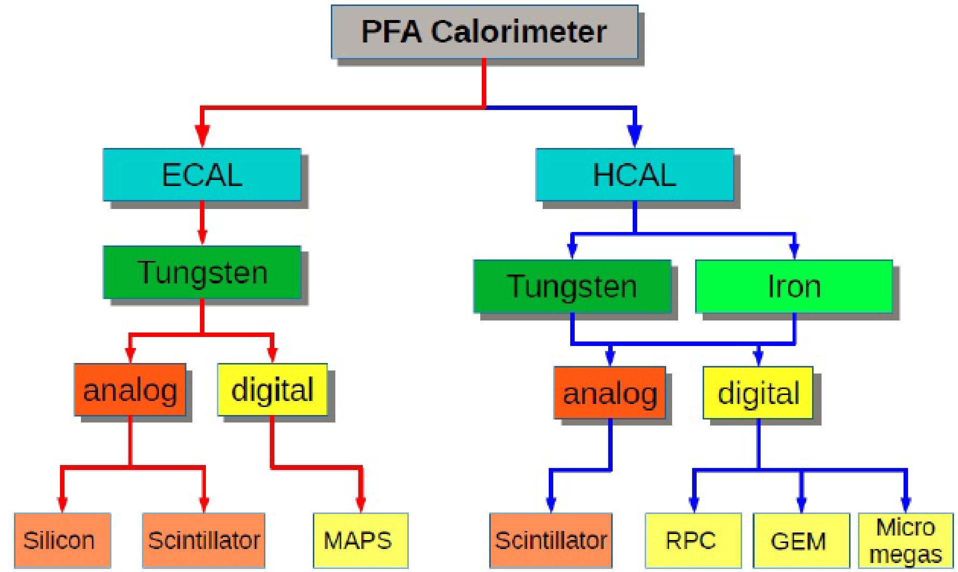
- A prototype of timing electronics
  - Front-end board for MRPC readout
  - Detector interface board
  - DAQ system

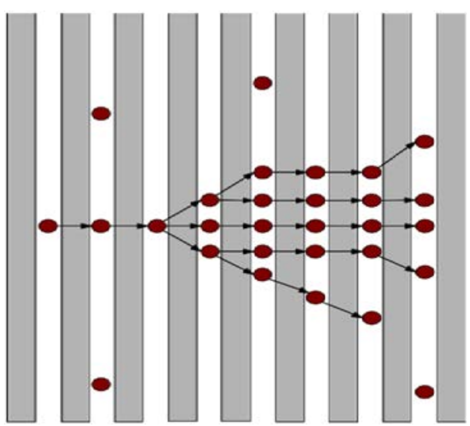
- Summary

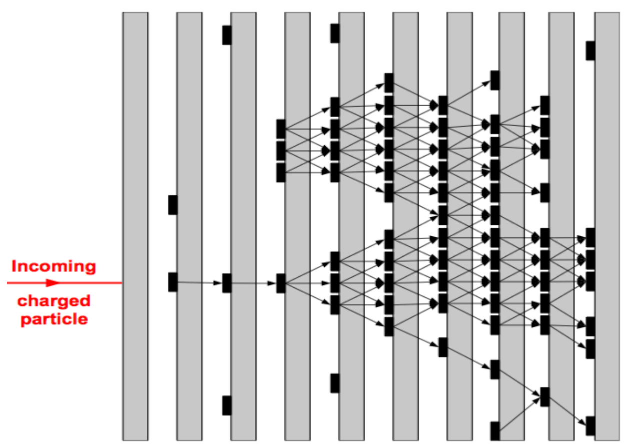
PFA based SDHCAL for CEPC

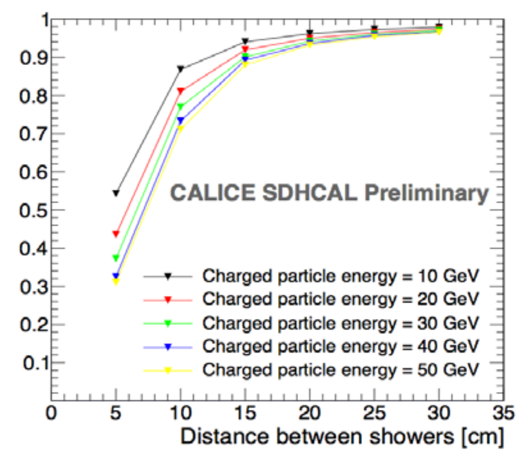
- High granularity PFA
  - Particle Flow Algorithm
  - **Topology** and **energy** information

- PFA algorithm
  - It connect first hits and then their clusters using distance and orientation information, then correct using tracker information



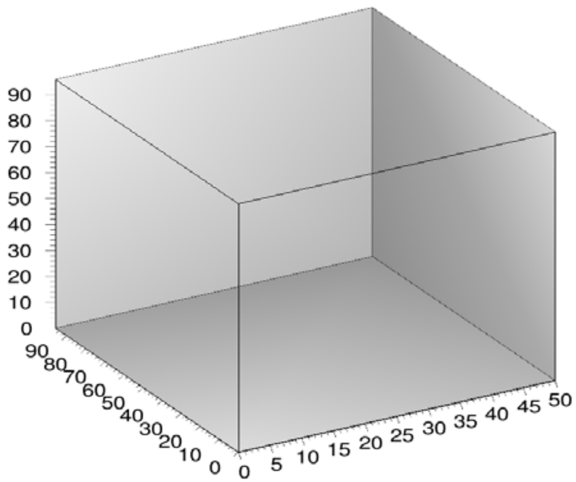


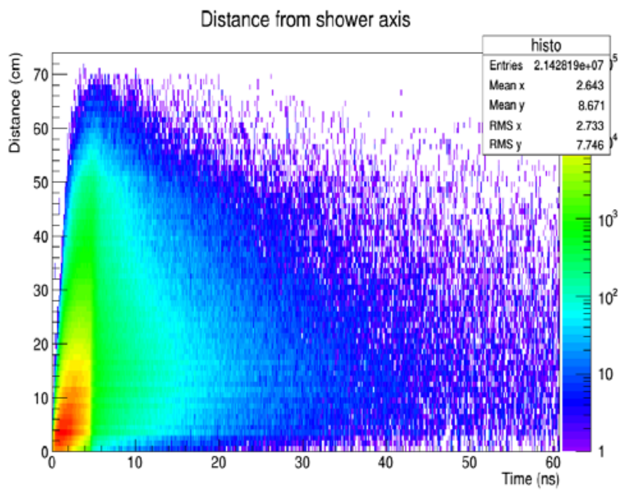


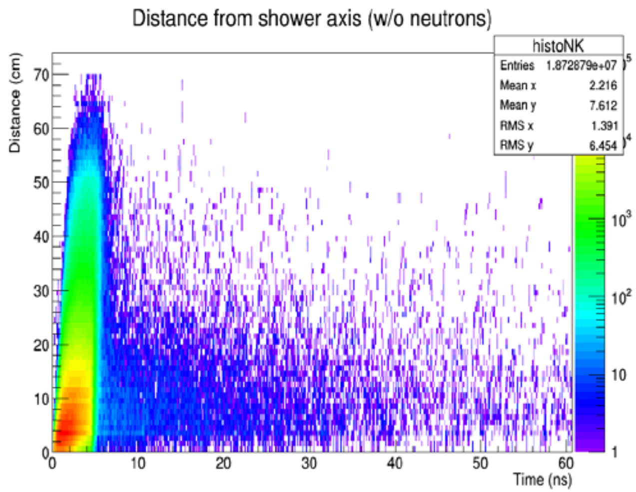


Timing in PFA Calorimeter

Timing could be an important factor to identify delayed neutrons and better reconstruct their energy.

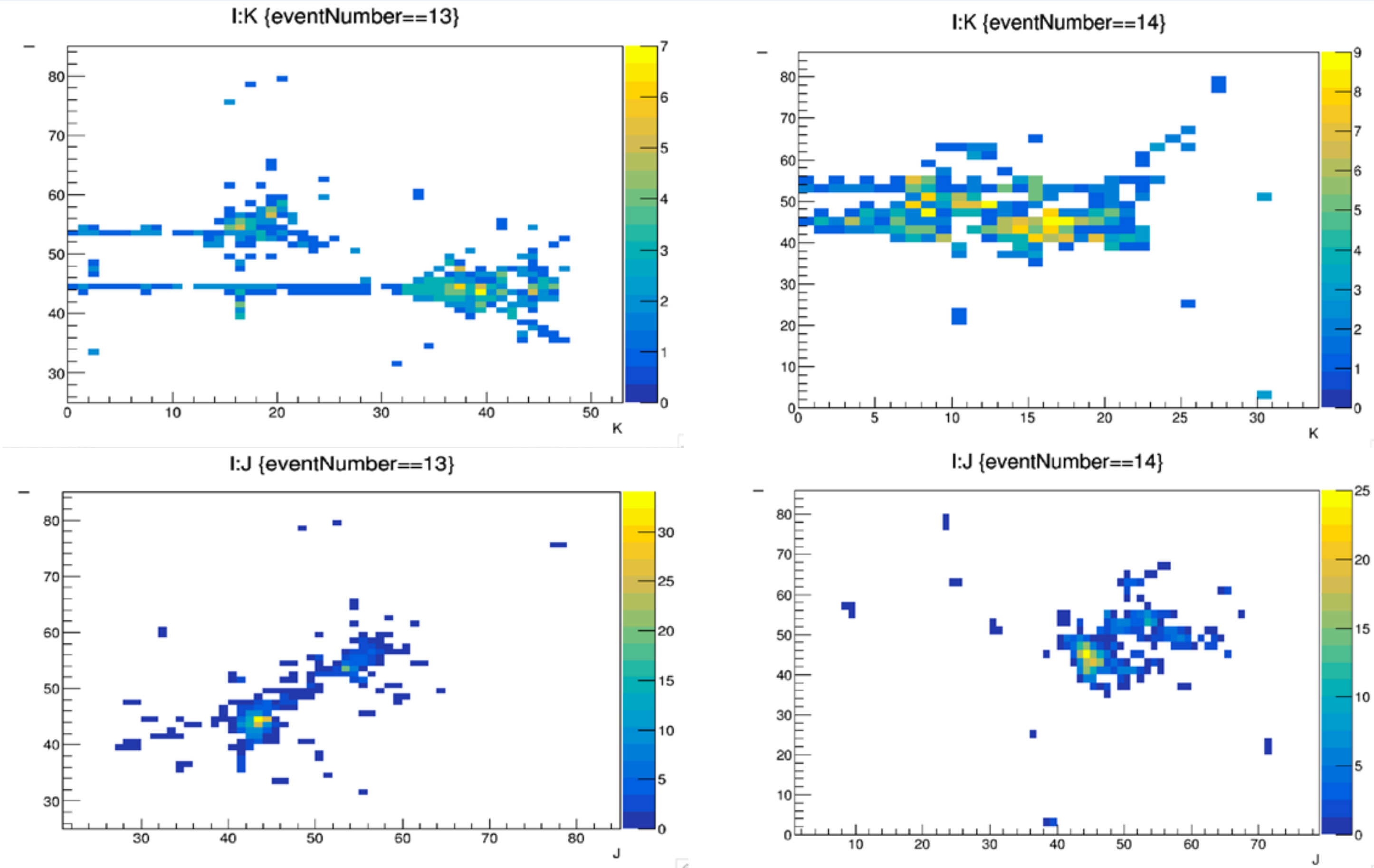






Timing in PFA Calorimeter

- Timing information can help to separate close by showers and reduce the confusion for a better PFA application.
- Example: Pi-(20 GeV), K-(10 GeV)



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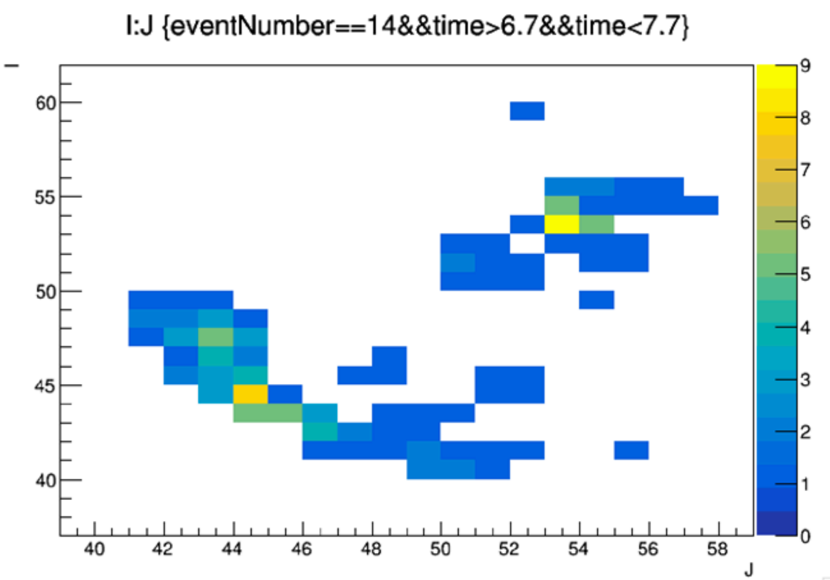
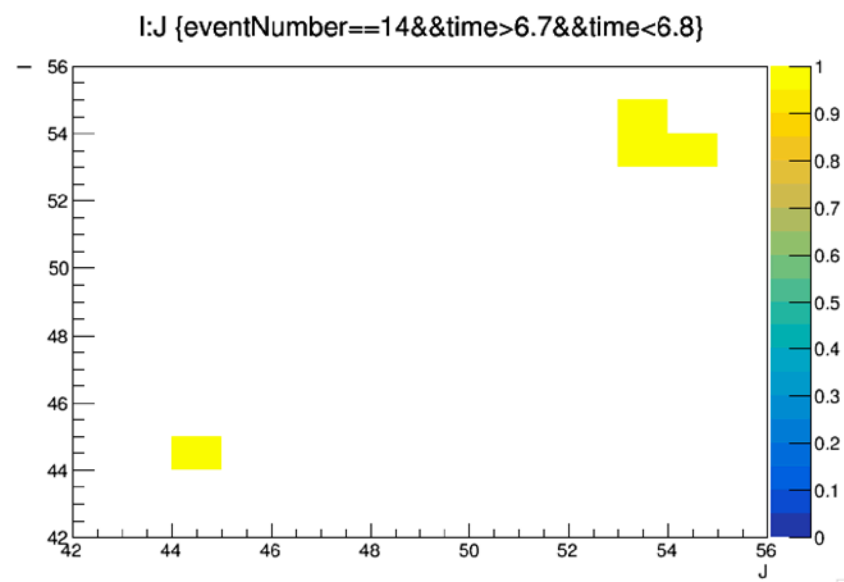


1ns timing resolution



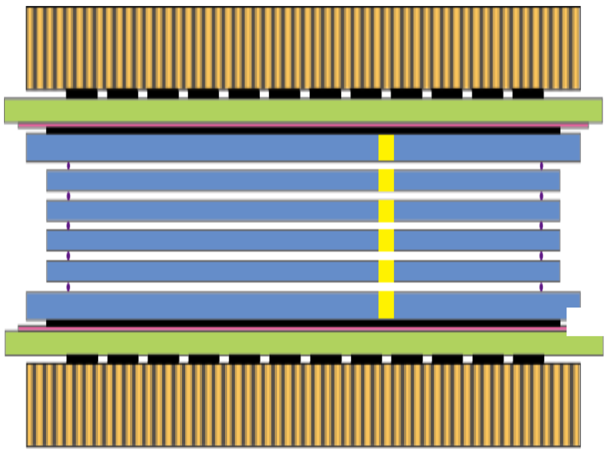
100ps timing resolution

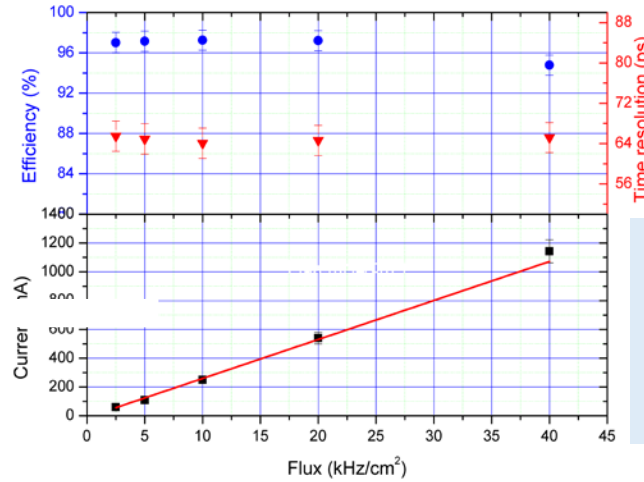
SDHCAL with Timing Measurement

- 5-dimension PFA SDHCAL:
  - Position, Energy and Timing
  - Identify neutral and charged hadrons
- Detector and electronics upgrade
  - High performance timing measurement

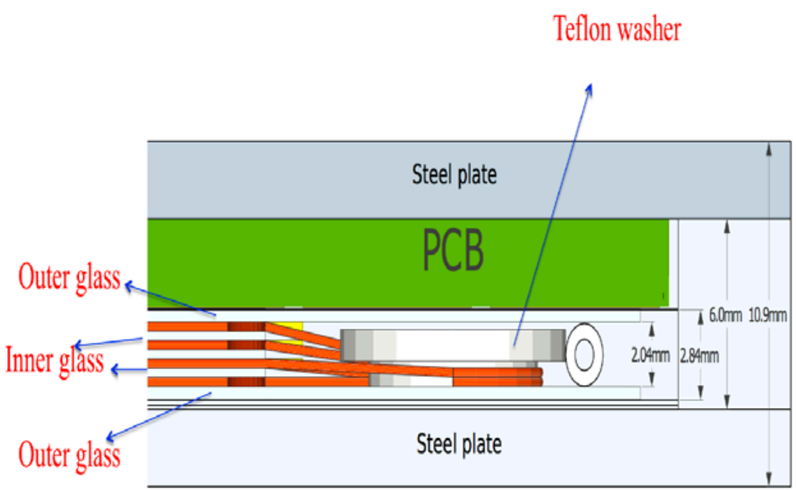
Multi-gap RPC

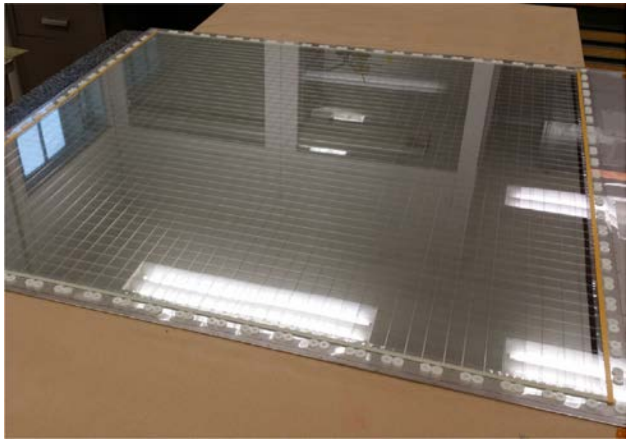
Multi-gap RPC are excellent fast timing detectors





Time resolution of better than 100 ps was obtained with 5-gap RPC by Tsinghua group





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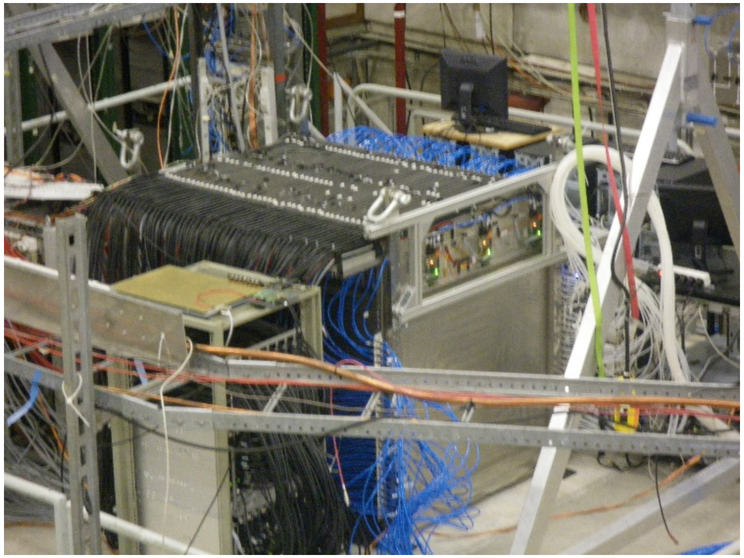
SDHCAL Electronics



SDHCAL Prototype

SDHCAL FE based on HARDROC

SDHCAL prototype
Size: 1m x 1m x 1.4m
No. of layers: 48
Cell size: 1cm x 1cm
No. of channels: 440K
Power: 1mW/ch

- SDHCAL Readout ASIC: HARDROC from Omega group
- Time resolution: time stamping 200ns
- 64 input channels
- 3-threshold: 110fC, 5pC, 15pC

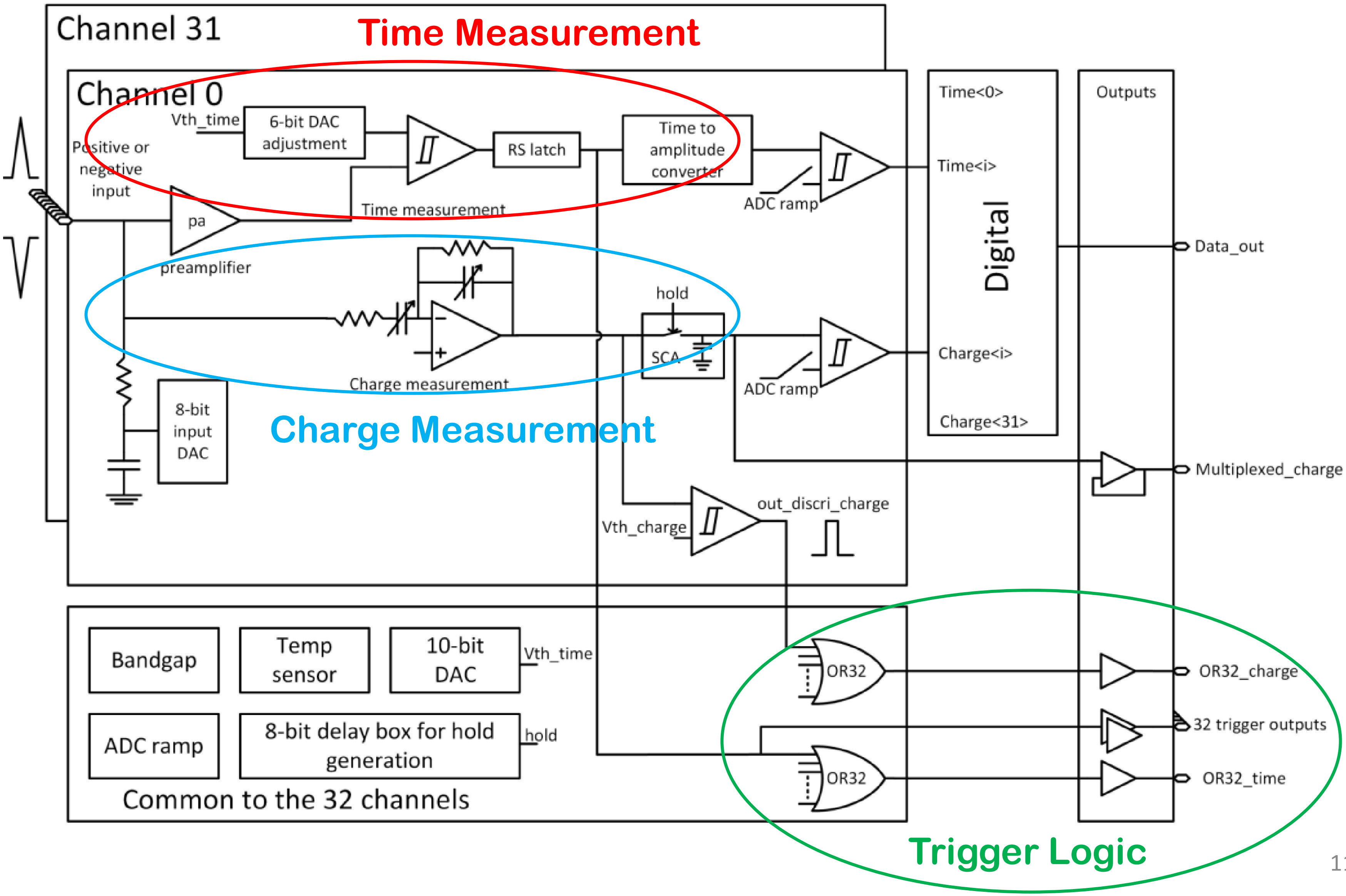
Readout Electronics Upgrade

HARDROC3B

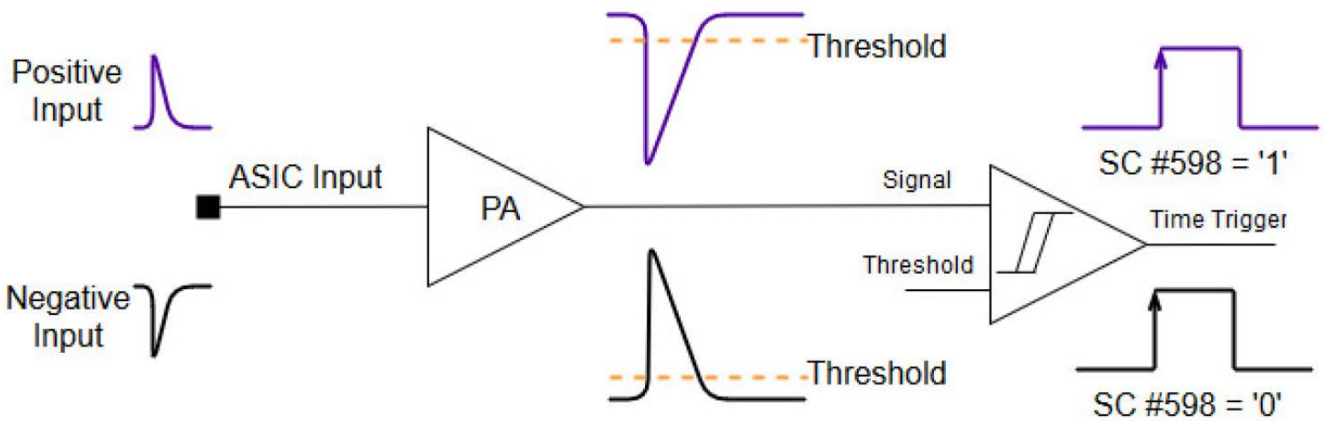
PETIROC2A

- Time measurement with 10 bits TDC interpolating 40MHz clock
  - **Timing resolution below 40 ps**
- Charge measurement with 10 bits DAC
- Other parameters:
  - The 32chs input connected with PCB PAD (detector unit)
  - Each channel split into two parts for charge and time measurement
  - Power consumption (~6mW/channel)

PETIROC2A

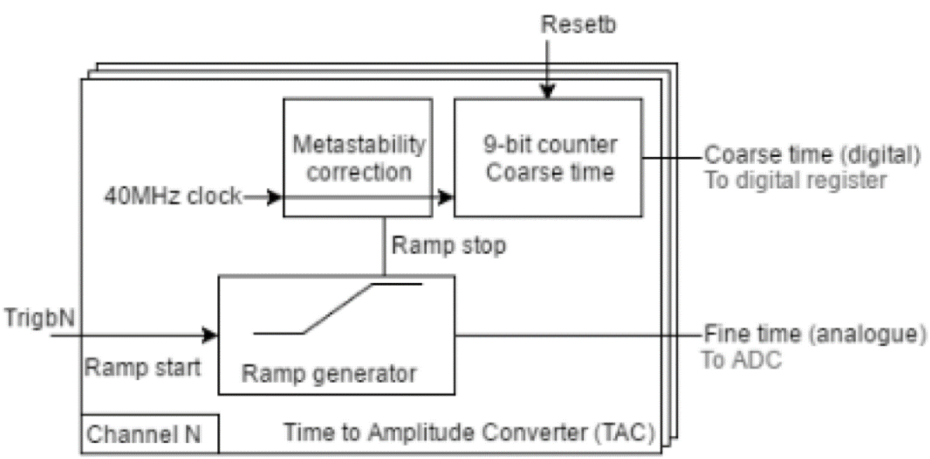

Channel 31
Time Measurement
Channel 0
Vth_time
6-bit DAC adjustment
RS latch
Time to amplitude converter
Positive or negative input
pa
preamplifier
Time measurement
ADC ramp
hold
SCA
Charge measurement
ADC ramp
8-bit input DAC
Charge Measurement
Vth_charge
out_discri_charge
Time<0>
Time<i>
Digital
Charge<i>
Charge<31>
Outputs
Data_out
Multiplexed_charge
Bandgap
Temp sensor
10-bit DAC
Vth_time
ADC ramp
8-bit delay box for hold generation
hold
Common to the 32 channels
OR32
OR32
OR32_charge
32 trigger outputs
OR32_time
Trigger Logic

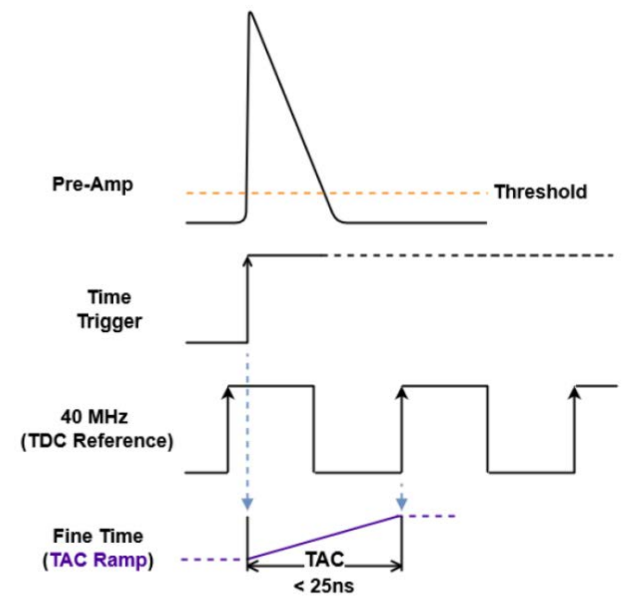
Timing Measurement @ PETIROC2A



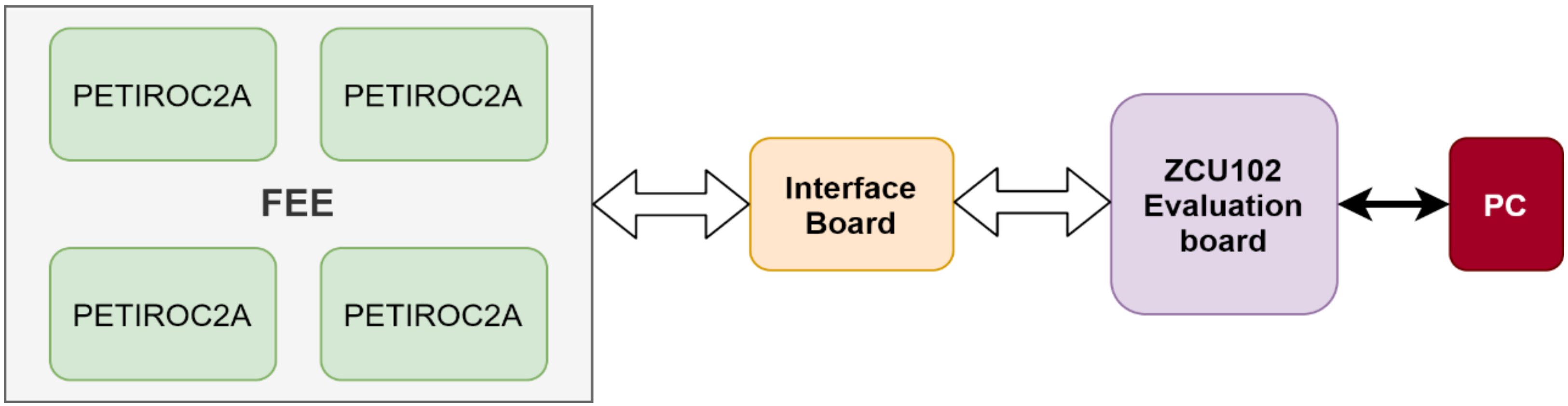
Fast Amplifier

Leading edge timing discriminator





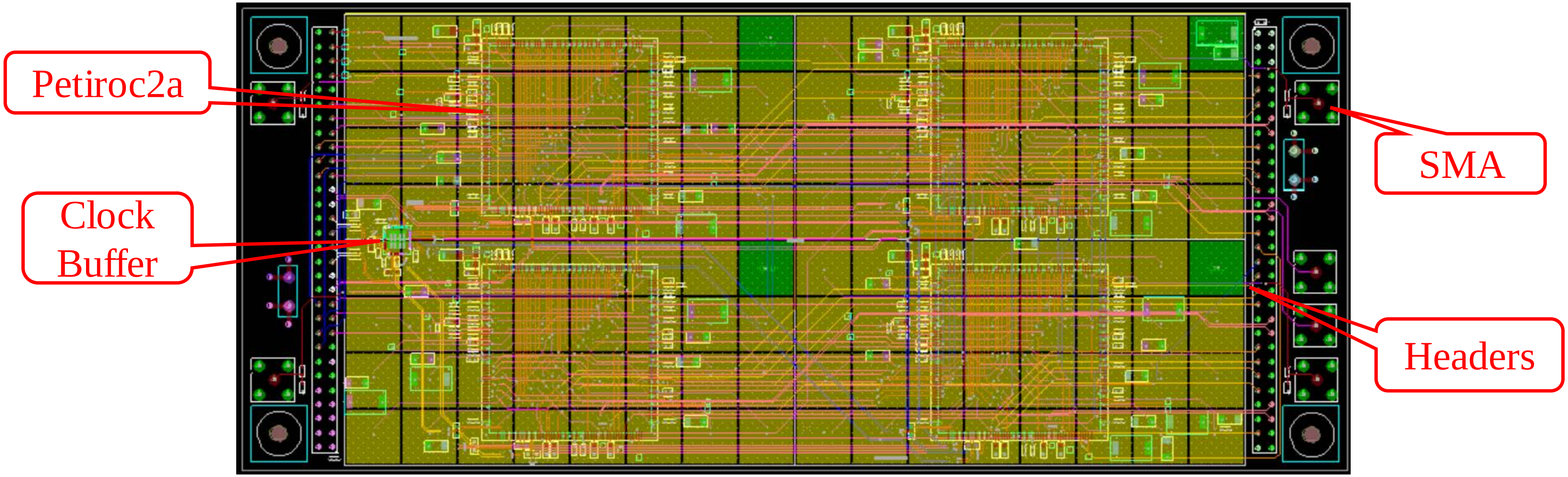
FEE Prototype



Front-end electronics and data acquisition

- First step: Front-End prototype with four PETIROC2A chips
- DAQ system based on commercial Xilinx ZCU102
- Detector Interface (DIF) card for data transfer between the FE electronics and the back-end DAQ

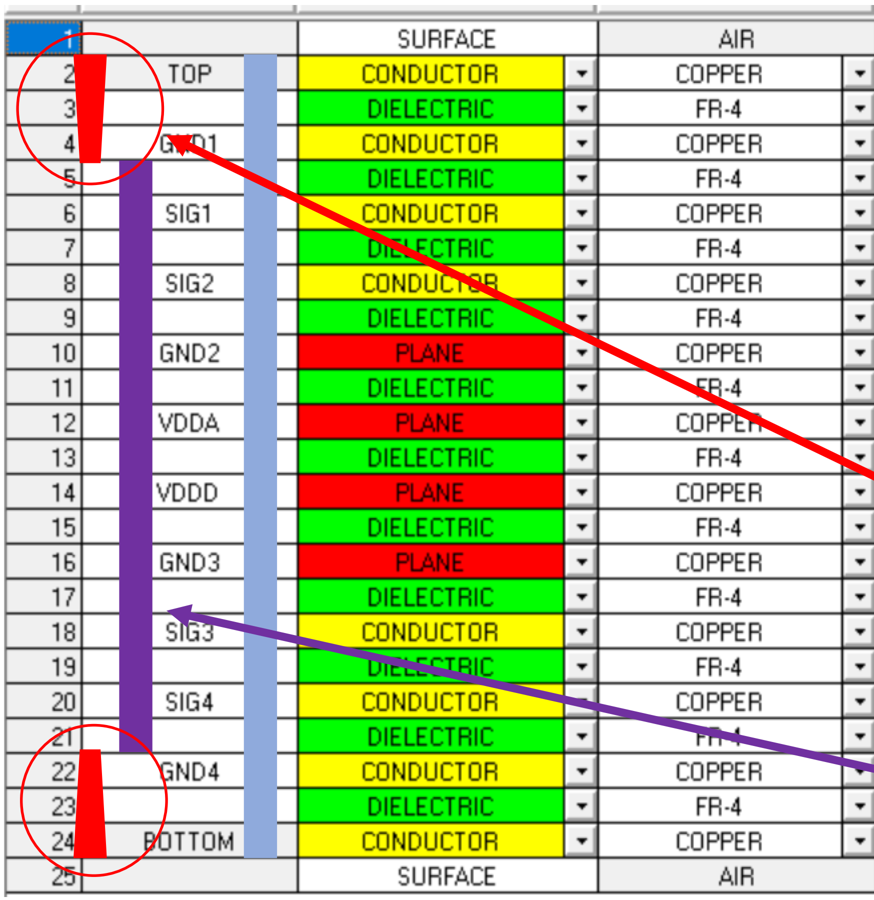
Design of Front-end Board



PCB layout of front-end electronics(prototype board)

- Four PETIROC2A chips
- 128 pads (yellow square) , induction unit size: 1cm×1cm.
- Clock buffer(2:8) for clock signal (40MHz and 160MHz)
- Two headers for communication with DAQ
- SMA for injection test.

Design of Front-end Board

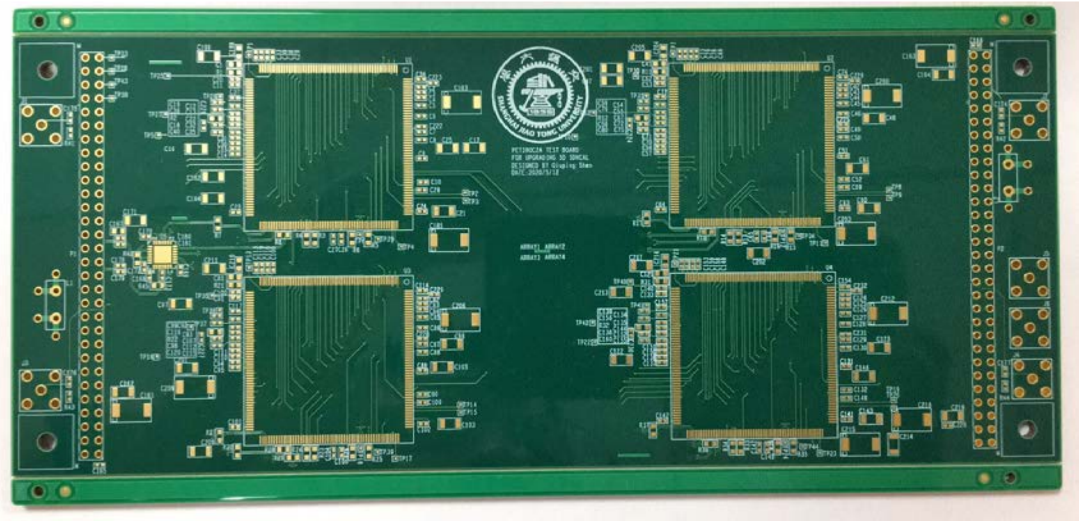


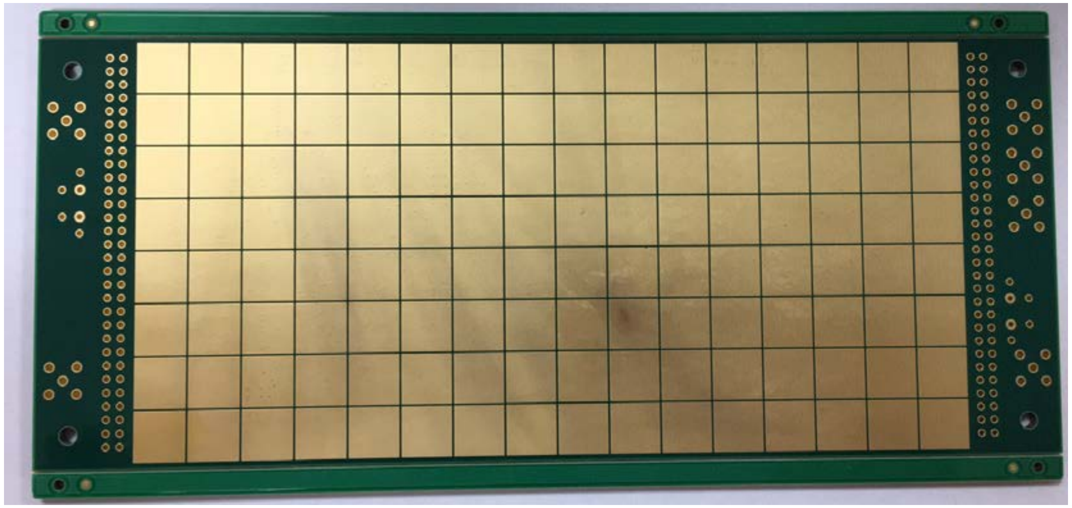
Stack-up and via design

- 12 layers PCB
- Many induction units are at the bottom

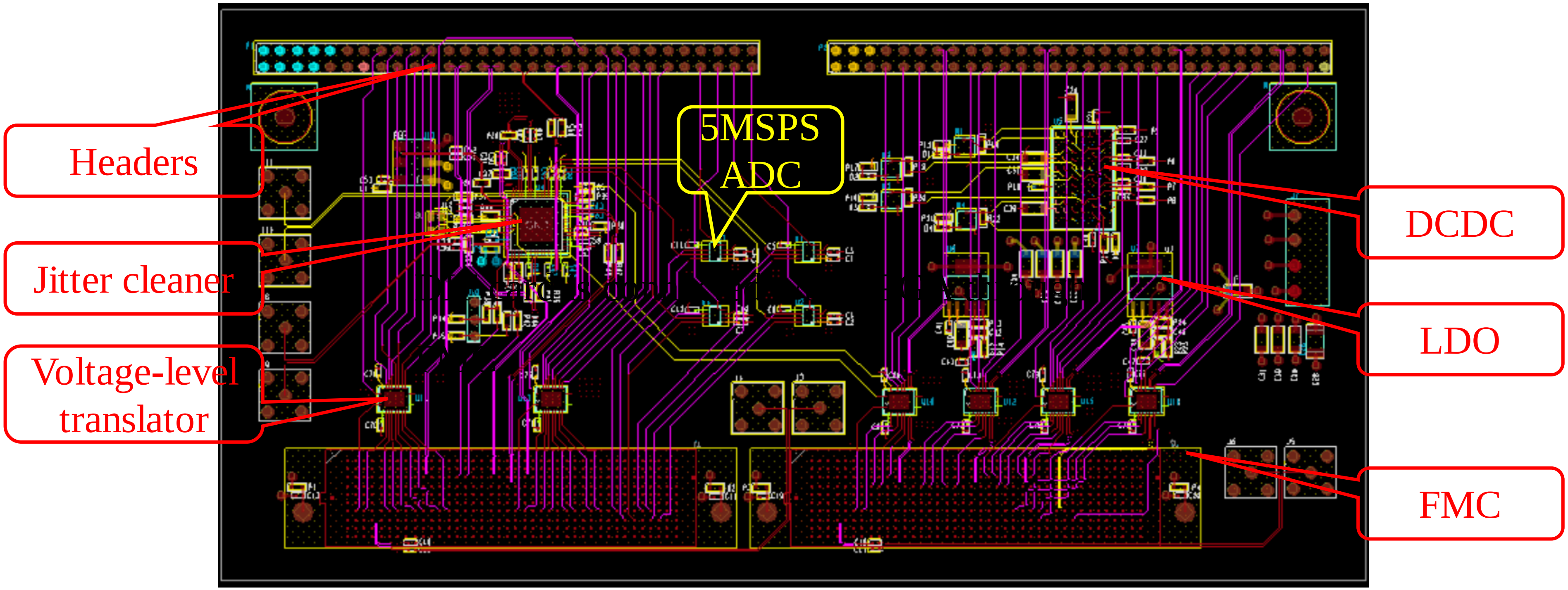
- Via technology:
  - Laser-drilled Via Technology (small size: ~0.1mm) between outside two layers
  - Buried Vias with the size 0.3mm

Front-end Board





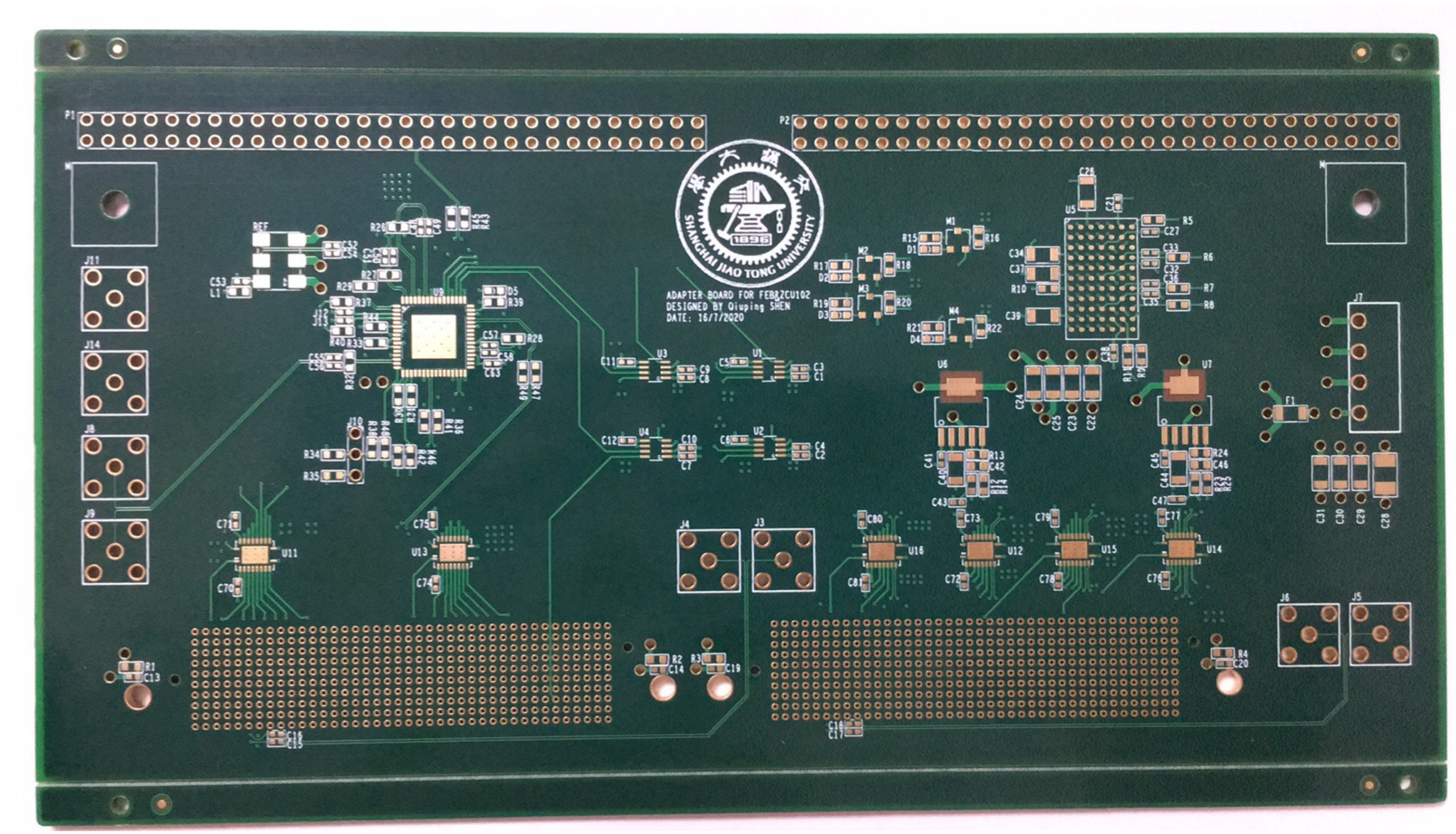
Detector Interface Card



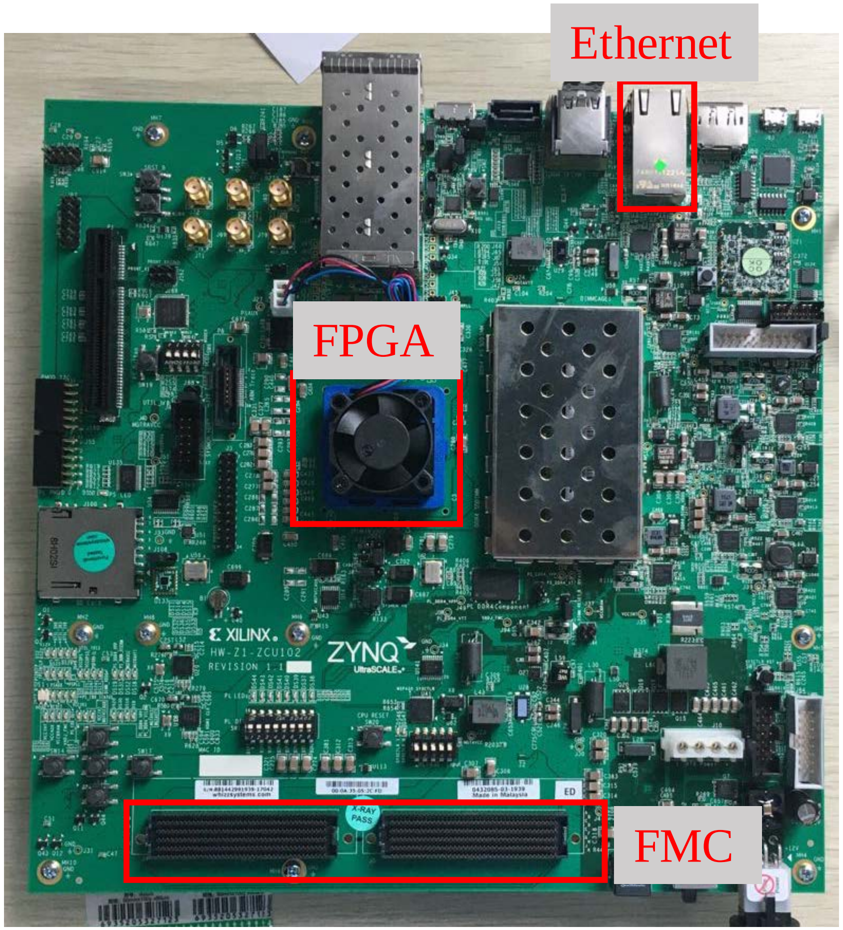
PCB layout of DIF card

- Voltage regulator
- Voltage level shifter
- Jitter cleaner (SI5345)
- Slow ADC (5MSPS)

Detector Interface Card



DAQ Board



Xilinx ZCU102

- FPGA: ZYNQ UltraScale+ MPSoC
  - SFP, Ethernet, DDR4 etc.
- 2x FMC-HPC connectors
  - 128 single-ended or 64 diff signals
  - 66 I/O used for four petiroc2a chips
- Ethernet communication
- FPGA design is ongoing.

Summary

- The timing information is very useful for SDHCAL; it help identify neutrons and charged particles.
  - MRPC can achieve 100ps timing resolution
  - PETIROC used as readout ASIC, supporting <40 ps timing resolution
- The design of a front-end prototype (with four PETIROCs) and a interface card has been completed.
  - Laser-drilled vias and buried vias are used for the FE board, due to induction pads at the bottom.
- The Xilinx ZCU102 board will be used as the DAQ system. The FPGA design is ongoing.