UNIVERSITY OF BIRMINGHAM

65nm CMOS imaging process for a high resolution pixel detector

Laura Gonella (University of Birmingham) with inputs from Walter Snoeys (CERN)

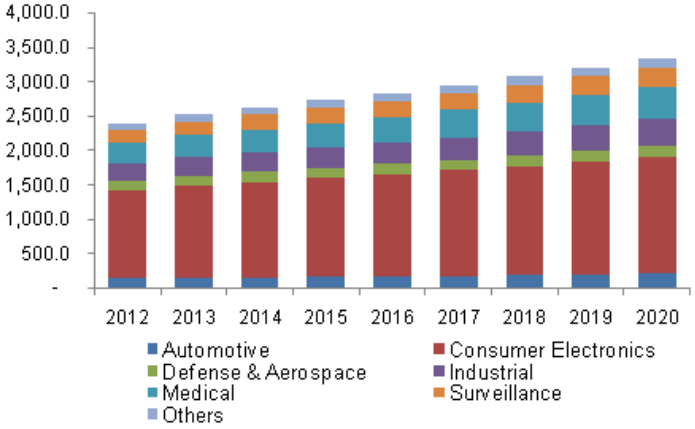
CEPC Workshop, 26 October 2020

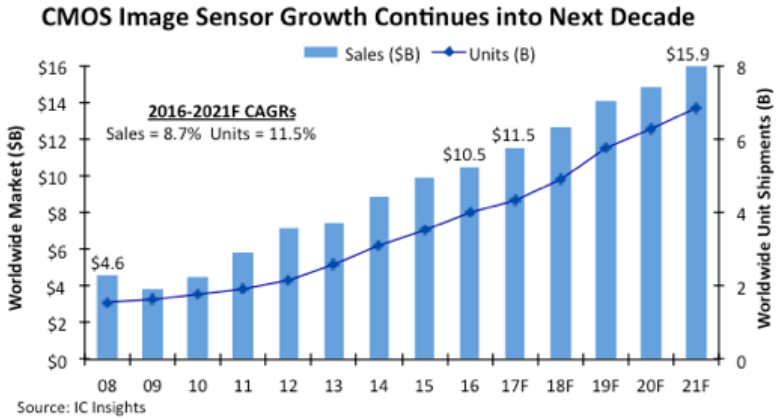
Overview

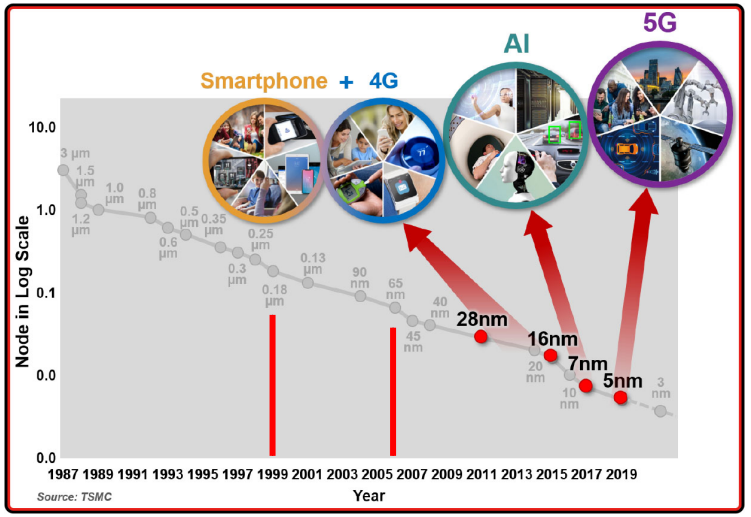
- CMOS imaging technology and HEP
- 65 nm CMOS imaging technology
- First target applications of 65 nm MAPS
  - ALICE ITS3 project
  - EIC SVT
- Status of design activities
- Conclusion

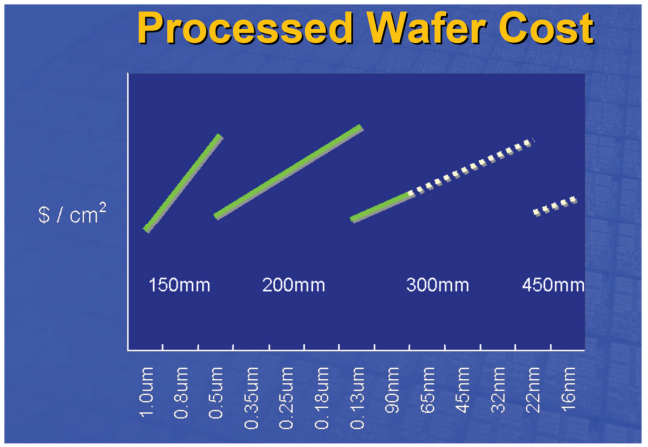
CMOS imaging technology

- Fast technology evolution and large market driven by various commercial applications
- Reduced processing costs per area with the introduction of larger wafer size (300 mm)







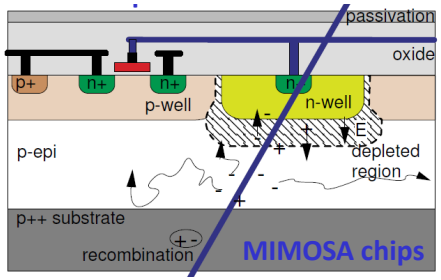


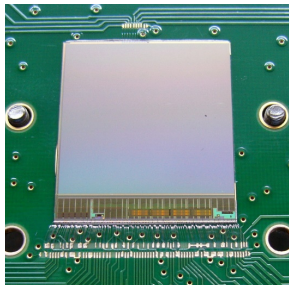
Source: Holt (2005).

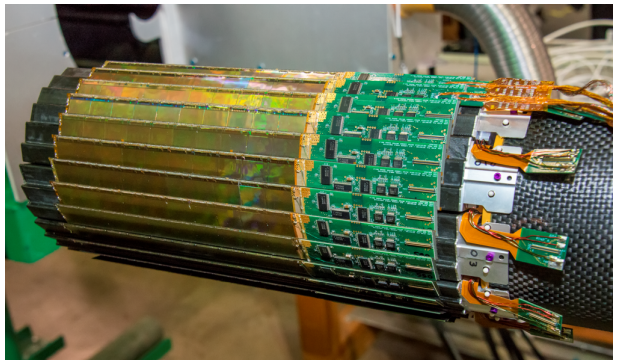
CMOS in HEP

MIMOSA 28 @ STAR HFT

First MAPS in an experiment
Twin well 350 nm AMS (NMOS only)
Integration time 190 us
Rolling shutter readout
NIEL tolerance 10^{12} n_{eq}/cm^2
MIMOSA sensors used in many applications, for instance EUDET telescope

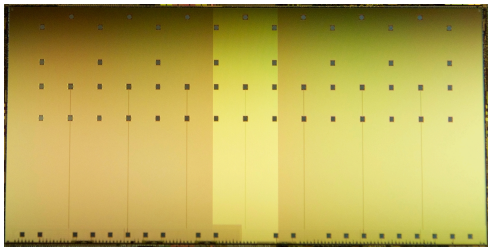


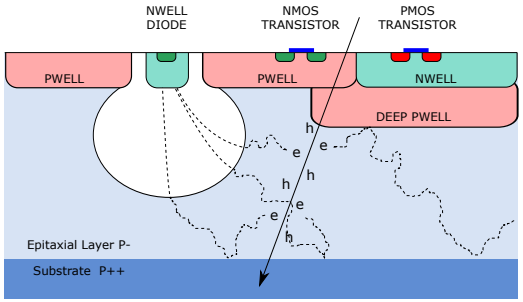


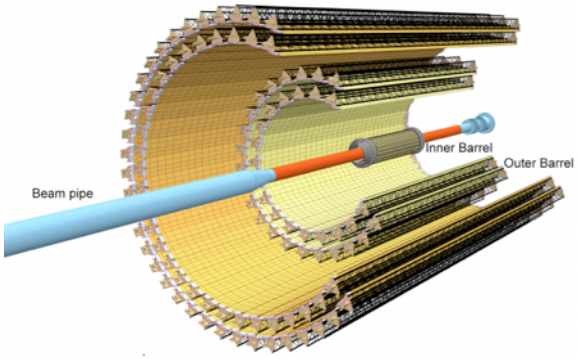


ALPIDE @ ALICE ITS

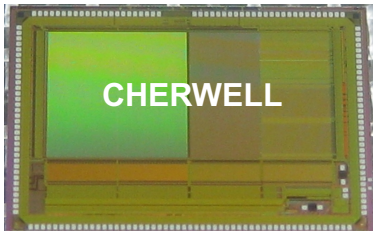
Quadruple well 180 nm TJ
Partially depleted, full CMOS
Integration time 4 us
NIEL tolerance few 10^{13} n_{eq}/cm^2
Also used at sPHENIX (BNL), NICA MPD (@JINR), …

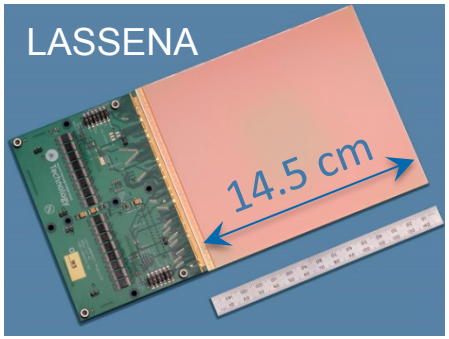


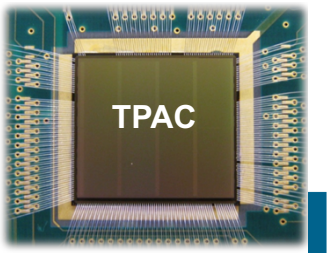


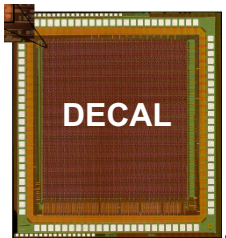


More sensors in this technology…









CMOS in HEP

W. Snoeys et al NIMA 817 (2017)
M. Dyndal et al 2020 JINST 15 P02005
K. Moustaks et al NIMA 936 (2019) 604-607
H. Augustin et al NIMA 936 (2019) 681-683

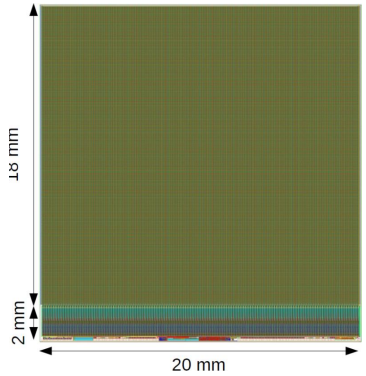
R. Cardella et al 2019 JINST 14 C06019
I. Caicedo et al 2019 JINST 14 C06006
T. Hirono et al NIMA 924 (2019) 87-91
R. Schimassek https://doi.org/10.1016/j.nima.2020.164812

Fully depleted MAPS

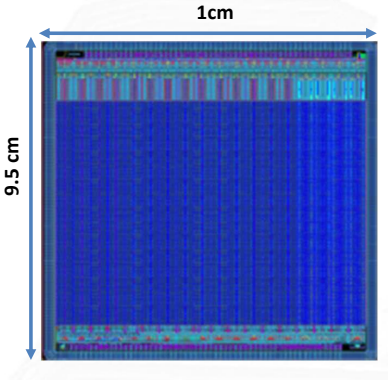
Latest generation prototypes
Demonstrated HL-LHC rate capability and radiation hardness

Large collection electrode:

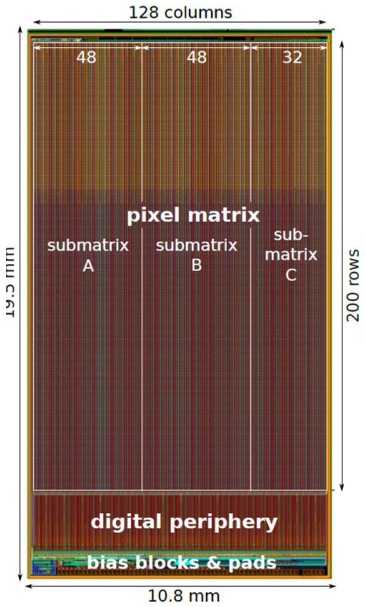
ATLASPix3 180 nm TSI



LF-MONOPIX 150 nm LFoundry

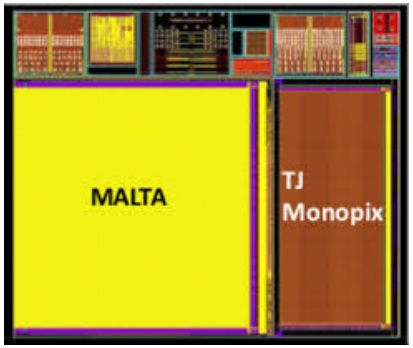


MuPix8 @ mu3e
180 nm AMS



Small collection electrode (with process modification):

MALTA and TJ-MONOPIX
180 nm TJ



… and more, see also RD50 developments

Motivations for 65 nm in HEP

- State-of-the-art MAPS for HEP use 180 nm CMOS imaging technologies
  - These technologies are now around 20 years old

- Proposed future HEP facilities, planned over the next few decades will need improved performance in terms of granularity, power consumption, rate and radiation hardness → smaller feature size technology needed

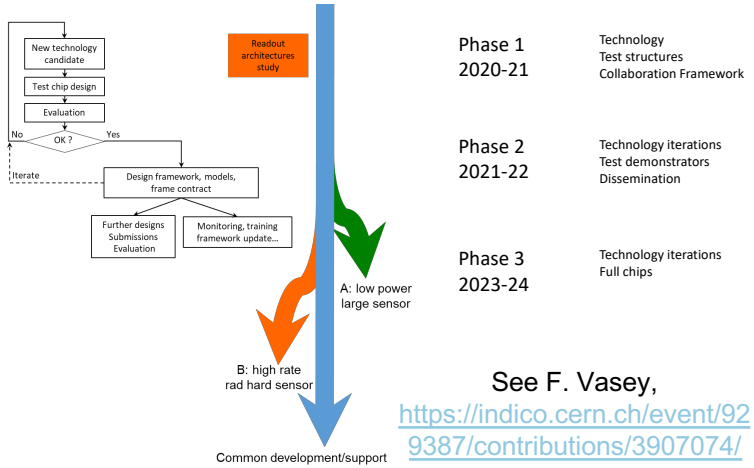
- The HEP community is starting exploration of 65 nm technologies
  - Higher logic density (increased performance/area, higher granularity)
  - Lower power
  - Higher speed (logic, data transmission…)
  - Process availability
  - Higher NRE costs and complexity, but lower price per area

CERN EP R&D programme: WP1.2 MAPS

- Evaluate technology candidates for the development MAPS for future HEP experiments
  - 65 nm, further studies of TJ 180 nm process, more advanced nodes

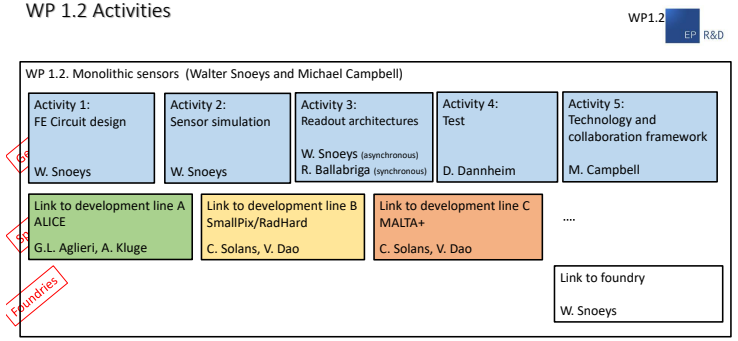
- Work is organised around three areas
  - Technology selection and validation
  - Pre-prototyping of a large, low-power and high-resolution sensor (ITS3 sensor for ALICE/e+e-)
  - Pre-prototyping of a fast and rad hard sensor (for high luminosity general purpose experiments)

WP 1.2 Timeline



See F. Vasey, https://indico.cern.ch/event/929387/contributions/3907074/

WP 1.2 Activities



WP leaders:
Walter Snoeys, Michael Campbell

First technology selection

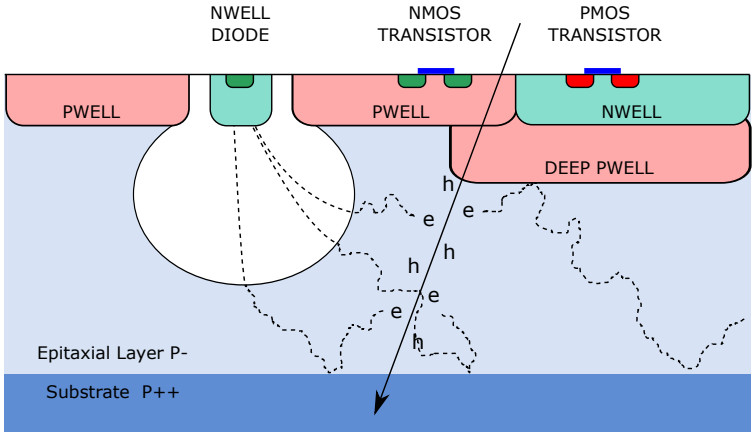
- Several 65 nm flavours: high density logic, RF, and imaging (ISC)

- ISC preferred
  - 2D stitching experience, special sensor features, lower defect densities, at present limited to 5 metal layers but more metals later, no MPWs available

- Modus operandi agreed by foundry in May: start directly in ISC with Multiple Layers per Reticle with standard metal stack
  - Avoid non-representative results (for transistor irradiation measurements)
  - Multiple Layer per Reticle (in between MPW and engineering run)
  - Several starting materials available; the collection electrode is always n-type, the same readout circuit can be used for different starting materials

Starting material: first possibility

- Similar sensor structure possible as in ALPIDE
  - Deep wells available
  - High resistivity p-type epitaxial layer ~ 10 micron thick
  - Depending on pixel size and area taken by readout, sensitive layer not necessarily fully depleted



J. Phys. G: Nucl. Part. Phys. 41 (2014) 087002

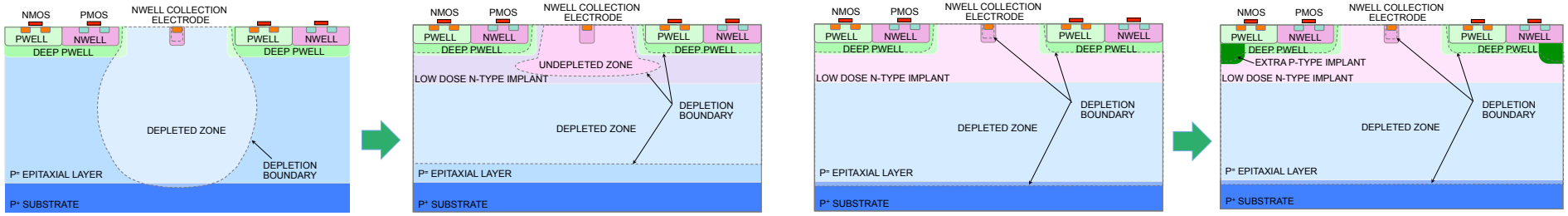
See W. Snoeys,
https://indico.cern.ch/event/929387/contributions/3907086/attachments/2063152/3585457/WP1-2_24_6_2020_b.pdf

Starting material: Other options

- Move junction away from collection electrode
  - full depletion, better time resolution and increased radiation hardness

Example 180 nm

Main damage mechanism: displacement damage (Non-Ionizing Energy Loss or NIEL)
Collect signal charge FAST before it gets trapped => depletion and large electric field…



Standard, not fully depleted

Not fully depleted at low reverse bias

Depletion at higher reverse bias

Further improvements by influencing the lateral field

Additional implant for full depletion => order of magnitude improvement

Side development of ALICE for ALPIDE

NIMA 871 (2017) pp. 90-96 https://doi.org/10.1016/j.nima.2017.07.046

Triggered development in ATLAS H. Pernegger et al, 2017 JINST 12 P06008

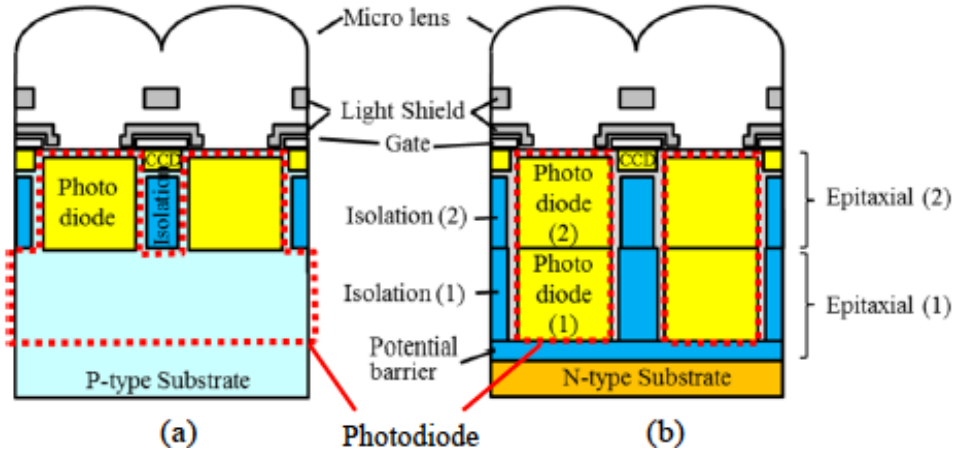
See W. Snoeys,
https://indico.cern.ch/event/929387/contributions/3907086/attachments/2063152/3585457/WP1-2_24_6_2020_b.pdf

Starting material: Other options

Novel Pixel Structure with Stacked Deep Photodiode to Achieve High NIR Sensitivity and High MTF

Hiroki Takahashi, Hiroshi Tanaka, Masahiro Oda, Mitsuyoshi Ando, Naoto Niisoe, Shinichi Kawai*, Takuya Asano*, Minoru Sudo*, Mitsugu Yoshita*, Tohru Yamada*
TowerJazz Panasonic Semiconductor Co., Ltd. 800 Higashiyama, Uozu City, Toyama 937-8585, Japan
*Panasonic Semiconductor Solutions Co., Ltd. 1 Kotari-yakemachi, Nagaokakyo City, Kyoto 617-8520, Japan

DOI: 10.1109/VLSIT.2016.7573450



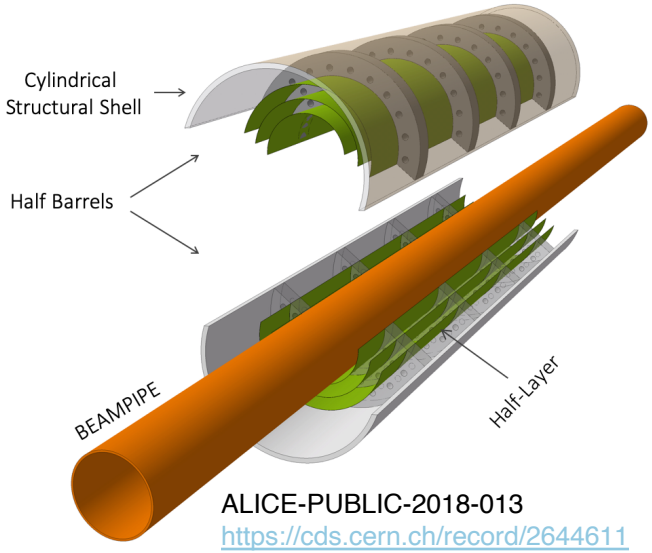
- Already in production for visible light
- Single thickness or double (stacked)
- Also here the junction is displaced from the collection electrode with similar advantages
- Can be explored perhaps in a second phase
- One example out of several starting material options
- Readout circuit agnostic (collection electrode remains n-type)

See W. Snoeys,
https://indico.cern.ch/event/929387/contributions/3907086/attachments/2063152/3585457/WP1-2_24_6_2020_b.pdf

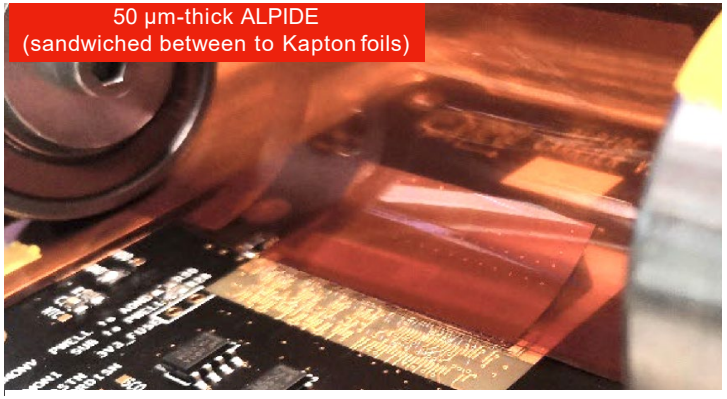
ALICE ITS3 vertex detector

- The ALICE ITS3 project aims at developing a new generation MAPS sensor at the 65 nm node coupled with R&D into extremely low X/X_0 truly cylindrical vertex detection for the HL-LHC
  - See M. Mager's talk later today

- Sensor features: low power; large area, stitched; ultra thin and bent



ALICE-PUBLIC-2018-013
https://cds.cern.ch/record/2644611



https://www.jlab.org/indico/event/400/contribution/10/material/slides/0.pdf

ITS3 sensor specifications

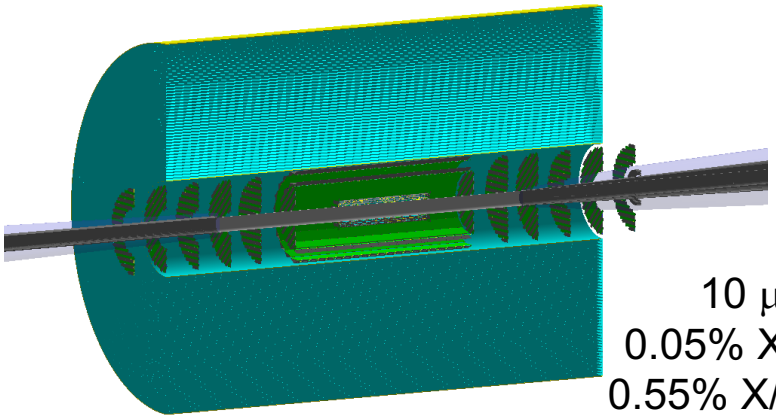
Specifications

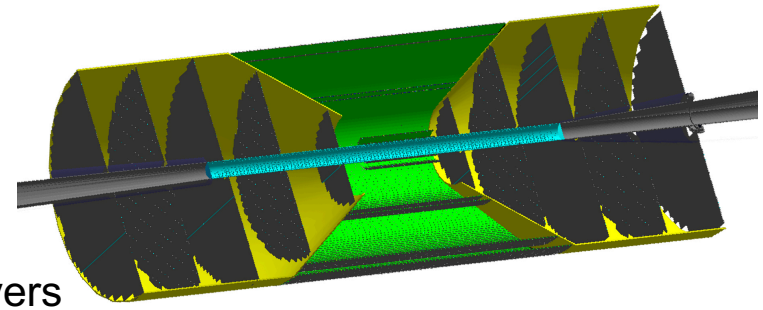
Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 µm	20-40 µm
Pixel size	27 x 29 µm	O(10 x 10 µm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 µs	~ 200 ns
Time resolution	~ 1 µs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm^2	100 MHz/cm^2
Max particle readout rate	10 MHz/cm^2	100 MHz/cm^2
Power Consumption	40 mW/cm^2	< 20 mW/cm^2 (pixel matrix)
Detection efficiency	> 99%	> 99%
Fake hit rate	< 10^{-7} event/pixel	< 10^{-7} event/pixel
NIEL radiation tolerance	~3 x 10^{13} 1 MeV n_{eq}/cm^2	10^{14} 1 MeV n_{eq}/cm^2
TID radiation tolerance	3 MRad	10 MRad

EIC SVT

- A well integrated, large acceptance Silicon Vertex and Tracking (SVT) detector designed with high granularity and low material budget is planned for the Electron-Ion Collider to enable high precision measurements that are key to its science programme
  - Expected start of operation approximately 2030

- Two baseline configurations are studied, based on ITS3 sensor technology
  - Hybrid, i.e. silicon SVT complemented by gas outer tracker and end-caps, ~12m^2
  - All-silicon compact design, ~15m^2
  - Vertex and tracking layers in the central region, disks in the forward/backward region





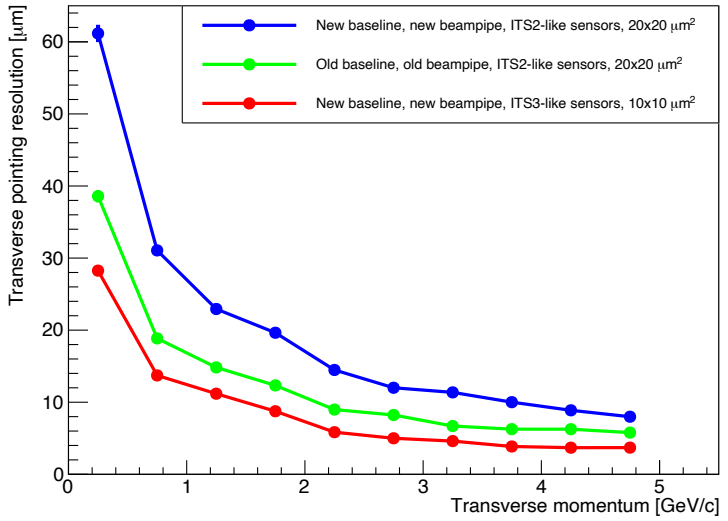
10 μm pixel pitch
0.05% X/X_0 vertex layers
0.55% X/X_0 tracking layers
0.24% X/X_0 disks

ITS3-derived EIC SVT

- Common development with ITS3
  - ITS3 sensor specifications meet or even exceed the EIC requirements
  - Timescale largely compatible
- Studies are ongoing to adopt the ITS3 detector concept for the vertex layers
  - Needed to achieve the required vertex resolution with larger diameter beam pipe
- Cost and yield of stitched wafer-scale sensors not compatible with use in the EIC detector outside the vertex layers → a reticle-size sensor version needed for the EIC tracking layers and disks

Preliminary EIC MAPS sensor requirements

Parameter	EIC Vertex and Tracking MAPS
Technology	65 nm (Backup: 180 nm)
Substrate Resistivity [kohm cm]	1 or higher
Collection Electrode	Small
Detector Capacitance [fF]	<5
Chip size [cm x cm]	Full reticule or stitched
Pixel size [μm x μm]	20 x 20
Integration Time [μs]	2
Timing Resolution [ns]	< 9 (optional)
Particle Rate [kHz/mm^2]	**TBD**
Readout Architecture	Asynchronous
Power [mW/cm^2]	< 20
NIEL [1MeV neq/cm^2]	10^{10}
TID [Mrad]	< 10
Noise [electrons]	< 50
Fake Hit Rate [hits/s]	< 10^{-5}/evt/pix
Interface Requirements	**TBD**



eR25 project; Birmingham, LBNL, RAL;
https://wiki.bnl.gov/conferences/images/6/6d/ERD25-Report-FY21Proposal-Jun20.pdf

Technology exploration and sensor design status

- Collaborative framework being prepared by CERN in discussion with interested institutes in the EP R&D WP1.2, pursuing monolithic sensors development in more advanced technologies

- Technology exploration planned over two MLR runs
  - Work on MLR1 is being finalized, in a collaboration with several institutes, see next slide
  - MLR2 to follow, possibly next year, other institutes joining to participate

- Technology investigation and sensor development also driven by the first application, the ITS3 effort toward a large area, low power and high resolution sensor for the inner pixel layers of the ALICE experiment

- Full stitched sensor development planned over three engineering runs

Technology access and progress on MLR1

- Initial exploration of technology
  - Transistor test structures and ring oscillators for radiation hardness studies
  - Analogue pixel test structures for charge collection studies
  - Prototype IP blocks: bandgap reference, LVDS and CML line driver, …

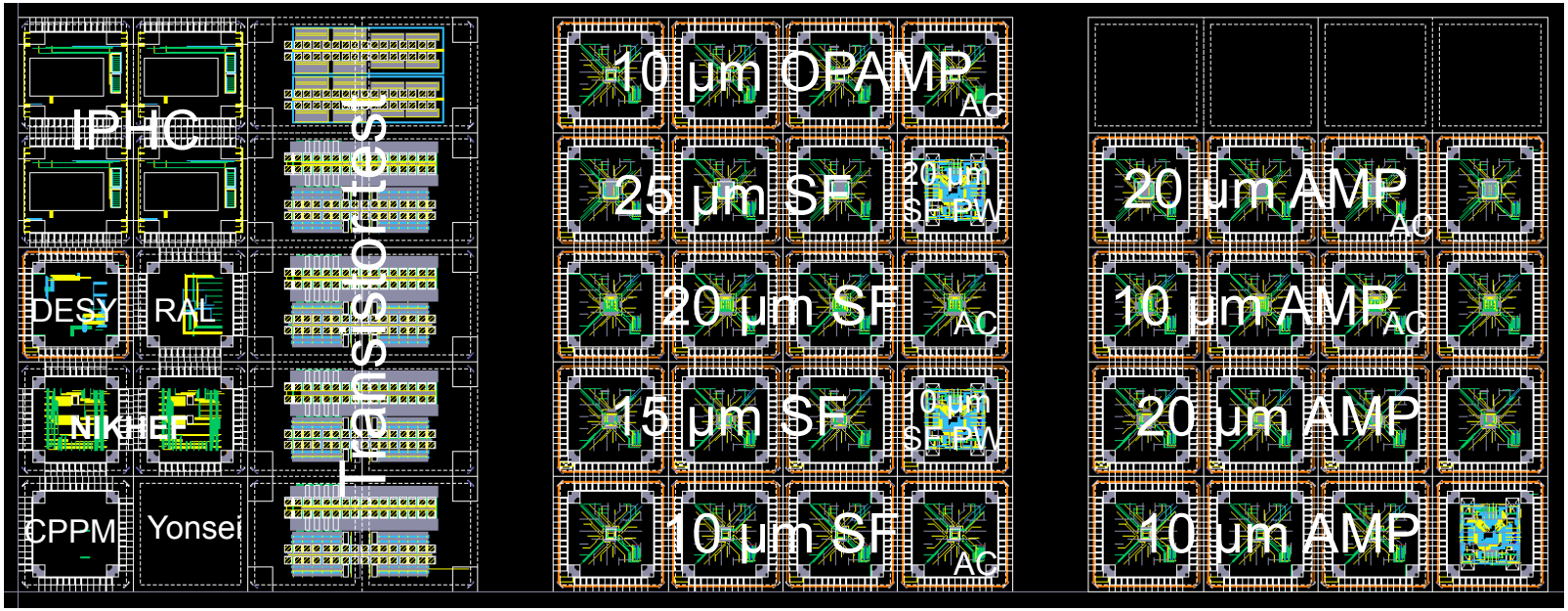
- Participating institutes
  - CERN, CPPM, DESY, Yonsei University Seoul, IPHC Strasbourg, NIKHEF Amsterdam, RAL/Uni Birmingham/LBNL (EIC institutes)

- Access cleared for participating groups mid July (Yonsei end of August), PDK installed immediately after

- Excellent contact with foundry

MLR1

- Significant amount of work by all designers in the different teams
  - Several questions on devices, design rules and others gathered and addressed to foundry
  - Challenging but significant learning
  - At present everyone on full-custom flow, IPHC put in place first digital flow
- Mock tape-out exercised in September, submission planned 15 November



MLR integration in progress

Still in evolution

Conclusion

- The HEP community is starting exploration of 65 nm CMOS imaging technologies to develop MAPS in more advanced technologies
  - Improved performance, lower cost/unit area …

- Work also driven by the ALICE ITS3 project toward the design of a large area, low power, high resolution MAPS sensor for the HL-LHC
  - Interesting for other applications (EIC already participating, planned e+e- colliders)

- First technology selected, modus operandi agreed with foundry, access to PDK in place and first submission scheduled on 15th of November