Status of the TaichuPix chip for the high-rate CEPC Vertex Detector

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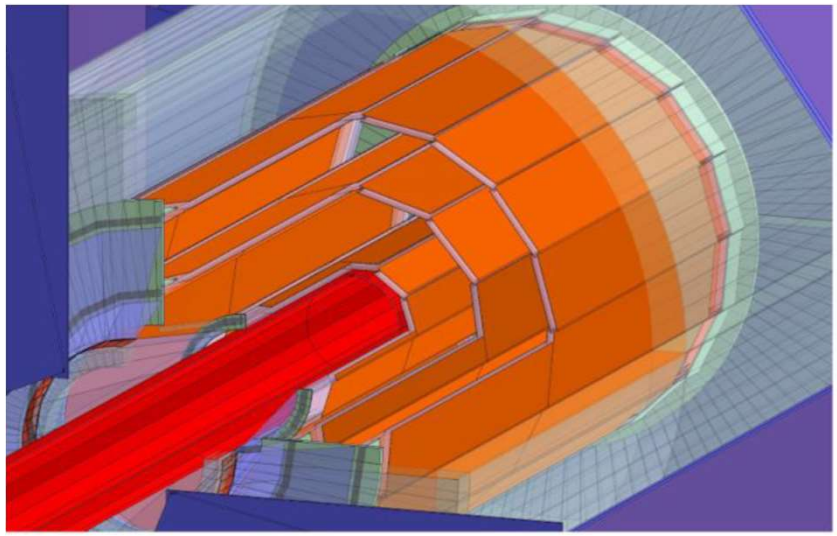
On behalf of the CEPC MOST2 Vertex detector design team

2020-10-26

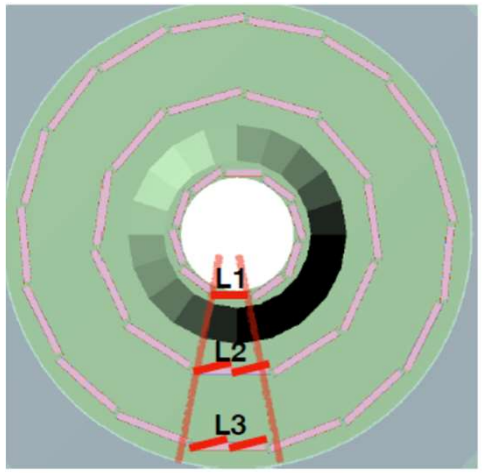
Outline

- **TaichuPix concept for high rate CEPC vertex detector**
- **Chip architecture**
- **Preliminary test results**

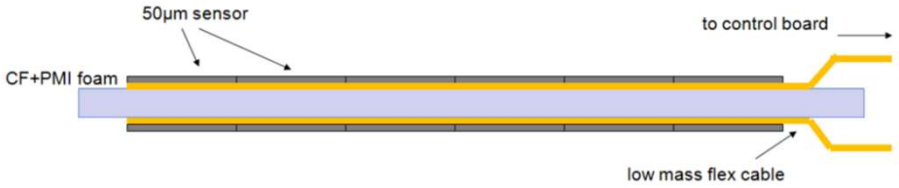
CEPC Vertex Detector Concept



3-layers of double-sided pixel sensors



		R(mm)	|z|(mm)	σ(μm)
Ladder1	Layer1	16	62.5	2.8
	Layer2	18	62.5	6
Ladder2	Layer3	37	125	4
	Layer4	39	125	4
Ladder3	Layer5	58	125	4
	Layer6	60	125	4



A ladder module conceptual design

ATLAS/CMS upgrade
(15 μm)

Alice upgrade
(8 ~ 10 μm)

CEPC vertex
(3 ~ 5 μm)

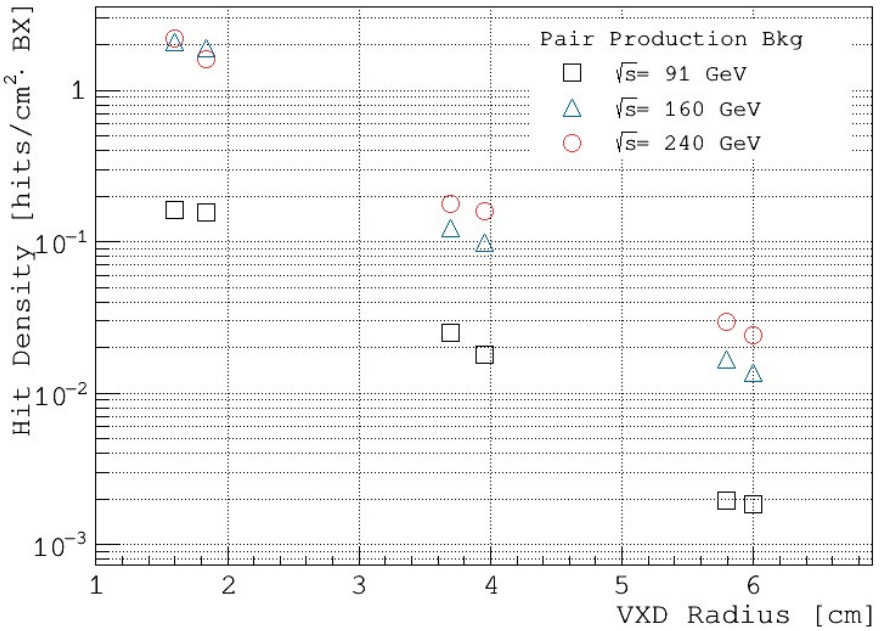
Resolution

Ref: Pixel Vertex Detector Prototype MOST 2018-2023 (MOST2), Joao Costa, 2019.11

Challenges and R&D activities on pixel sensors

- **Bunch spacing**
  - **Higgs: 680ns; W: 210ns; Z: 25ns**
  - **Meaning 40M/s bunches (same as the ATLAS Vertex)**
- **Hit density**
  - **2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z**
- **Cluster size: 3pixels/hit**
  - **Epi- layer thickness：~18μm**
  - **Pixel size：25μm×25μm**
- **Hit rate: 120MHz/chip @W**

From the CDR of CEPC



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- **Two major constraints for the CMOS sensor**
  - **Pixel size: < 25μm* 25μm (σ~5μm)**
    - **aiming for 16μm*16μm (σ~3μm)**
  - **Readout speed: bunch crossing @ 40MHz**
- **None of the existing CMOS sensors can fully satisfy the requirement of high-rate CEPC Vertex Detector**
- **TID is also a constraint**
  - **1~2.5Mrad/year as required in MOST2 is achievable**

	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✔	X	✔
Readout Speed	X	✔	X
TID	X (?)	✔	✔

Main specs of the full size chip for high rate vertex detector

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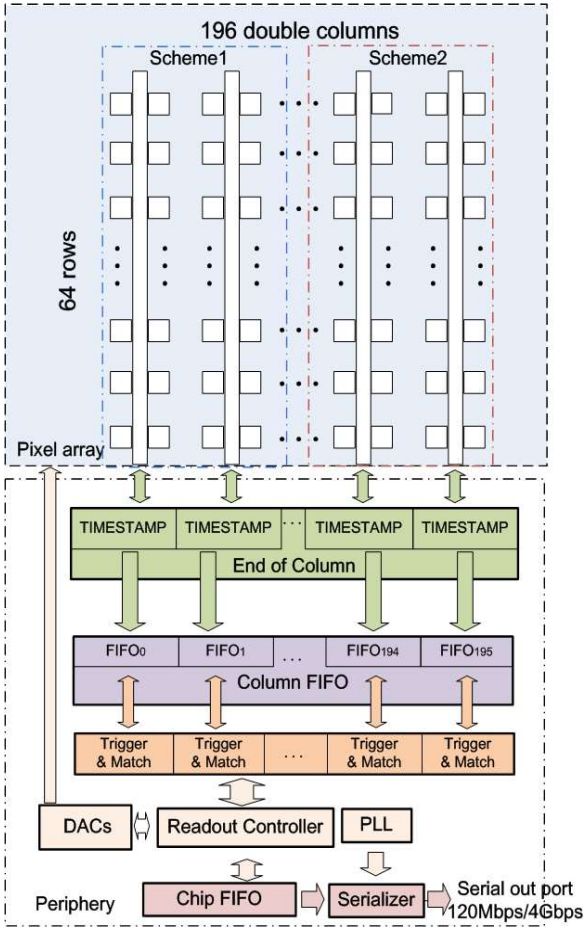
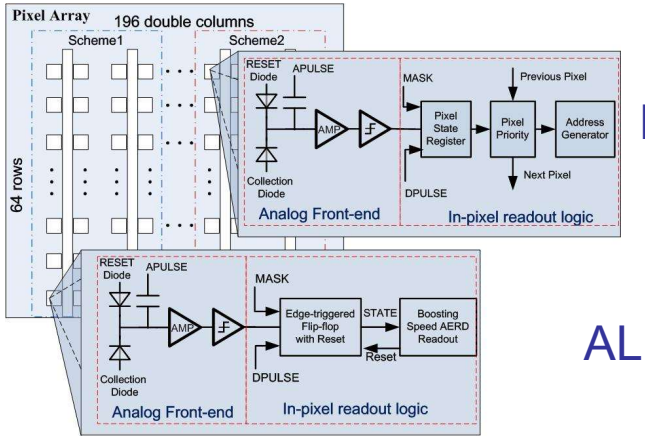
For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row×1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm^2 (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm×2.56cm

New proposed architecture



From Tianya Wu in User Manual

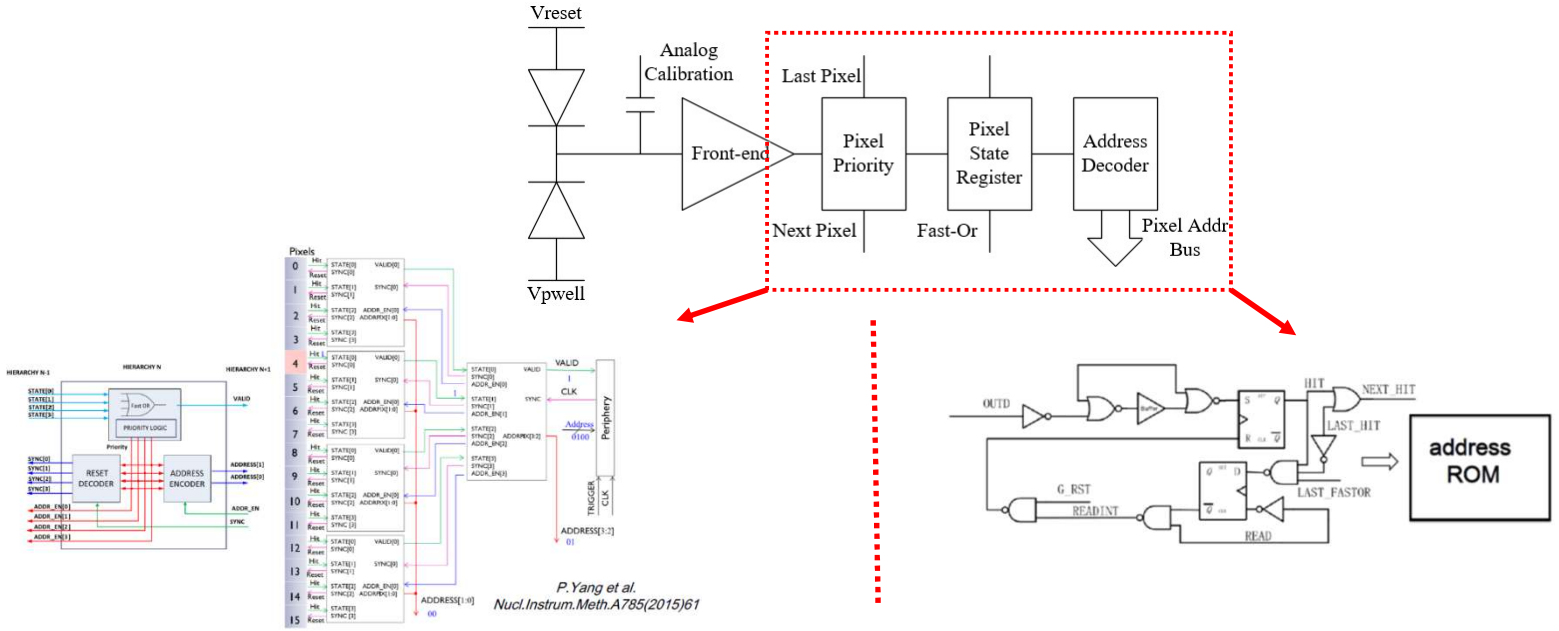


FE-I3-like Pixel

ALPIDE-like Pixel

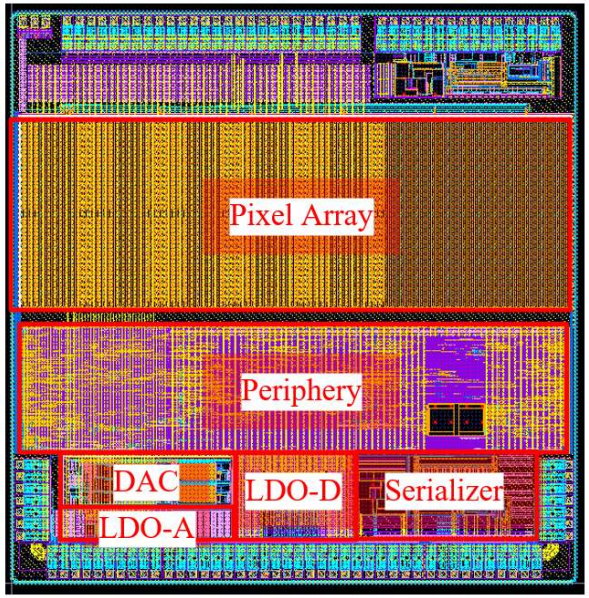
- **Similar to the ATLAS ITK readout architecture: "column-drain" readout**
  - **Priority based data driven readout, zero-suppression intrinsically**
  - **Modification: time stamp is added at EOC whenever a new fast-or busy signal is received**
  - **Dead time: 2 clk for each pixel (50ns @40MHz clk), negligible compared to the average hit rate**
- **2-level FIFO architecture**
  - **L1 FIFO: In column level, to de-randomize the injecting charge**
  - **L2 FIFO: Chip level, to match the in/out data rate between the core and interface**
- **Trigger readout**
  - **Make the data rate in a reasonable range**
  - **Data coincidence by time stamp, only matched event will be readout**

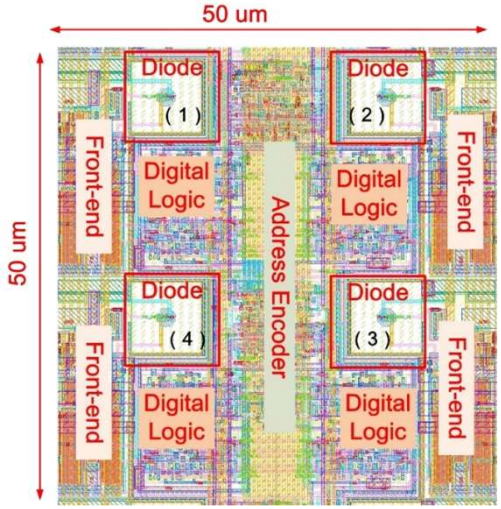
Pixel architecture – parallel digital schemes



- **Simplified column-drain readout:**
  - **Each double column shares a common Fast-Or bus for hit indication**
  - **Common time stamp register @40MHz will record the hit arrival time**
  - **Hit pixels in the same cluster will share a common time stamp as the Trigger ID**
- **Two parallel digital readout architectures were designed:**
  - **Scheme 1：ALPIDE-like: benefit from the proved digital readout in small pixel size**
    - ➢ **Readout speed was enhanced for 40MHz BX**
  - **Scheme 2：FE-I3-like: benefit from the proved fast readout @40MHz BX (ATLAS)**
    - ➢ **Fully customized layout of digital cells and address decoder for smaller area**

Design Status of the TaichuPix Chip

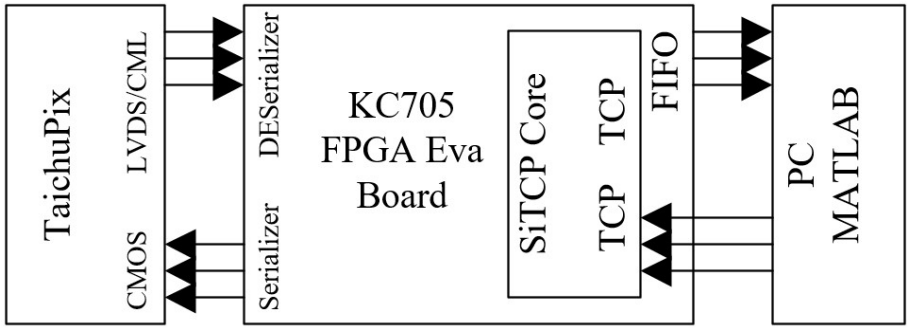


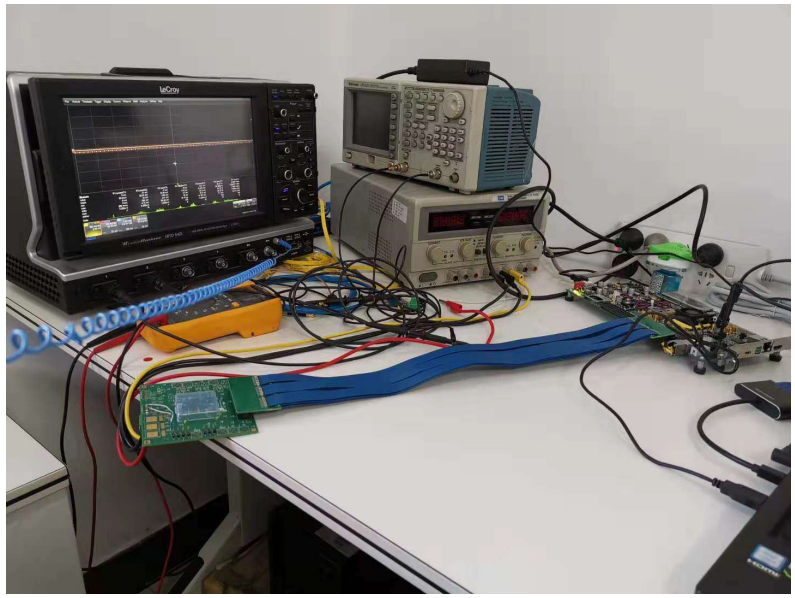


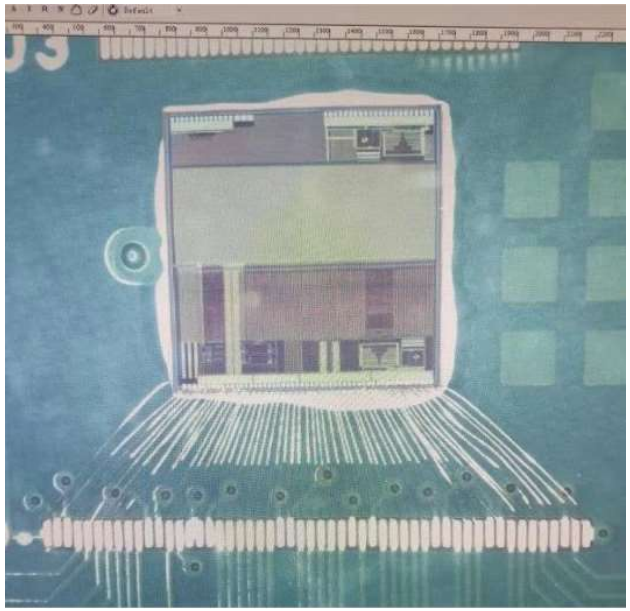
Chip size：5mm×5mm
Pixel size：25μm×25μm

- Two MPW chips were submitted and verified
  - 1st MPW 2019.06~2019.11
  - 2nd MPW 2020.02~2020.06
  - Thanks IFAE for their tunnel for submission to TJ
- Chip size 5mm×5mm with standalone features
  - Pixel size of 25μm×25μm
  - A full functional pixel array (small scale)
    - A 64×192 Pixel array
      - Parallel designs of the pixel cell were verified in sub sectors
  - Periphery logics
    - Fully integrated logics for the data-driven readout
    - Fully digital control of the chip configuration
  - Auxiliary blocks for standalone operation
    - High speed data interface up to 4Gbps
    - On-chip bias generation
    - Power management with LDOs
    - IO placement in the final ladder manner
      - Multiple chip interconnection features included

Test setup for chip evaluation

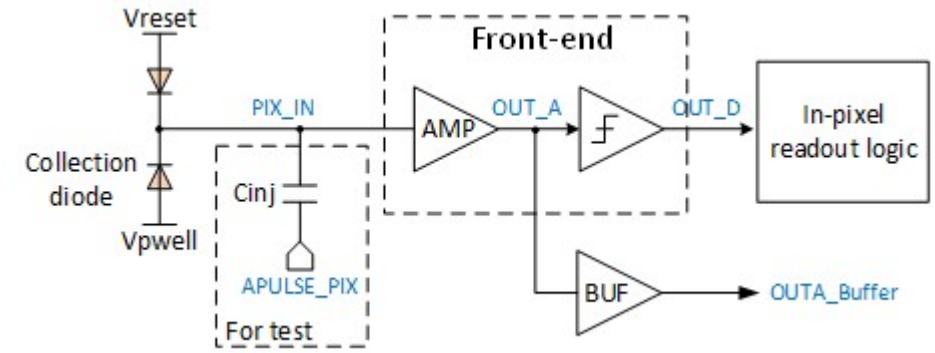


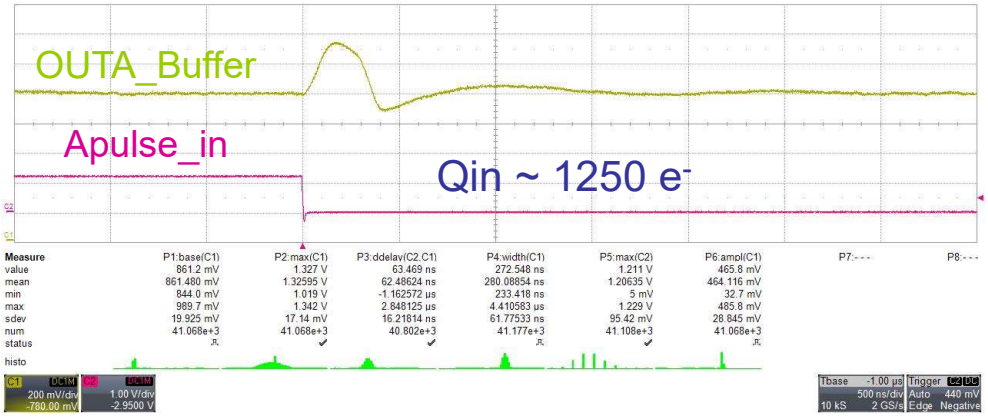




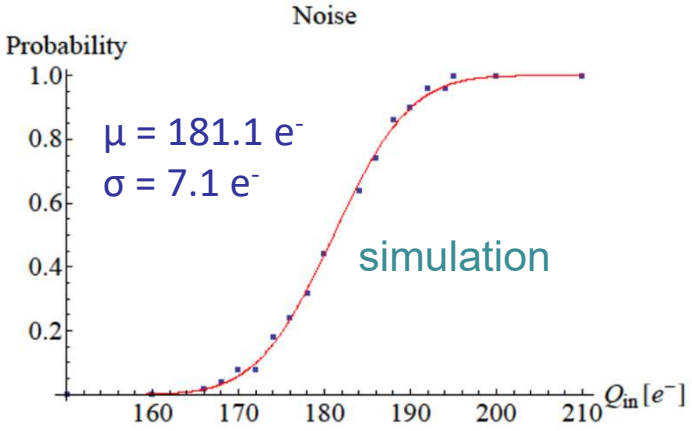
- **Test setup based on KC705 Xilinx FPGA Eva board**
- **General data stream**
  - **Downstream from PC to chip: TCPIP@MATLAB → SPI package@ FPGA → TaichuPix Periphery**
  - **Upstream from chip to PC: TaichuPix Serializer → FIFO@FPGA → TCPIP@MATLAB**

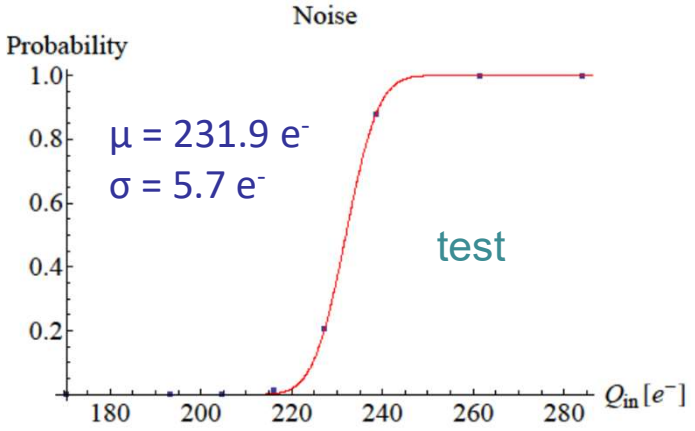
Preliminary test of the pixel analog circuit





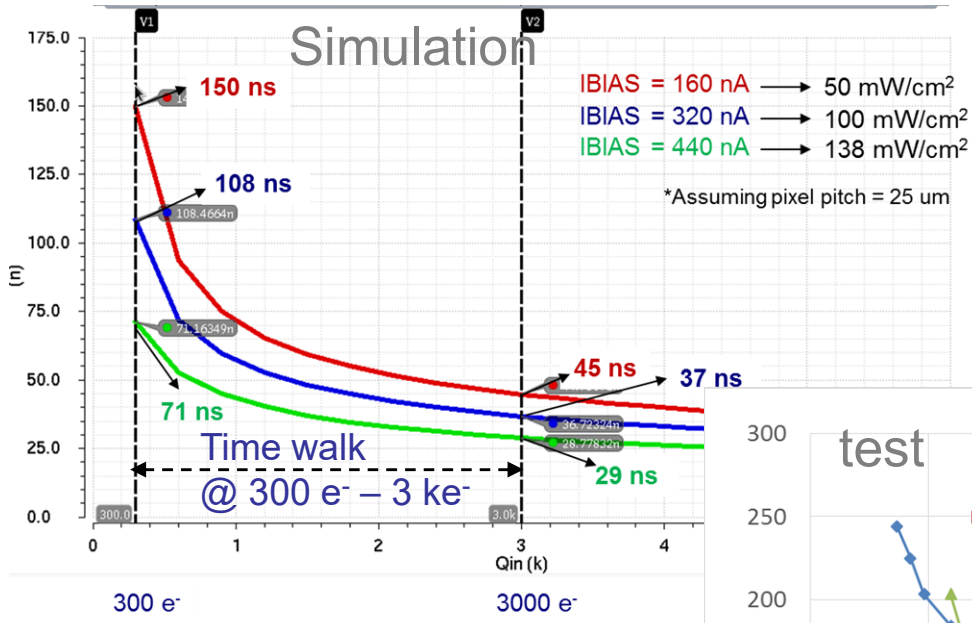
- **Pixel analog circuit was tested by injection pulses**
- **Preliminary test showed the output waveform agreed with simulation**
- **Tested noise about 5.7e$^-$, a little better than simulation results**

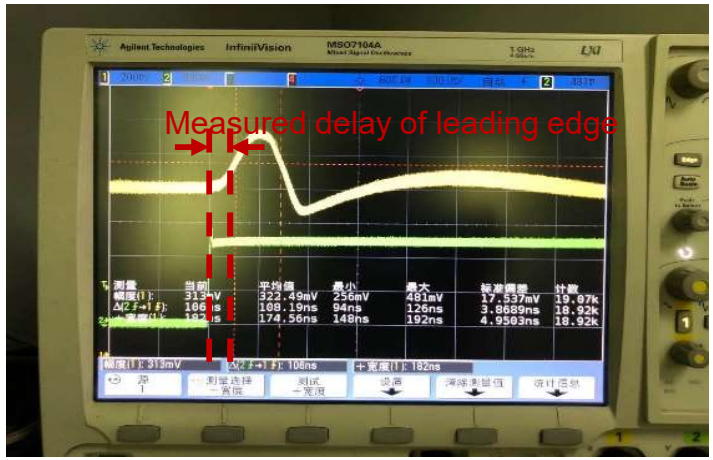




Preliminary test of the timing performance

- **The delay of the analog output will decrease as the input charge increases**

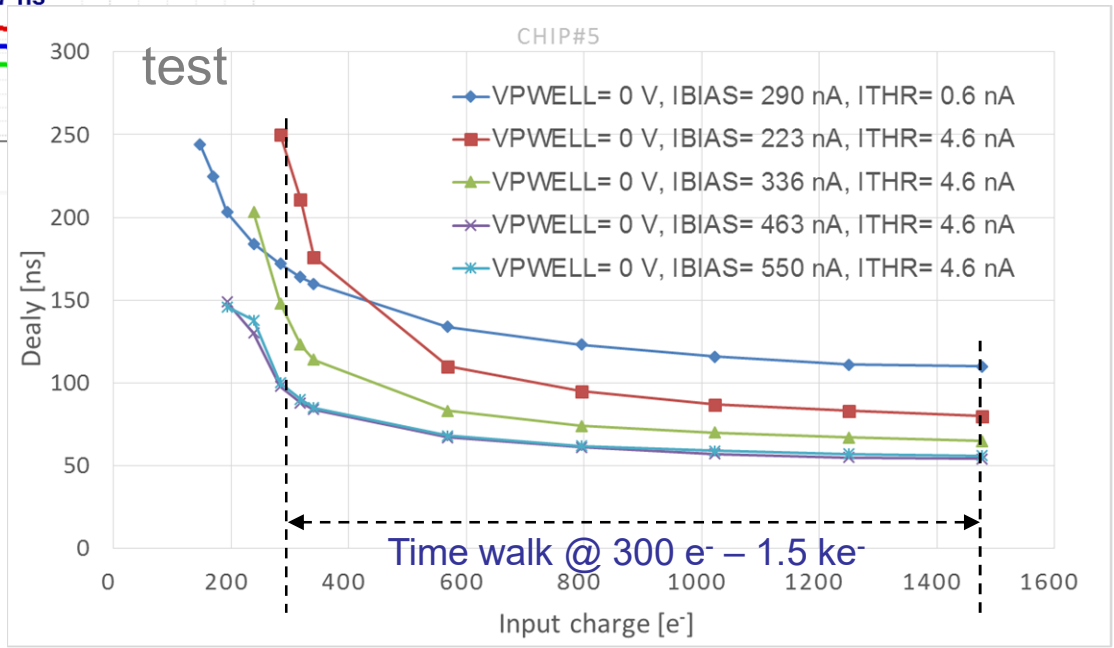




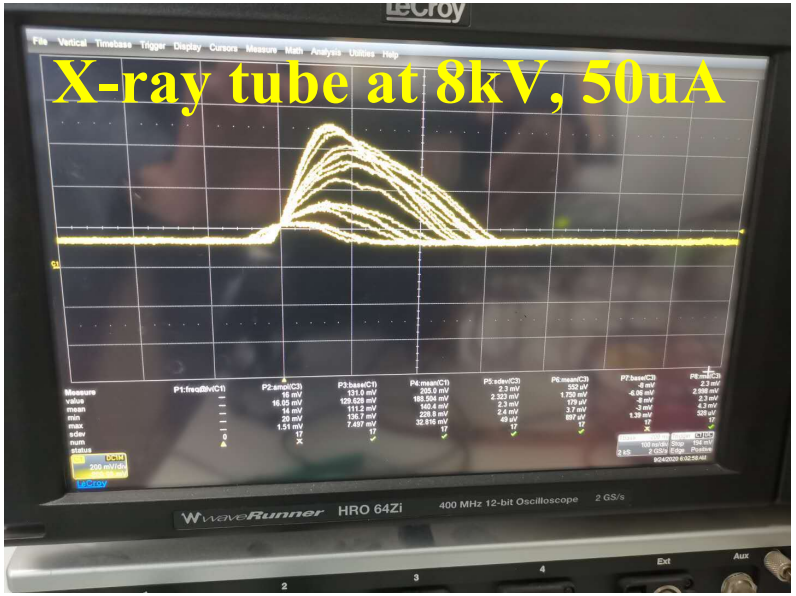
Timing performance agreed with the simulation

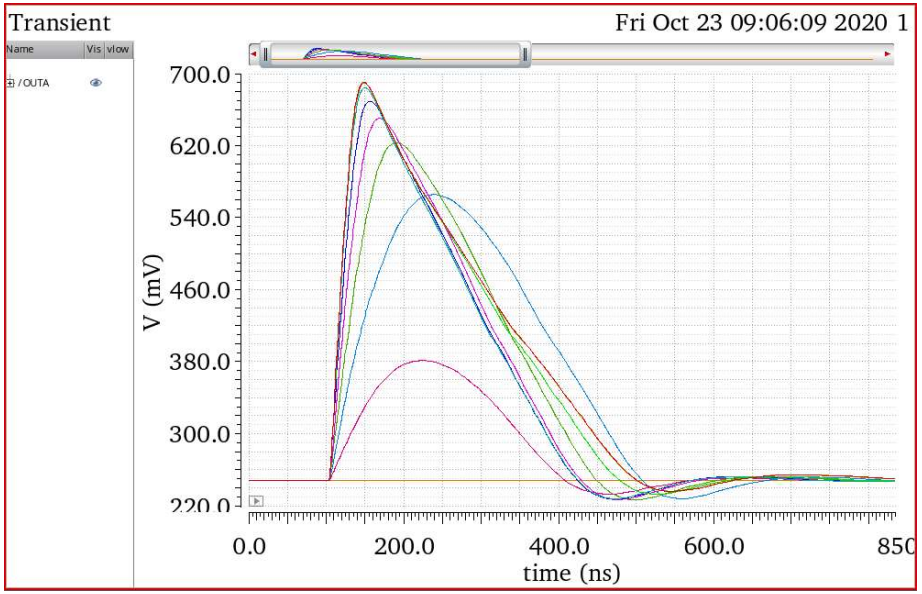
Tested time walk (~36 ns@ 300 e⁻ – 1.5 ke⁻) vs simulation (~33 ns@ 300 e⁻ – 3 ke⁻) @ power ~ ~130 mW/cm²(Design value)

Leading edge delay vs. input charges @ diff. bias



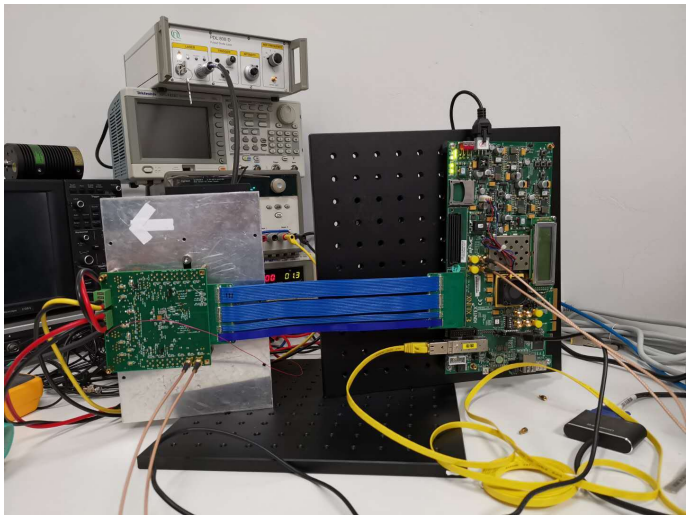
Preliminary verification with radioactive

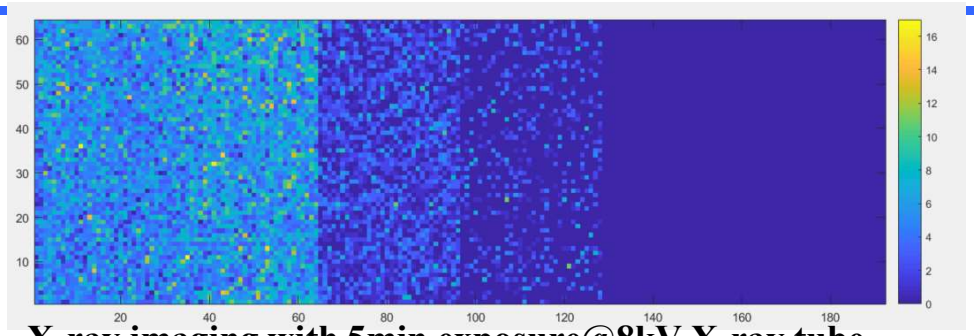




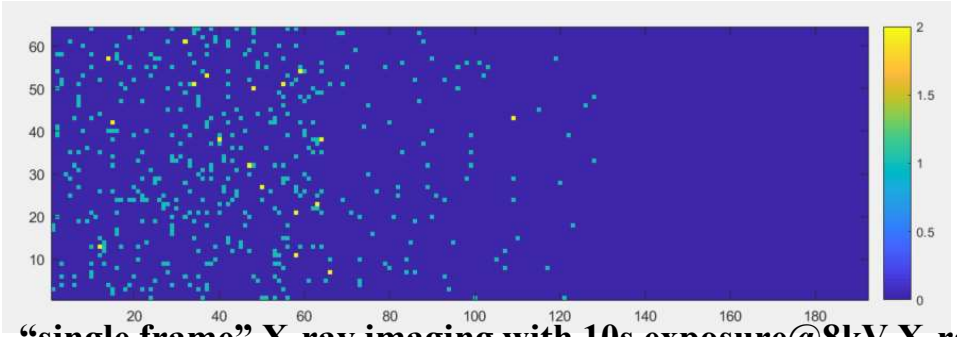
- **Analog output waveform agreed with the simulation when tested by X-rays**
  - **Signal amplitude, signal width, edge speed…all are almost agreed**
  - **Note: for the small signal, the S/N ratio was also good, inferred that the noise performance was also normal(good)**

Preliminary “DAQ” system established for test





X-ray imaging with 5min exposure@8kV X-ray tube



“single frame” X-ray imaging with 10s exposure@8kV X-ray tube

- “DAQ” system established for the test system, with continuous data acquisition
- Triggerless readout @160Mbps LVDS were applied at the current stage
- The full signal chain (pixel analog-digital-periphery-data interface) was proved by both X-ray and laser imaging
  - Full array/sector was sensitive
  - “Single frame” imaging showing no crosstalk detected between clusters (good S/N ratio)
- X-ray imaging with 5min exposure showed clearly the different sectors of the pixel array (2 sectors were masked)

Summary and plan

- **Two MPWs of TaichuPix were designed with all features integrated for standalone operation**
- **Major functionality and the full signal chain verified by radioactive source**
- **Laser test, beam test, and TID test were under consideration for more calibrated verification**
- **Thinking about a full size tapeout for the next**

Thank you !

Team organization

- Slides from Y. Zhang, Satellite meeting of MOST2 in Oxford, 2019.4

- **Design team:**
  - **IHEP, SDU, NWPU, IFAE & CCNU**
  - **Biweekly/weekly video design meeting on chip design (convened by IHEP)**

Institutes	Tasks	Designers
IHEP	Full chip modeling & simulation Pixel Analog, TCAD simulation High speed interface: PLL + Serializer	Wei Wei, Ying Zhang Xiaoting Li, Weiguo Lu, Mei Zhao
CCNU/IFAE	Pixel Digital	Tianya Wu, Raimon Casanova
NWPU	Periphery Logic, LDO	Xiaomin Wei, Jia Wang
SDU	Bias generation	Liang Zhang

- **Chip characterization**
  - **Test system development: SDU & + other interested parties**
  - **Electrical test: all designers supposed to be involved in the related module + other interested parties**
  - **Irradiation test: X-ray irradiator + beam line**