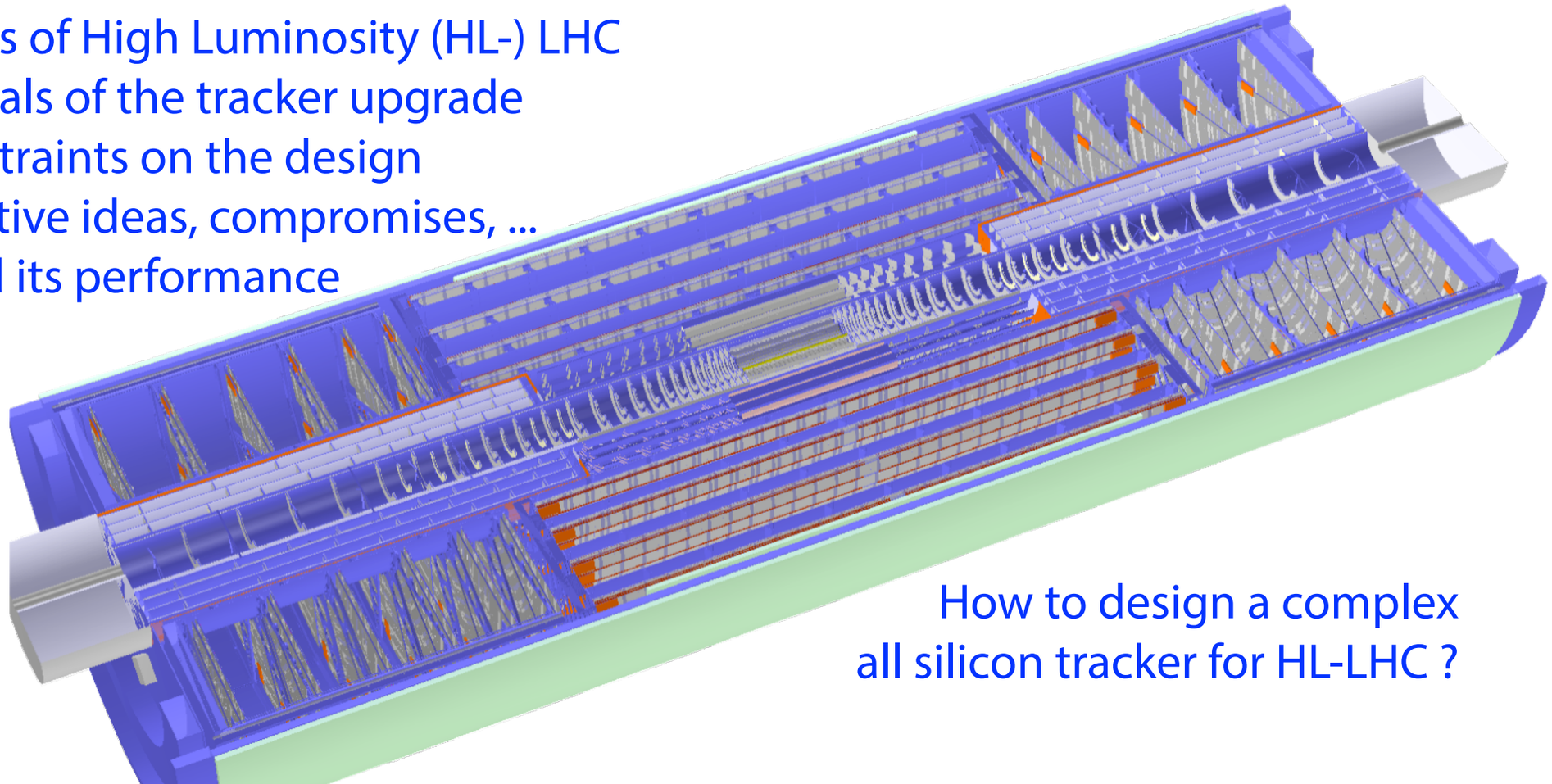
Lessons learned from the ATLAS Upgrade Tracker Design

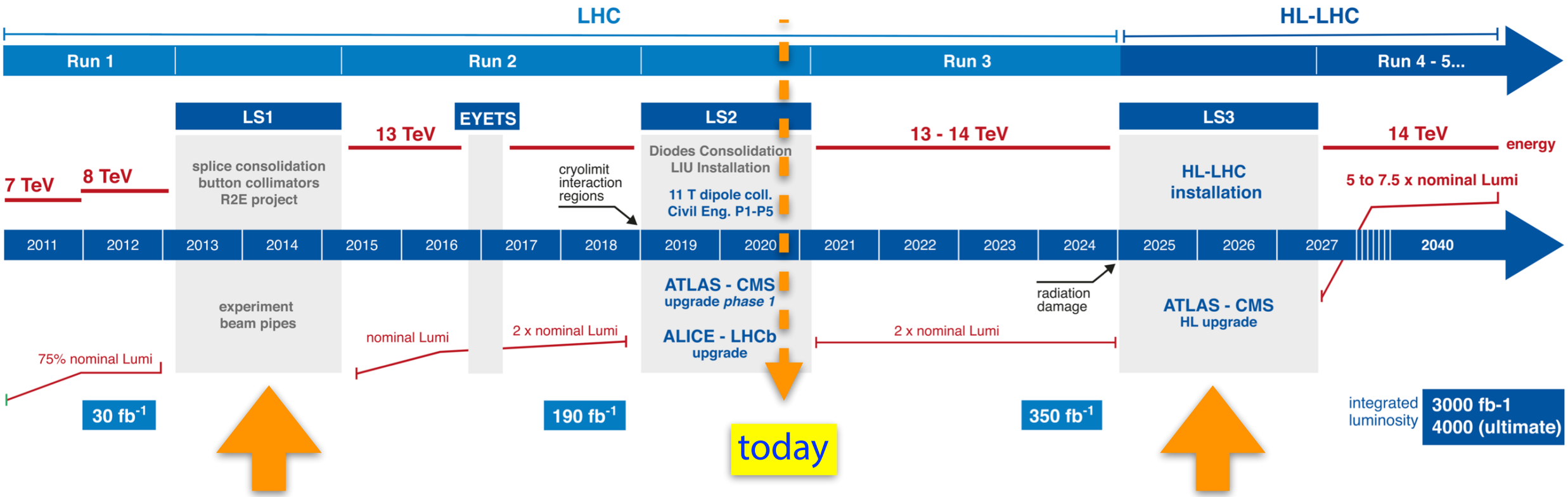
by Markus Elsing

- ➡ tracking challenges of High Luminosity (HL-) LHC
- ➡ motivation and goals of the tracker upgrade
- ➡ methods and constraints on the design
  - including innovative ideas, compromises, ...
- ➡ final ITk layout and its performance



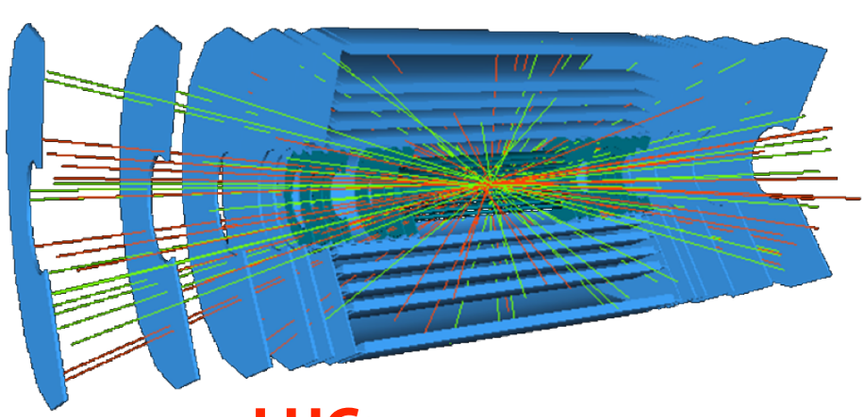
How to design a complex
all silicon tracker for HL-LHC ?

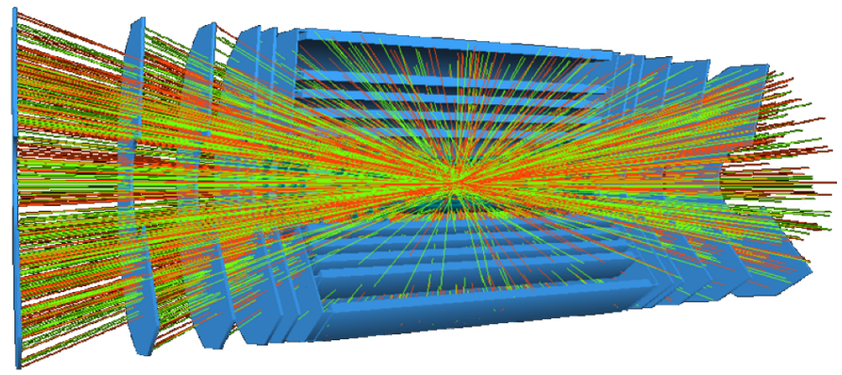
LHC Schedule and Parameters



Inner Detector: Pixel + SCT + TRT
"Phase-0" upgrade with IBL

"Phase-2" upgrade: full replacement
Inner Tracker (**ITk**) with Pixel + Strip



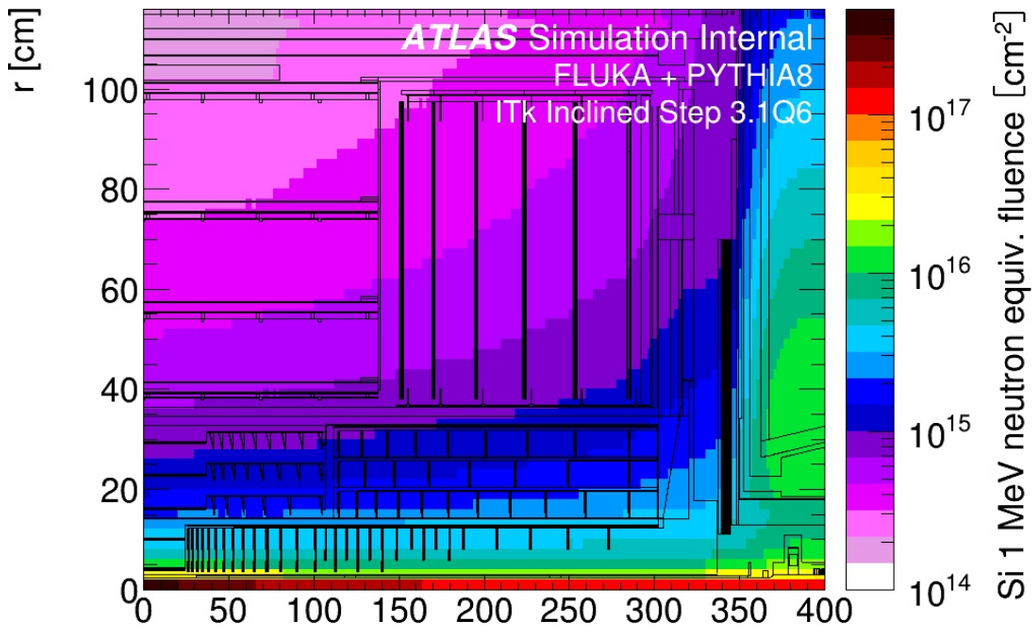


LHC:
pile-up of **19 - 55**

High Luminosity (LH) LHC:
pile-up of **140 - 200**

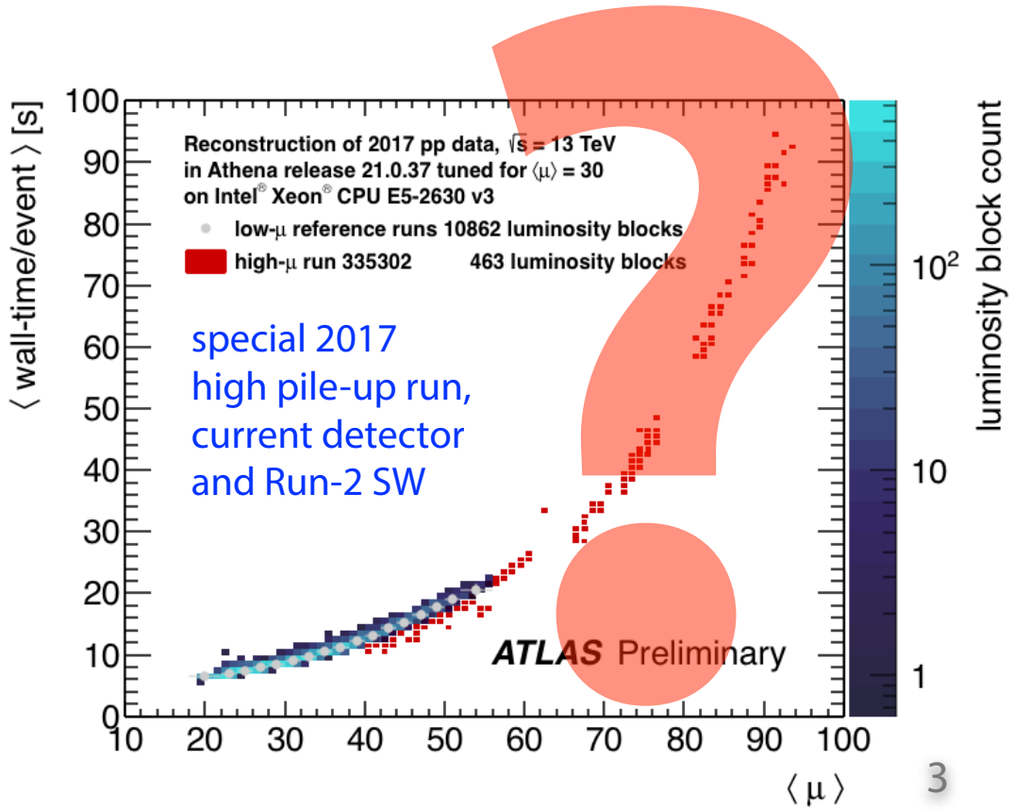
Goals of the Tracker Upgrade

- HL-LHC is a challenge !
  - ➡ peak luminosity: 5-7x10^{34} $cm^{-2}s^{-1}$ (**x5-7**)
  - ➡ average **pile-up**: up to ~200 (**x5**)
  - ➡ integrated luminosity: 4000 fb^{-1} (**x10**)
  - ➡ radiation hardness: up to 2x10^{16} neq/cm^2 (**x20**)
  - ➡ higher hit and trigger rates
  - ➡ requires all silicon tracker (with **Pixels** and **Strips**)



- physics goals are ambitious !
  - ➡ require same or better detector performance, despite harsh environment
    - keep excellent **b-jet tagging** and lepton tracking
    - **pile-up rejection** for jets and missing E_T
  - ➡ processes like Vector Boson Fusion (VBF) Higgs production call for an **extended η coverage (< 4)** (forward jet signature, current ID covers $|\eta| < 2.5$)

- tracking CPU additional requirement
  - ➡ event complexity may lead to huge CPU increase for **offline** and High Level Trigger (**HLT**) reconstruction

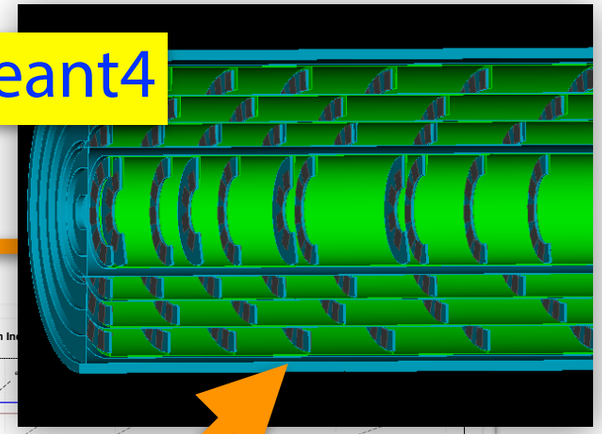


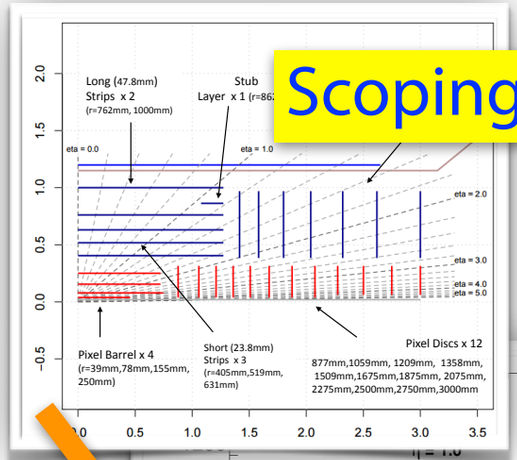
Layout Optimisation Strategy

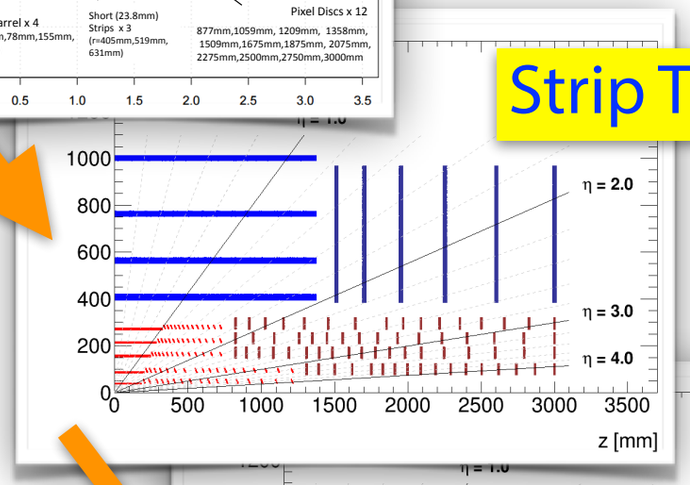
- optimisation is an iterative procedure
  - ➡ design tool **IdRes** allows for fast layout optimisation
    - hit coverage, resolutions, ...
  - ➡ **Geant4** to assess full layout performance
    - 3D hermeticity, tracking, CPU, ...
  - ➡ **simulation** studies support **engineering** work
    - supports, services, materials, clearances, ...

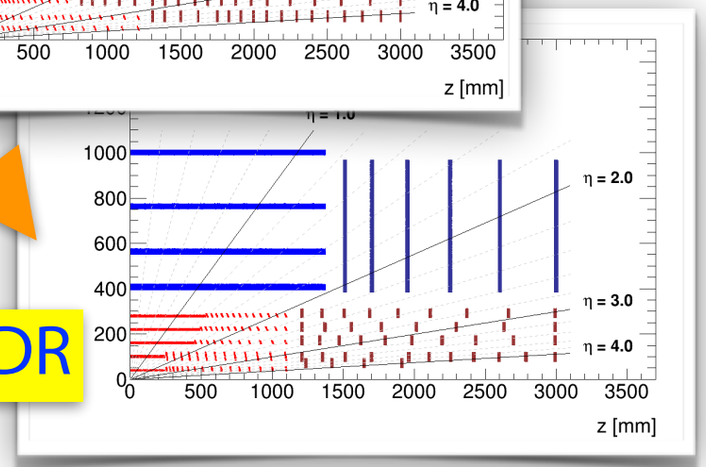
- a whole series of **layout evolutions**
  - ➡ **Strip TDR** layout evolved from **Scoping Document**
  - ➡ **Pixel TDR** layout basis for fully engineered final Pixel design one year later (**final ITk** layout)

- metric used for layout optimisation:
  - balance ambitions with **constructibility**
  - **performance** required for Phase-2 physics program
  - tracking **robustness** against detector failures
  - minimise **cost** (silicon surface, complexity, ...)
  - minimise **CPU** for reconstruction (computing cost)



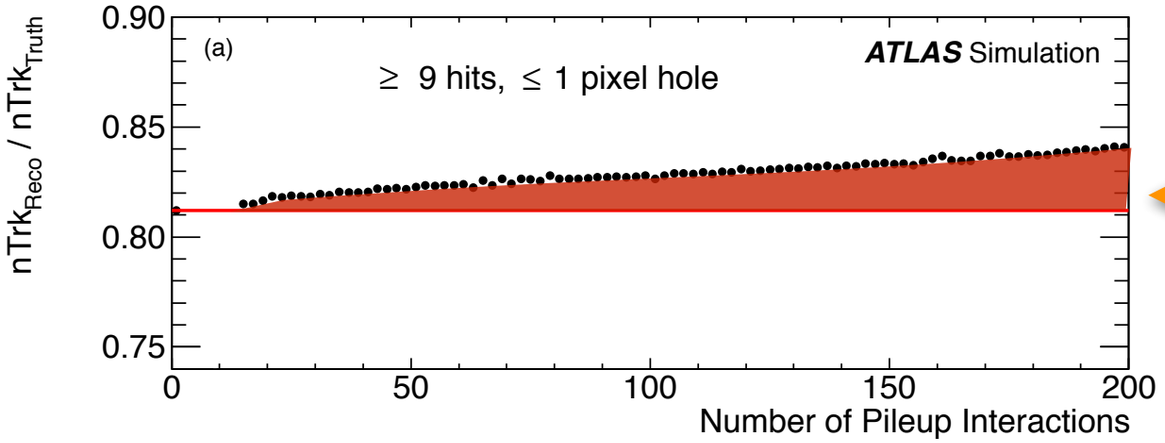




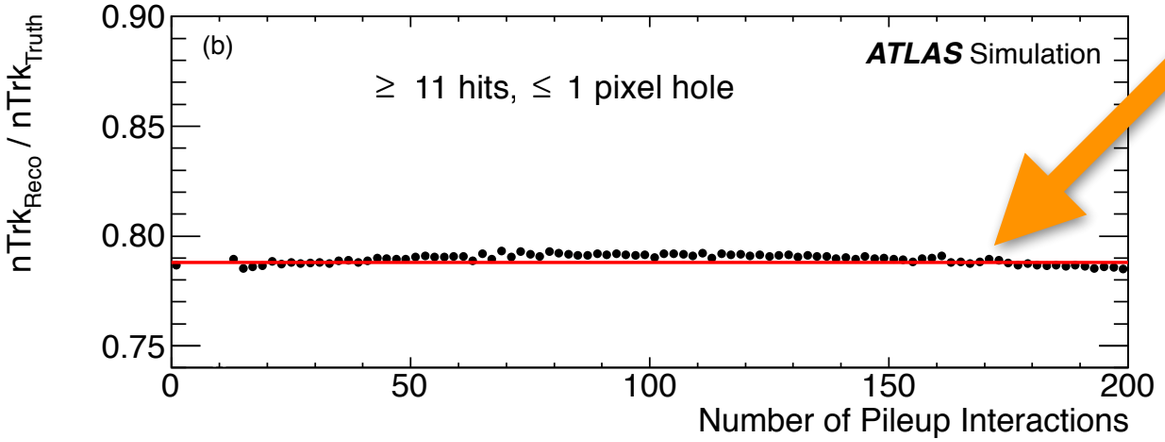


Hit Requirement for Robust Tracking ?

- experience from tracking at Run-1 and Run-2 pile-up levels
  - ➡ effective cuts to reduce fakes and limit CPU for high pile-up:
    increase cuts on **number of hits** and cuts on **holes** (sensors without hit found)



- increasing hits cut from ≥7 to ≥9
  - ➡ still additional component due to fakes and more bad tracks from hadronic interactions



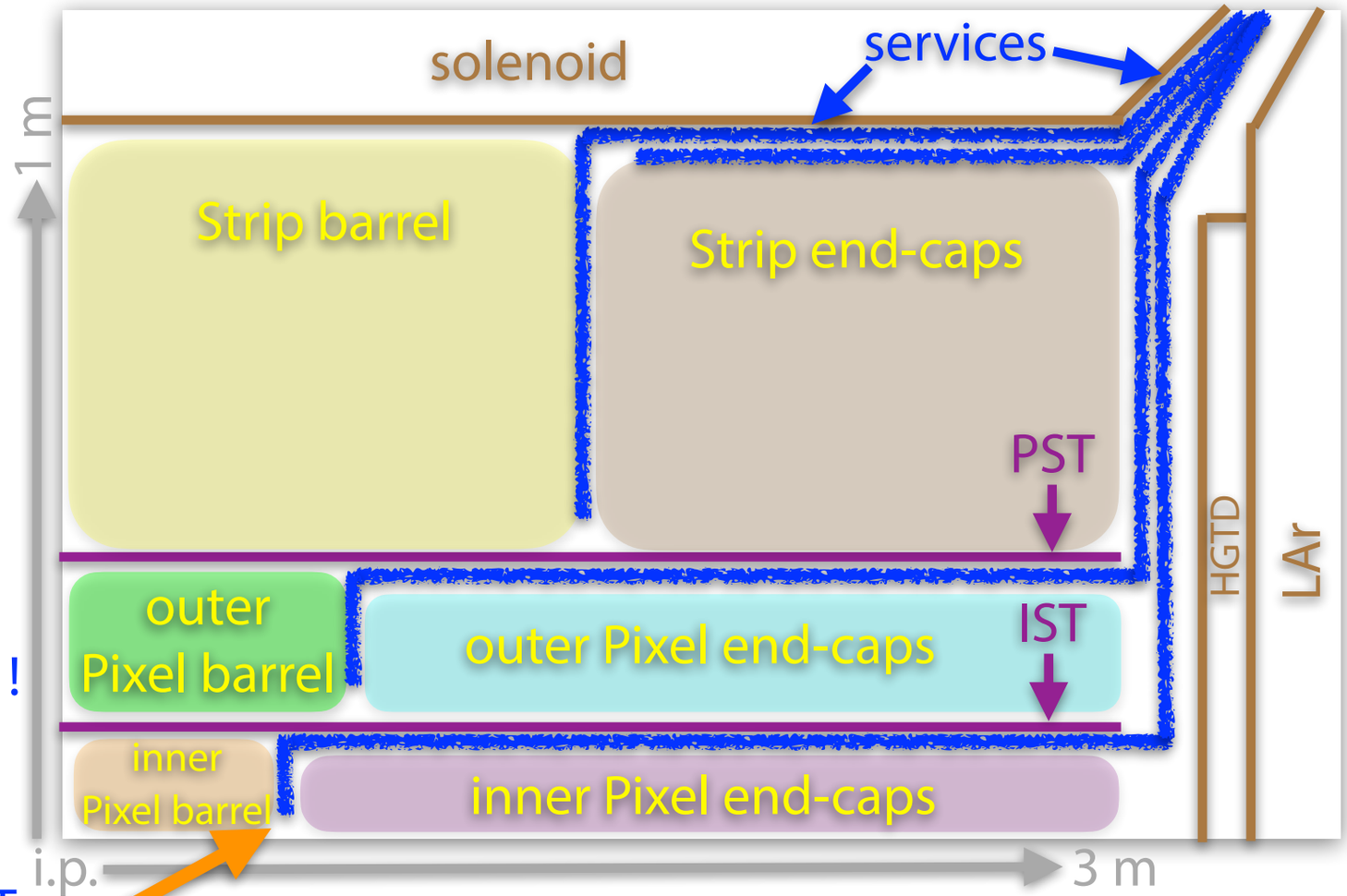
- increasing cut to ≥11 hits
  - ➡ fake component suppressed successfully
- adding 1 hit for **redundancy** ?!
  - ➡ $\varepsilon_{track} = (\varepsilon_{hit})^{12} + 11 \cdot (1-\varepsilon_{hit}) \cdot (\varepsilon_{hit})^{11}$
    $= \quad 69\% + 26\% = 95\%$ for $\varepsilon_{hit} = 97\%$

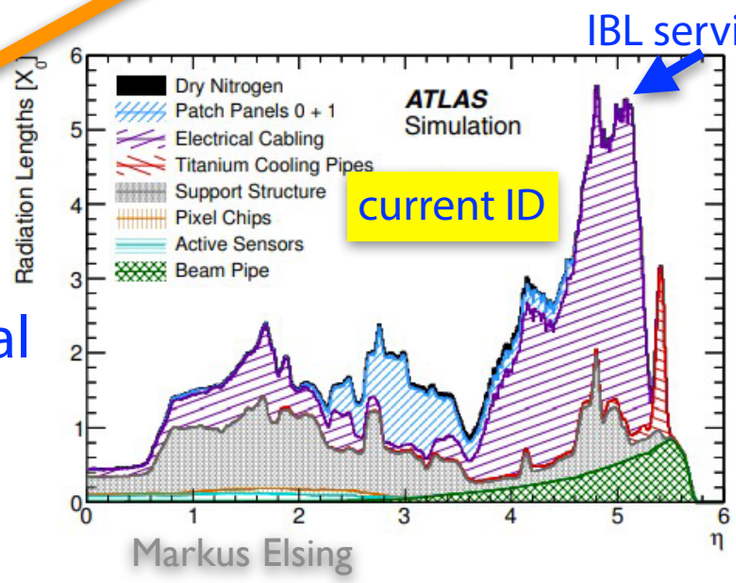
- need to allow for detector **defects** (robustness)
  - ➡ **13 hits** as the minimal requirement for the ITk, with the final detector granularity

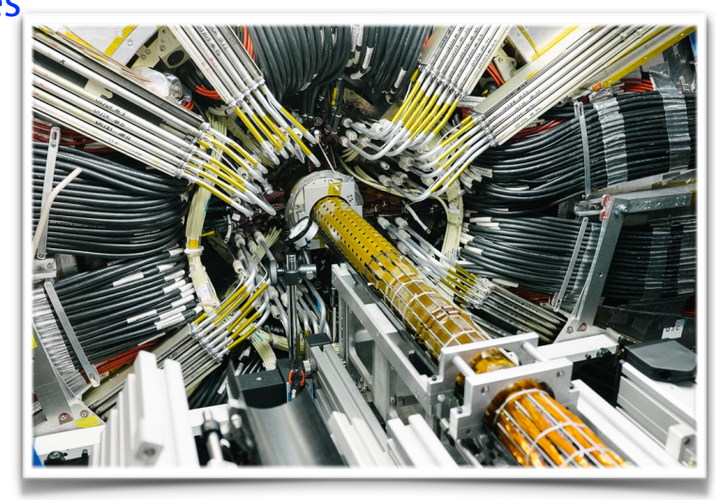
Construct a HL-LHC Tracker covering |η|<4 ?

- design constraints
  - ➡ separate **Strip** and **Pixel** volumes for construction and integration
    - Pixel Support Tube (**PST**)
  - ➡ harsh **radiation** environment
    - inner 2 Pixel layers replaced once to reach 4000 fb^{-1}
    - Inner Support Tube (**IST**)
  - ➡ HL-LHC pile-up and data rates
    - more channels, cooling, **services** !

- service routing + material
  - ➡ **services** need to run inside IST/PST
    - see effect of IBL services inside IST for current ID
  - ➡ barrel/end-cap **transition gaps** ?
    - barrel services and supports
    - **coverage gaps** with lots material and risk to line-up in η



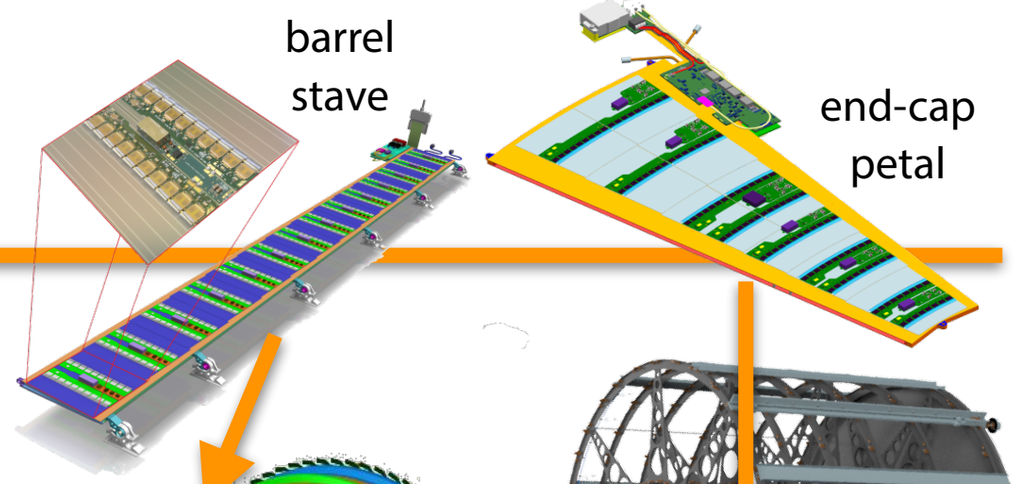


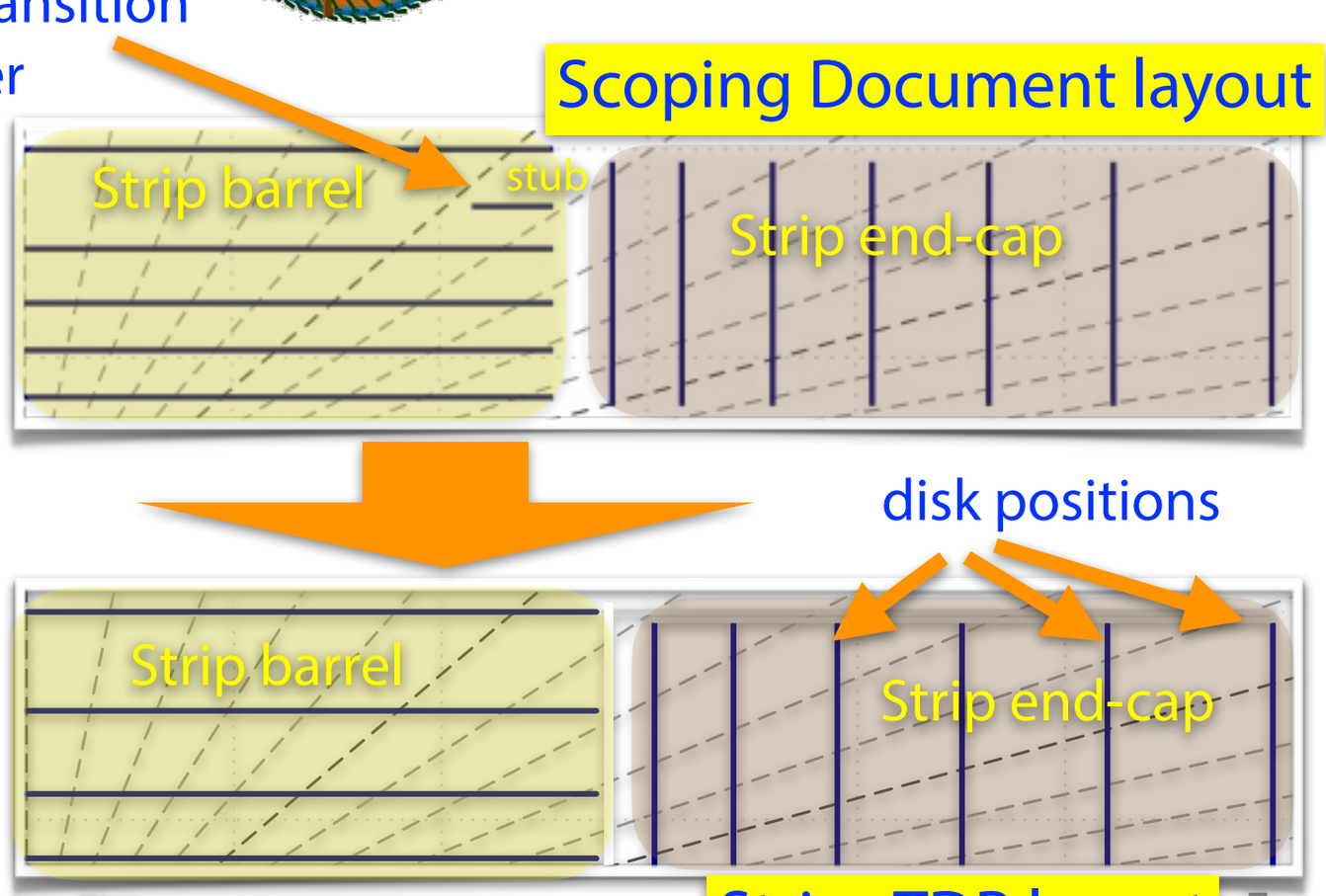


IBL insertion into IST

Strip Detector Layout

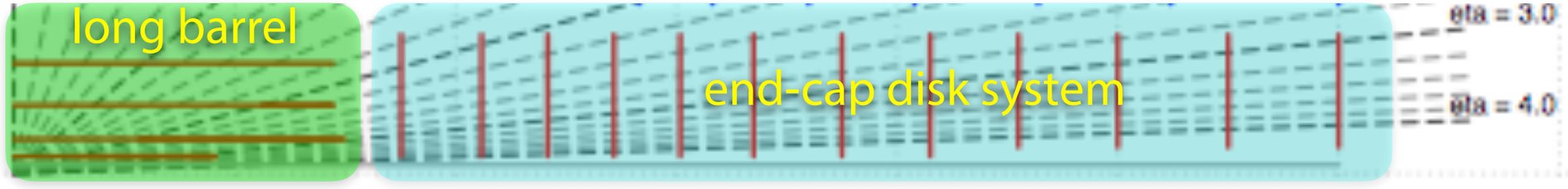
- **classical** detector design
  - ➡ barrel **layers** with **double-sided staves**
  - ➡ end-cap **disks** constructed with **double-sided petals**
  - ➡ small angle stereo to measure z(R)
  - ➡ more than **160 m²** of silicon !
- initial design:
  - ➡ 5 barrel layers and 7 end-cap disks
  - ➡ "**stub layer**" to cover barrel/end-cap transition
    - alternative to lower radius of full outer layer would reduce resolution in p_T
- final design optimisation:
  - ➡ go to 4 barrel Strip layers, in favour of 5th Pixel layer (granularity)
  - ➡ drop mechanically complex "stub layer" (accept gap)
  - ➡ **lengthen barrel** by 1 module
    - shift gap to larger η (more favourable)
    - remove 1 end-cap disk
    - re-optimise **disk position** (p_T resolution)





Innovative Pixel Support Technologies

- classical "Scoping Document" Pixel layout had problems



➡ massive **end-cap disk** system to go to **|η| ~ 4.0** not feasible for construction
  - and does not allow for 2 insertable inner layers (no IST) !

➡ **long barrel** layers would require significant amount of silicon surface

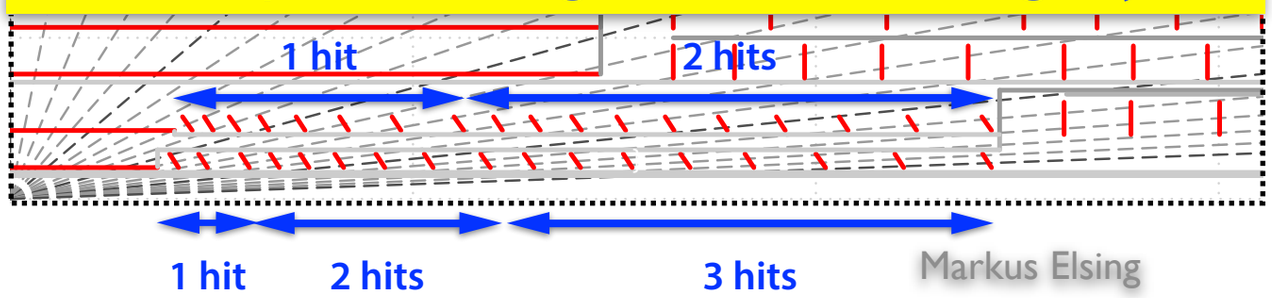
- innovative stave technologies to reduce silicon surface

➡ **inclined modules** at ends of barrel staves requires >30% less silicon (T.Todorov et.al)
  - shift **transition gap** to end of inclined section, inclining modules **reduces material**

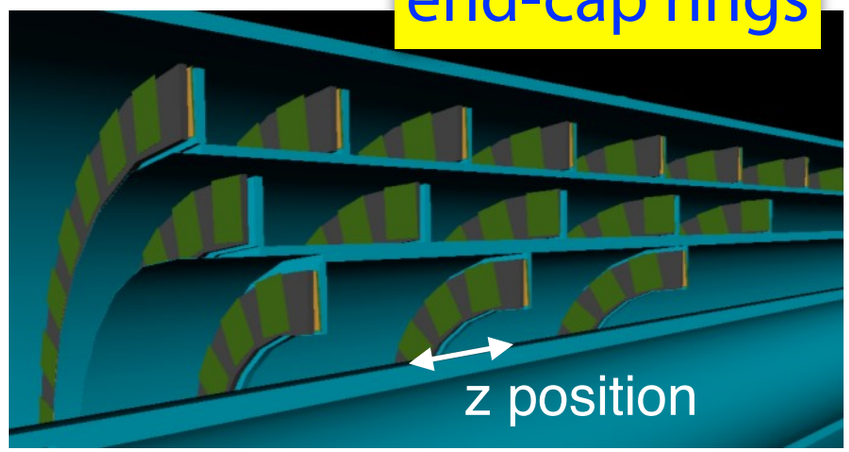
➡ end-cap disks replaced by **ring layers**, each ring positioned to optimise coverage
  - doubling the number of rings in a layer **adds a hit** where needed !

➡ less **material**, flatten hit **coverage** vs η, better IP **resolution** in forward region and reduce **CPU** avoiding large distances between modules

flexible positioning of N hits in ring layers

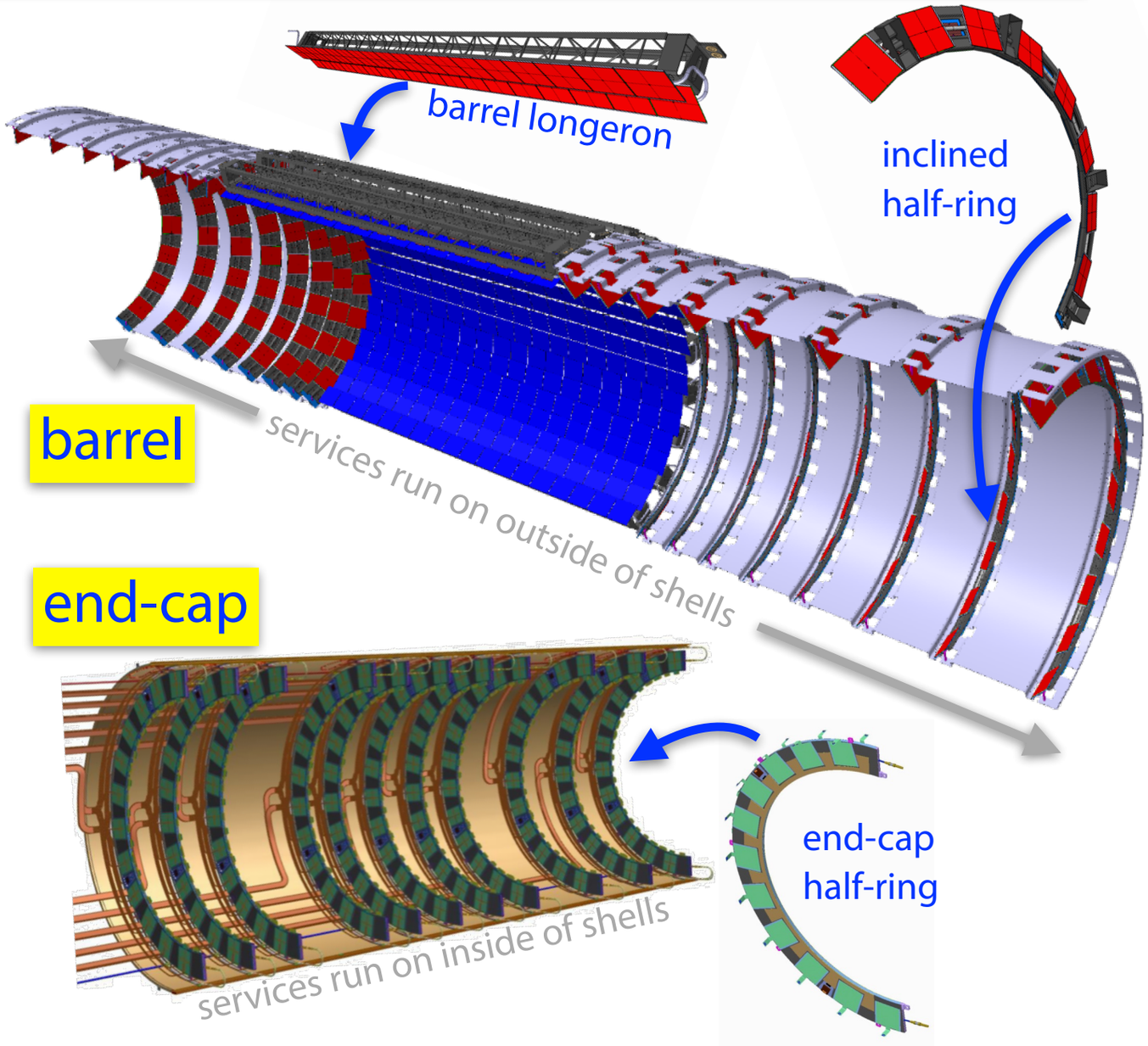


end-cap rings

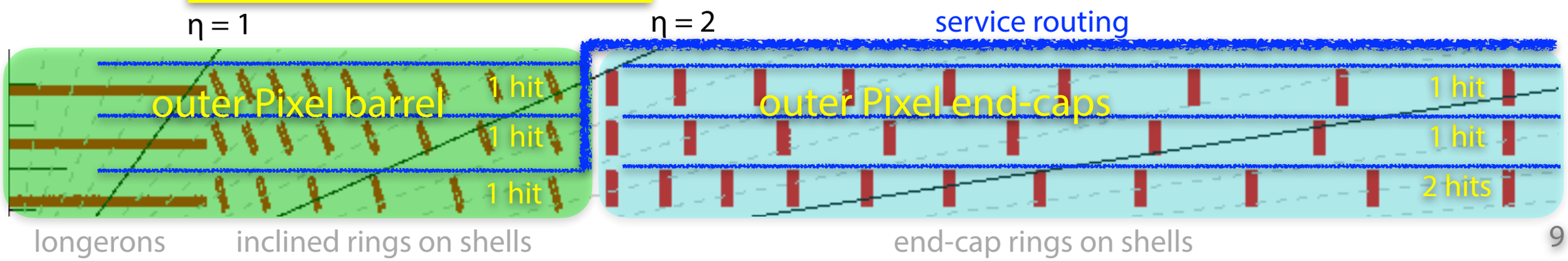


Outer Pixel Barrel and End-Cap Design

- outer Pixel barrel design
  - ➡ **longerons** with 2 "staves" each and **shell** supports for **inclined rings**
  - ➡ inclining modules **reduces material**
  - ➡ services run along outside of shells
  - ➡ shifts barrel/end-cap **gap to η = 2** (instead of η = 1)
- outer Pixel end-caps
  - ➡ 3 **shell layers** with rings
- it coverage per layer ?
  - ➡ **1 hit** in all barrel and end-cap layers, but for innermost end-cap layer (**2 hits**)

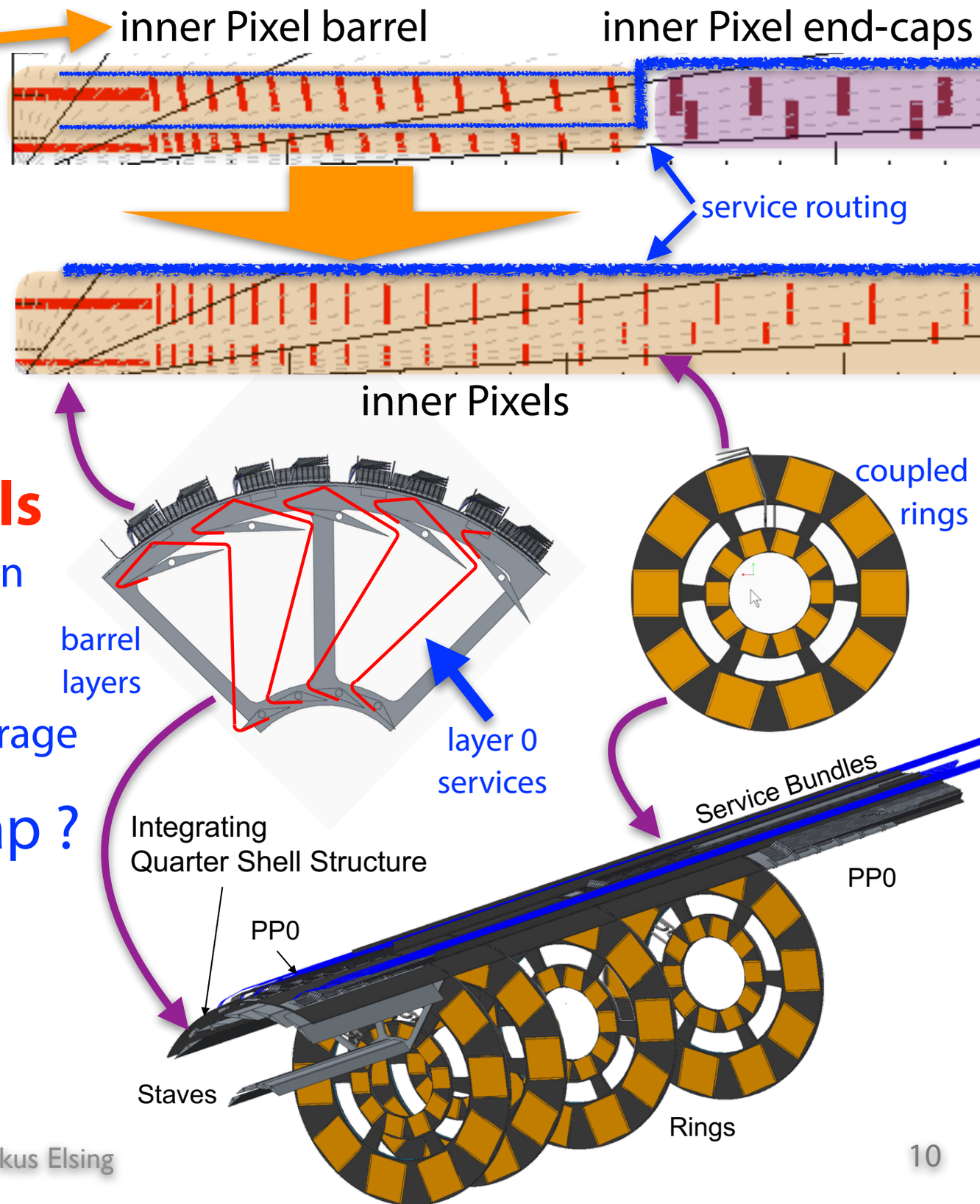


final outer Pixel layout

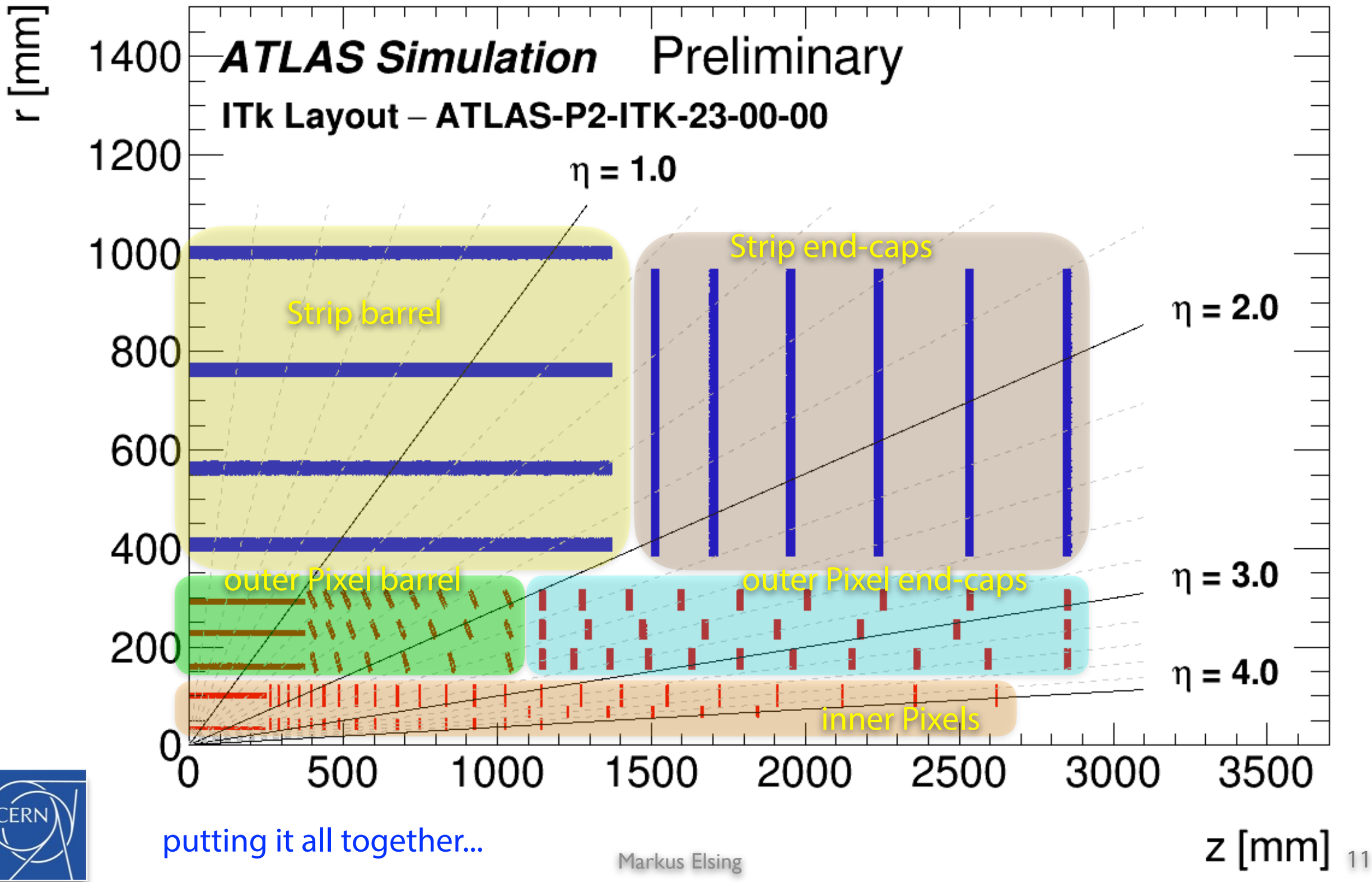


Inner Pixel System Layout

- **Pixel TDR** layout of inner barrel replicated outer Pixels
  - ➡ **2 shells** with flat and inclined sensors
  - ➡ inclined sensor positions optimised for for **hit coverage** vs η and to reduce **CPU**
  - ➡ <u>but:</u> positions of layer 0 and layer 1 rings **almost identical**
- **coupled rings** on **quarter shells**
  - ➡ opportunity to **simplify** mechanical design
  - ➡ extend in the forward with **single rings**
  - ➡ classical **staves** for flat barrel section
  - ➡ same **multiple hits** per ring layer for coverage
- how to avoid barrel/end-cap gap ?
  - ➡ novel routing of layer-0 barrel services **radially** out in between layer-1 modules
  - ➡ all services now run outside of shell



The ATLAS Phase-2 Tracker (ITk) Layout

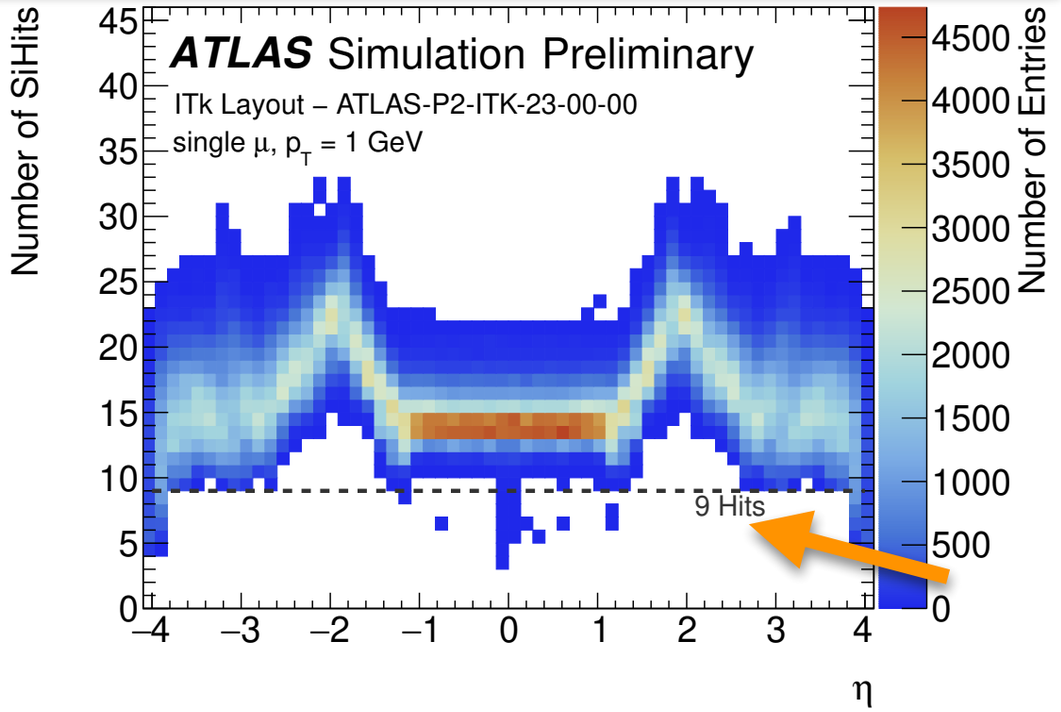


putting it all together...

Hit Coverage and required Silicon Surface

- ITK has minimum 13 hits in barrel, 9 hits in the forward

- compared to Scoping Document
  - ➡ reduce Strip surface by **-15%**
    - dropped 1 barrel layer, 1 disk and barrel stub
  - ➡ reduced Pixel surface by **-11%**
    - for a **5 layer** Pixel system instead of 4 layers (!)
    - improved hit coverage thanks to innovative **local support** designs (!)

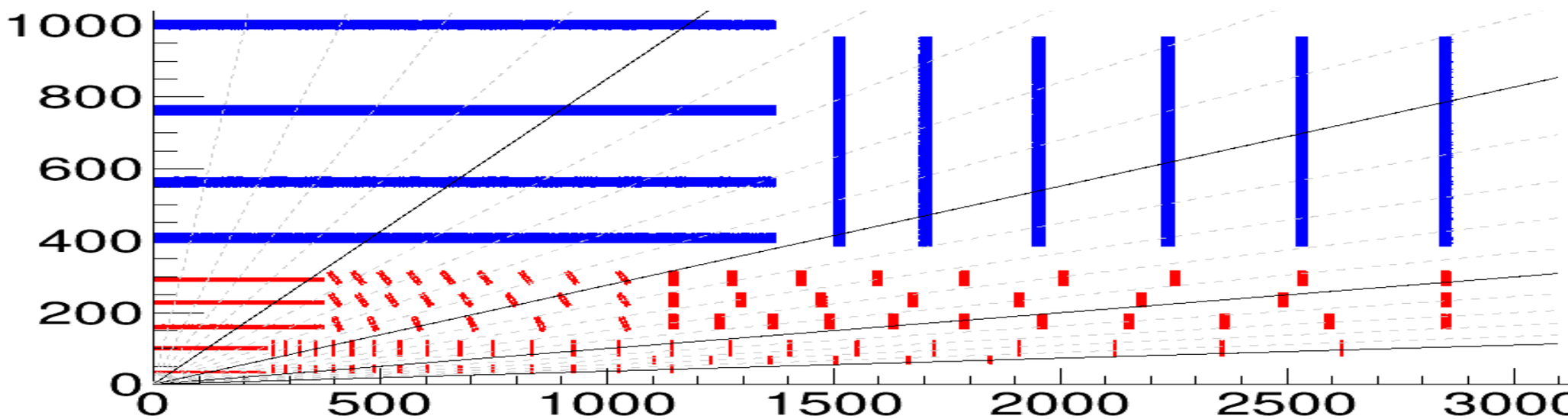


			LoI	Scoping Document	Strip TDR	Pixel TDR	Final
Strips	Barrel	Layers	5.1		4		
		Surfac	122 m²		105 m²		
	End-Cap	Disk	7		6		
		Surfac	71 m²		60 m²		
	Total Surface		193 m²		165 m²		
Pixel	Barrel	Layers	4		5		
		Surfac	5.1 m²		6.4 m²	8.3 m²	7.4 m²
	End-Cap	Disks	6	12	5 ring layers		
		Surfac	3.1 m²	9.2 m²	7.6 m²	4.4 m²	5.4 m²
	Total Surface		8.2 m²	14.3 m²	14.0 m²	12.7 m²	12.8 m²
η coverage			2.7	4.0			

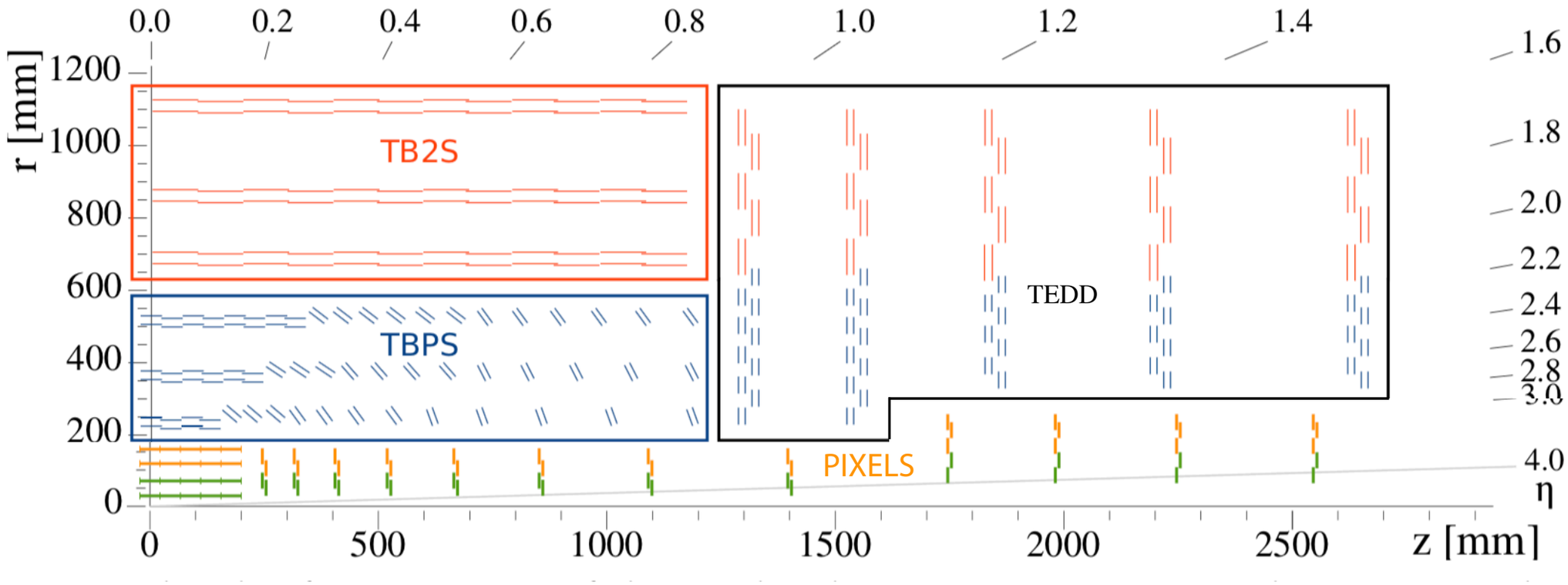
Comparison to CMS Phase-2 Tracker

- tried scaling layout plots to match dimensions...

➡ ATLAS:
- 4 double-strip
- 5 pixel layers
- total **9 layers**
- total **13 hits**

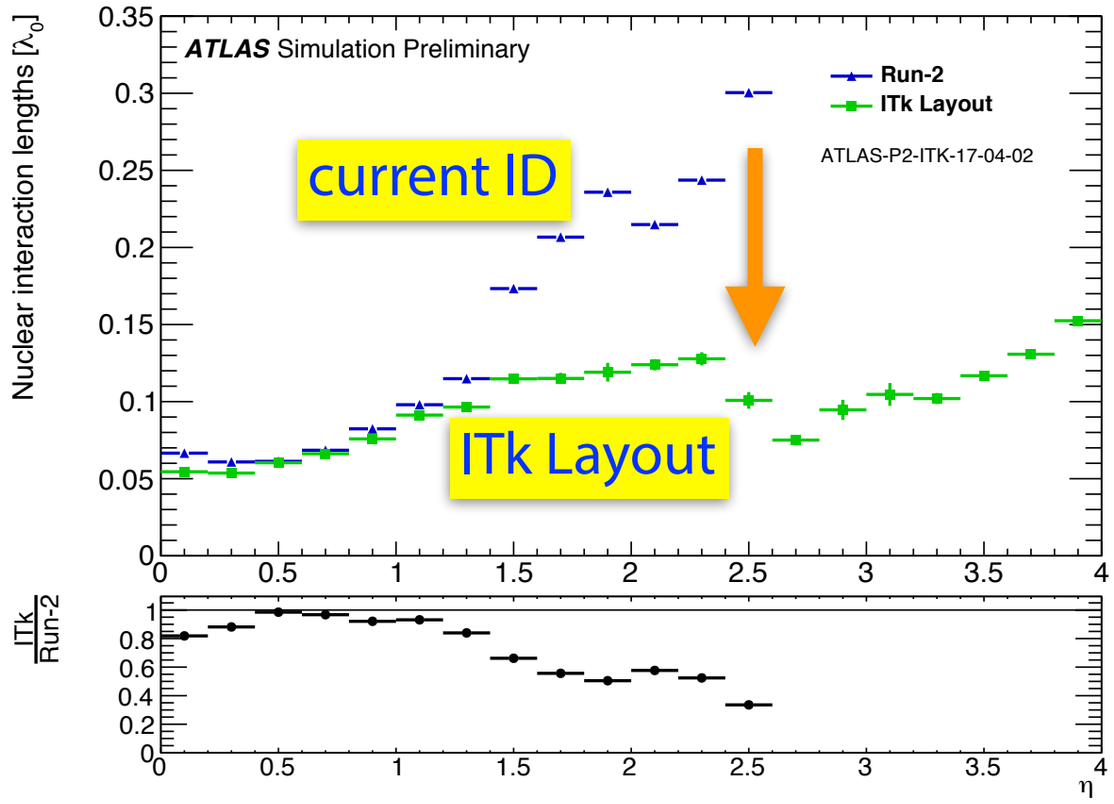


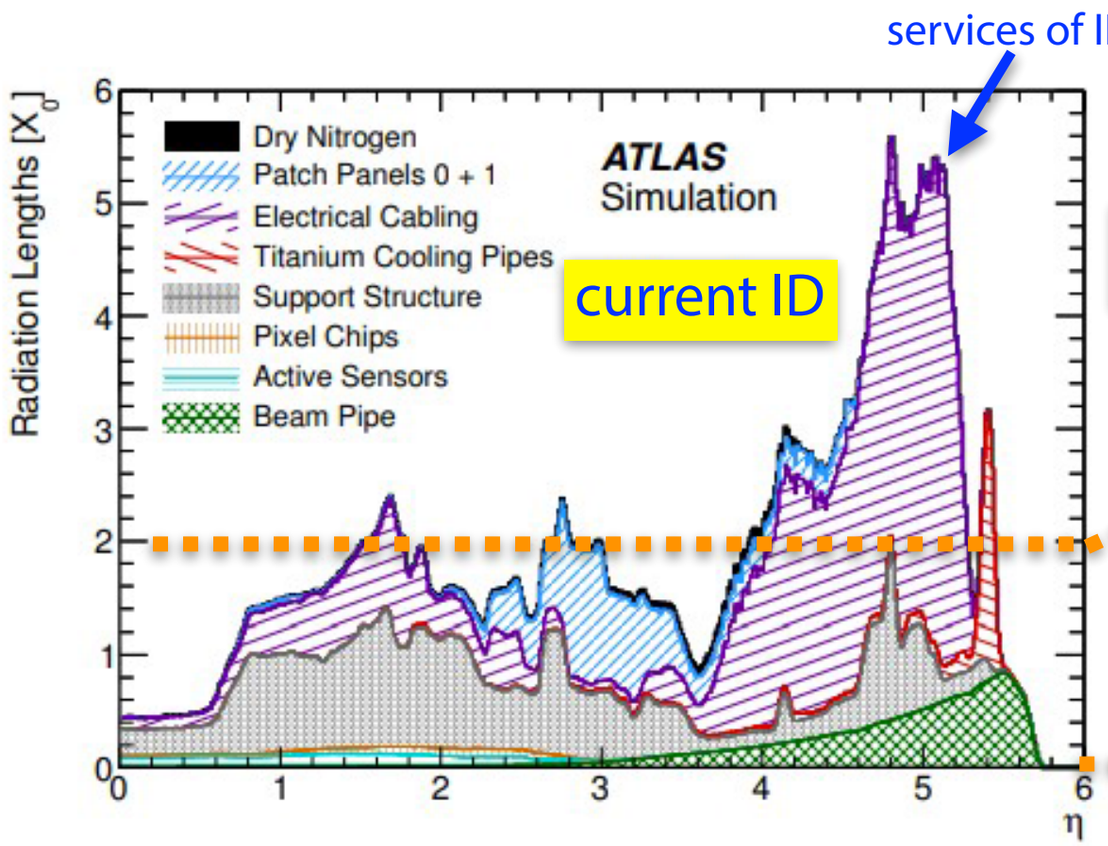
➡ CMS [TDR]:
- 3 double-strip
- 3 strip+pixel (trigger layers)
- 4 pixel layers
- total **10 layers**
- total **16 hits**



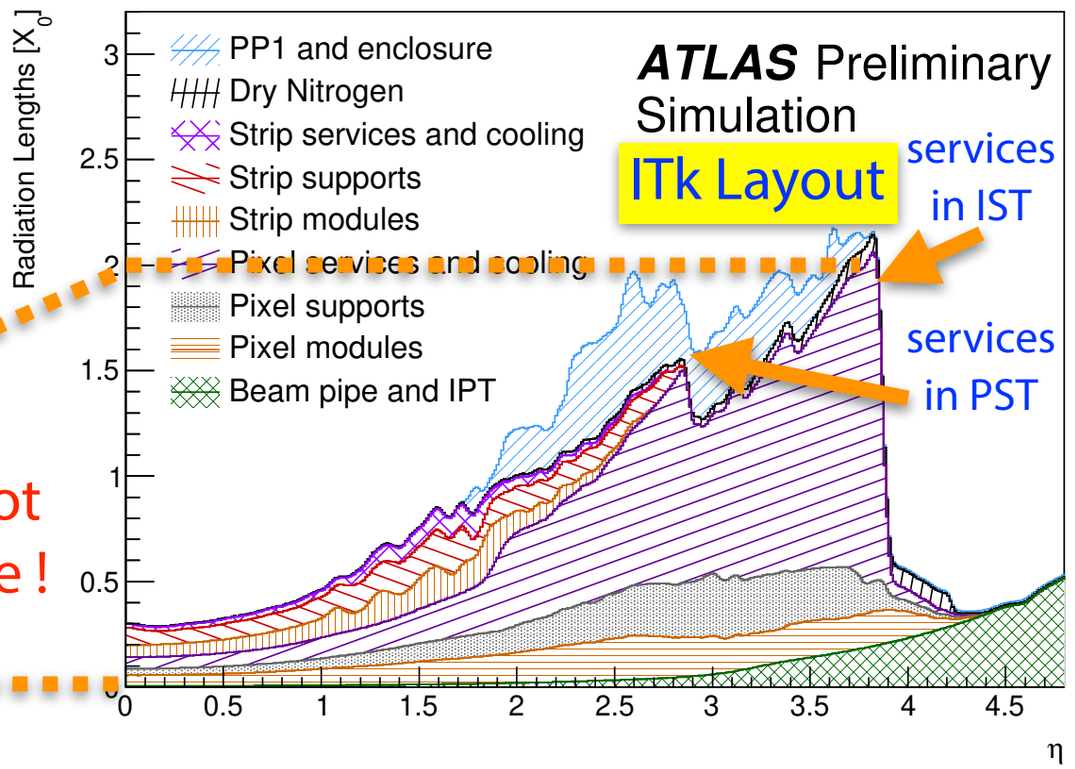
Passive Material ITk vs current ID

- ITk has less material that current ID
  - ➡ despite increase in channels, data rates, ...
  - ➡ inner Pixel services in IST dominating (geometry)
- reduction in λ_o until hit requirement
  - ➡ 7 hit cut for current ID, 9 hit cut for ITk, less in forward region (7-8)
  - ➡ reduced inefficiency due to hadronic interactions





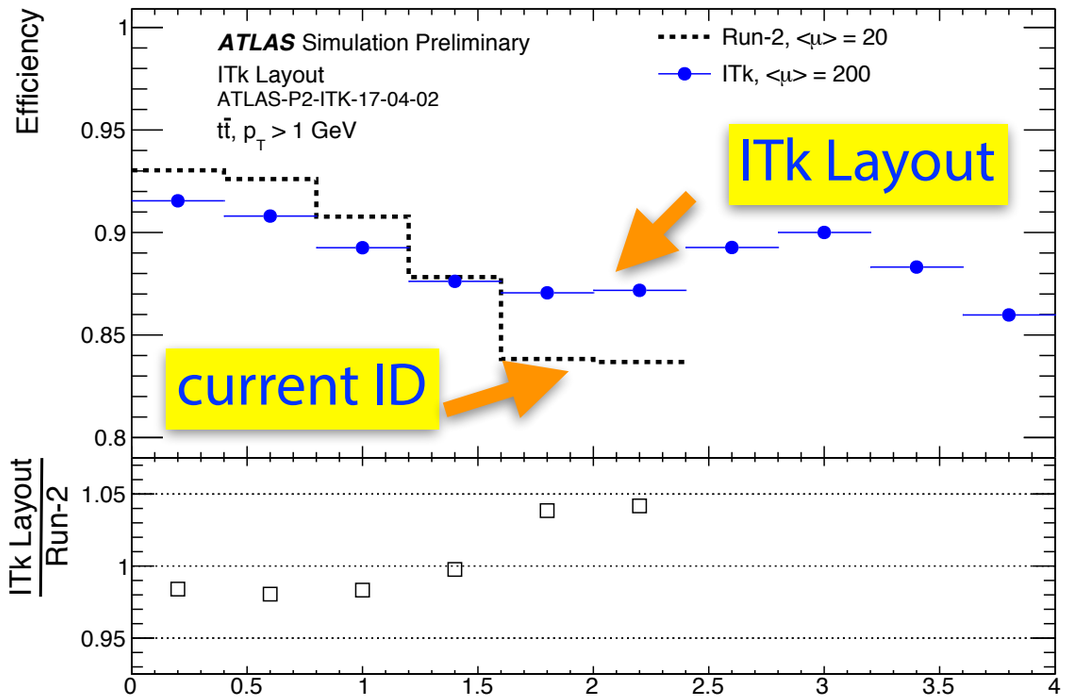
y-axis not the same !



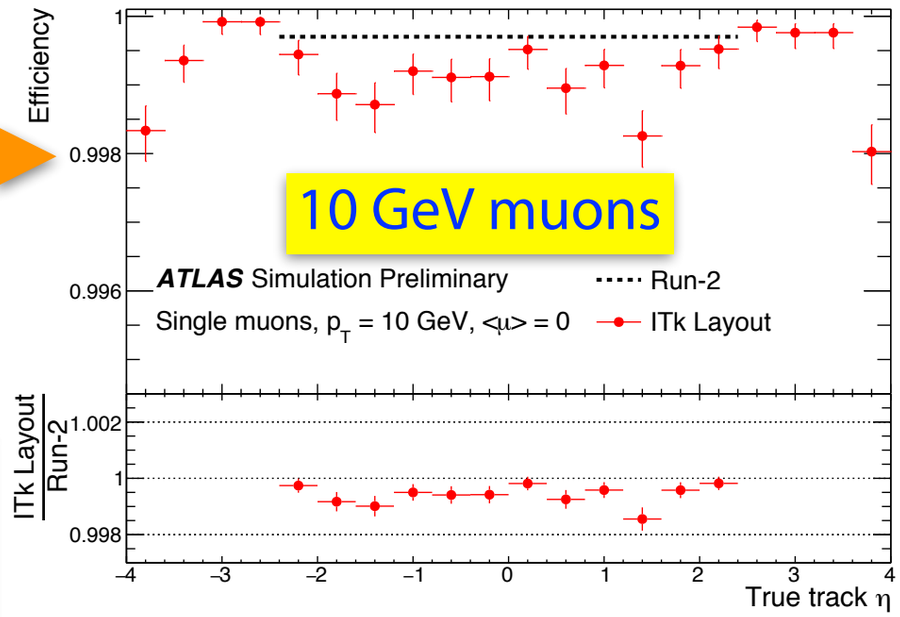
Performance: Efficiency and Fakes

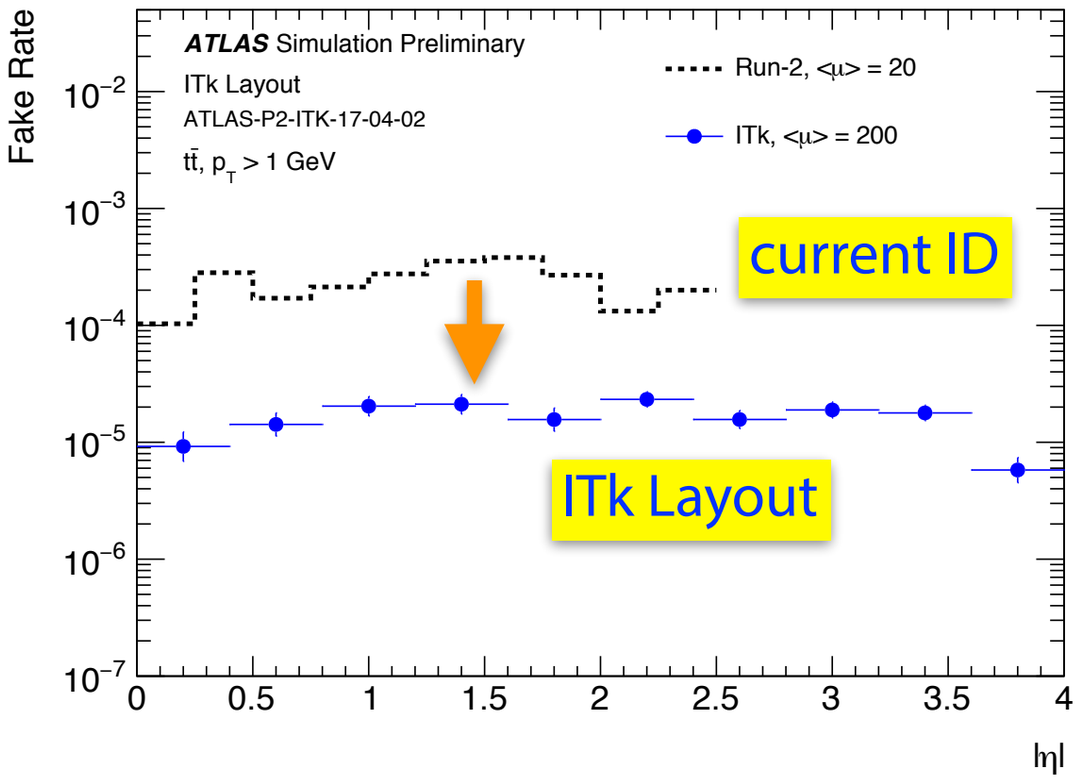
- track reconstruction efficiency
  - ➡ for muons: practically 1 (as expected)
  - ➡ for hadrons: inefficiency due to hadronic interactions dominate
  - ➡ ITk **efficiency stable** down to |η| of 4, despite 200 pile-up

- fake rate further reduce with ITk
  - ➡ tighter hit cuts than possible for current ID
  - ➡ **high purity** tracking with 200 pile-up



axis !





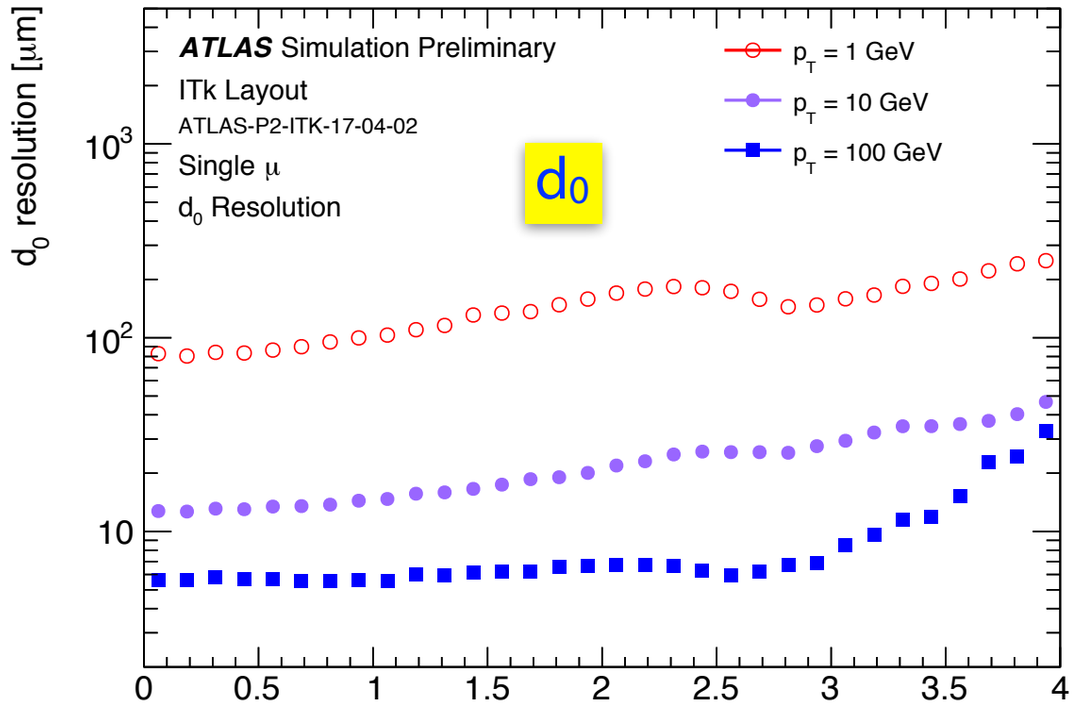
Performance: Impact Parameter Resolution

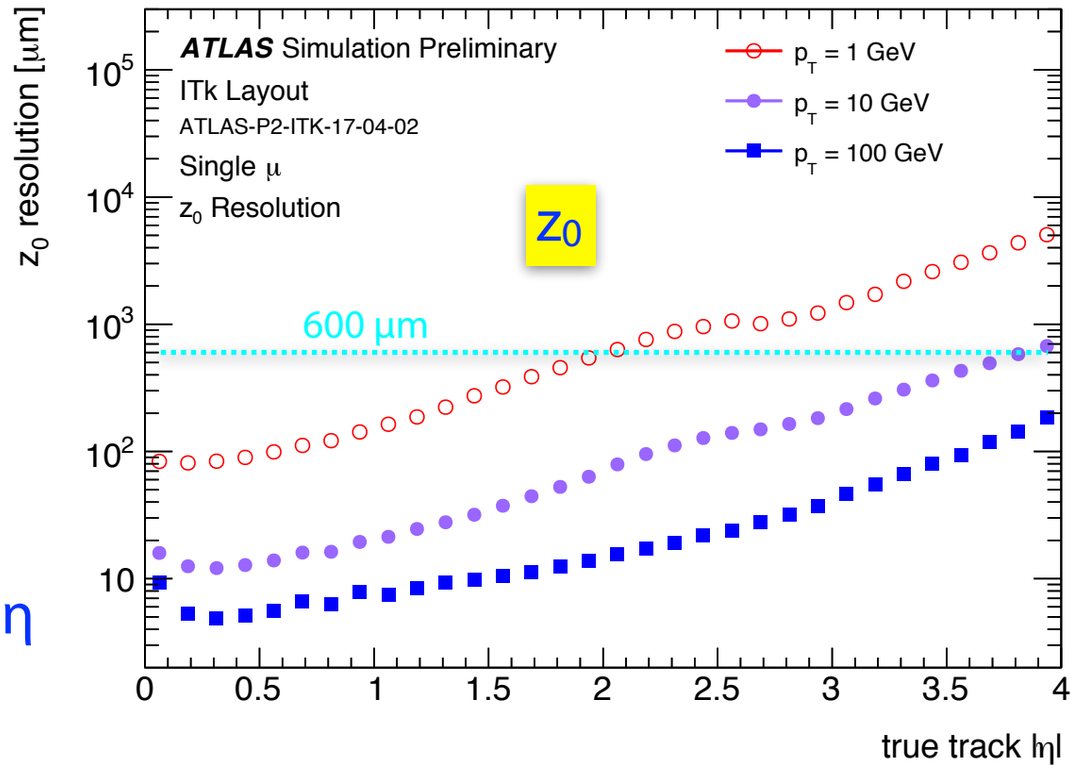
- resolutions benefit from:
  - ➡ **higher granularity** of Pixels
    - **25×100 µm²** in flat barrel **layer-0** (3D)
    - **50×50 µm²** elsewhere (3D, planar)

    (was 50×250(400) µm² for current ID)
  - ➡ staves in flat barrel of **layer-0** are at **34 mm**
    - limit for radiation hardness, thermal management and data rates

    (current IBL is at 33.25 mm)
  - ➡ **geometrical placement** of layers and rings

- resolutions in d_0 and z_0
  - ➡ at low p_T limited by **multiple scattering** (detector material)
  - ➡ d_0 resolution benefits from **smaller pitch** in layer-0 (relevant for b-tagging)
  - ➡ excellent z_0 resolution compared to typical **distance** between pile-up vertices (~ 600 µm)
  - ➡ excellent **forward resolutions**, even at high η

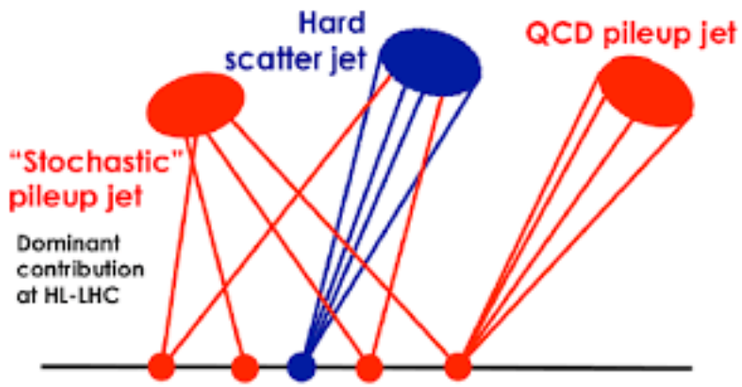




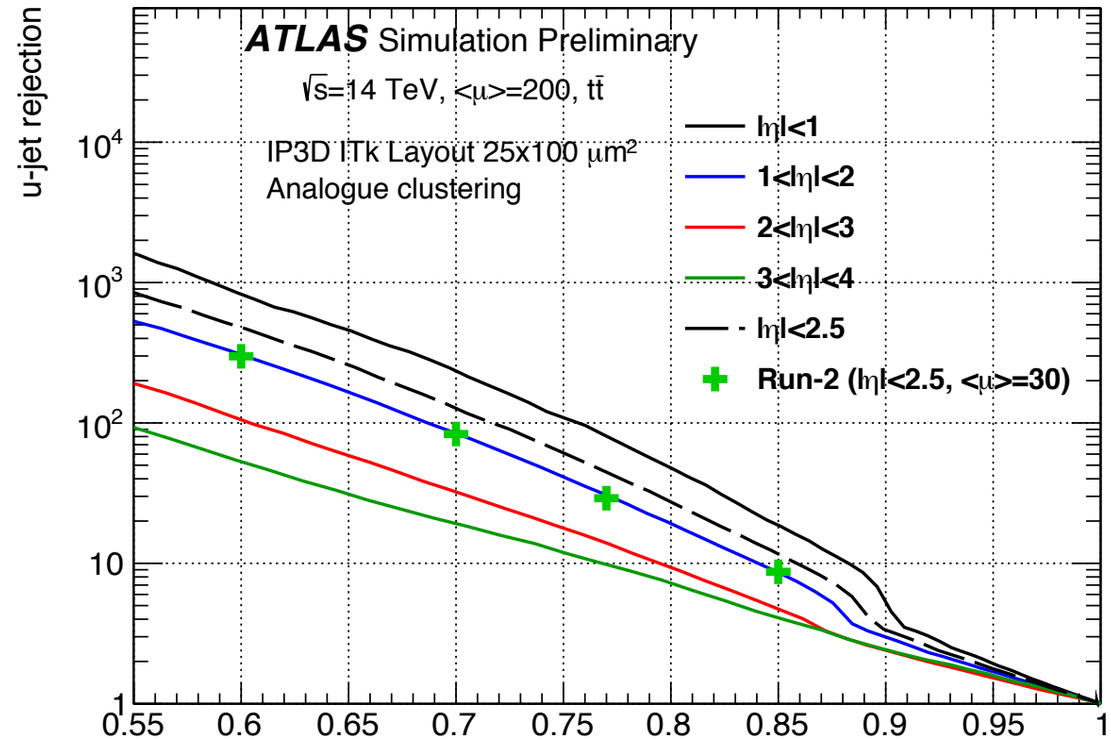
Performance: b-tagging and Pile-up Rejection

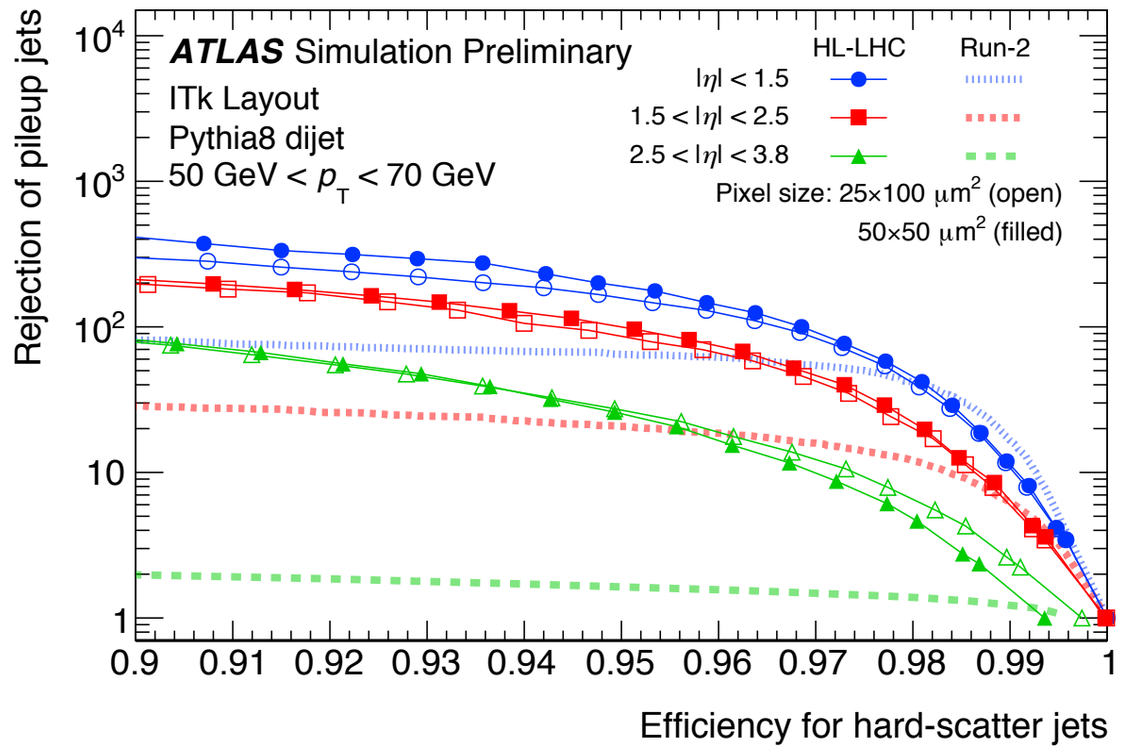
- b-jet tagging at 200 pile-up
  - ➡ impact parameter **tagging improves** over Run-2 performance
    - emphasis on improved d_0 resolution (pitch)
    - reduced fake rate, despite higher pile-up
  - ➡ **extended η-coverage** of b-jet tagging
    - excellent forward tracking performance

- pile-up jet rejection
  - ➡ exploits z-structure of interaction vertices along beam spot to reject pile-up jets



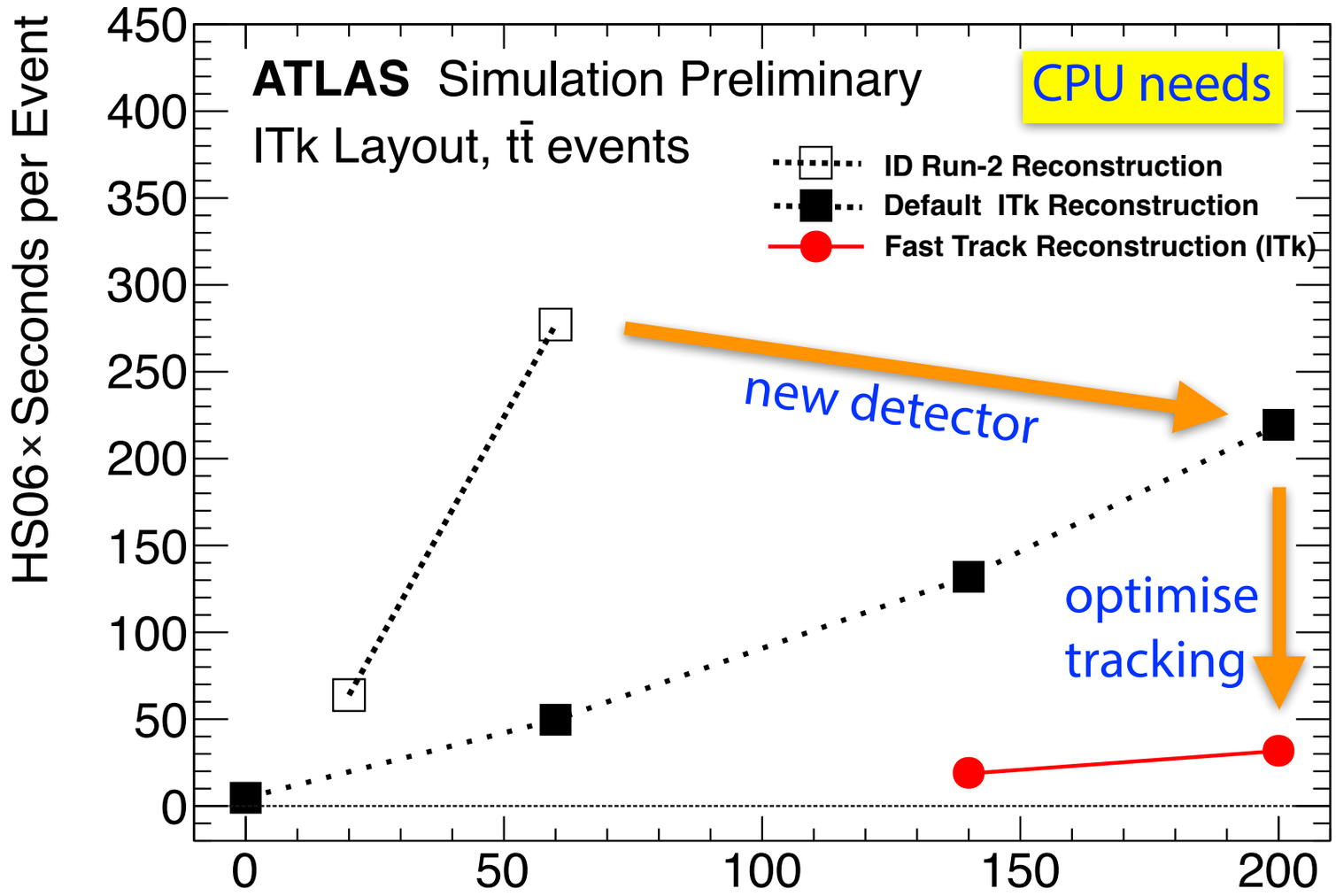
  - ➡ **ITk improves** over Run-2 performance
  - ➡ **η-coverage** extended to forward (VBF jets)

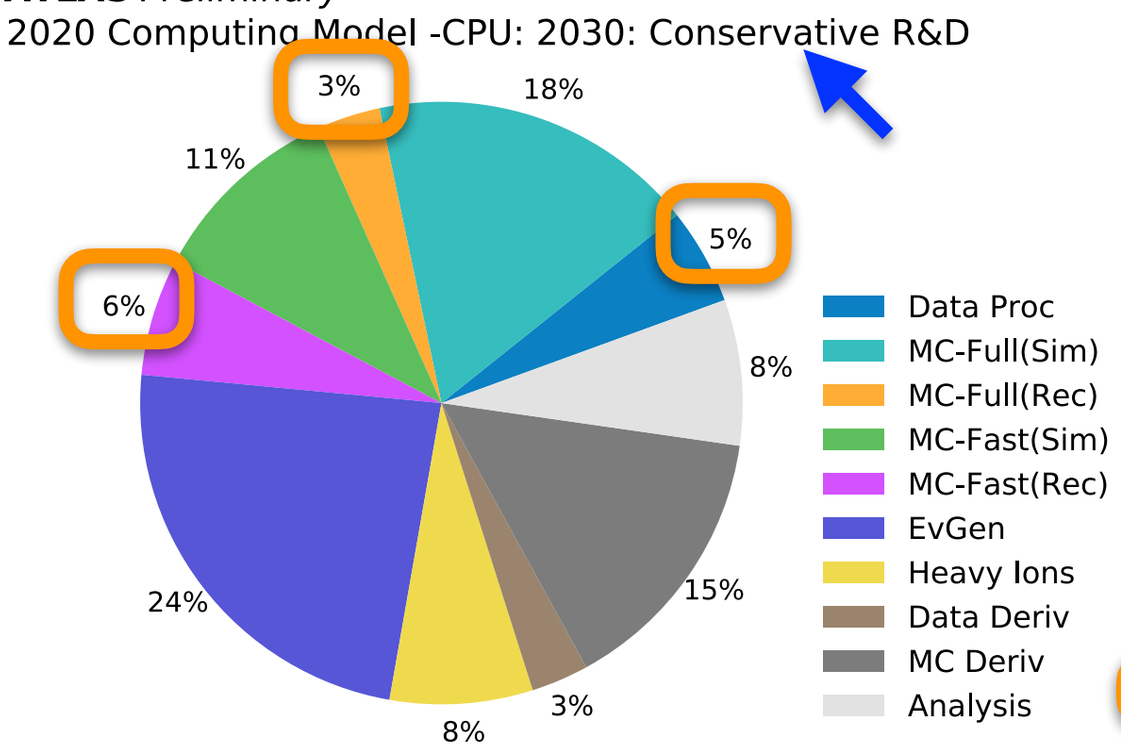




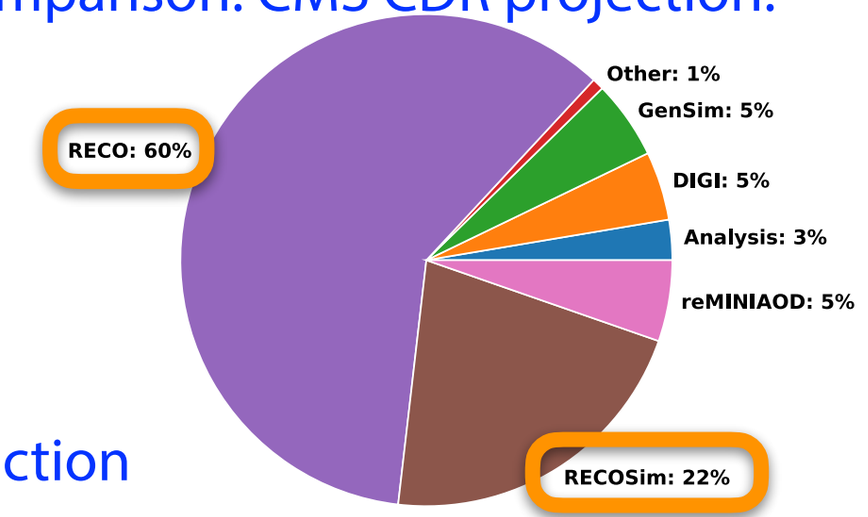
CPU Performance and Computing Model

- CPU major cost factor
  - ➡ default tracking with **ITk** reduces slope significantly
  - ➡ **optimised** ITk fast tracking (track seeding in Pixels, ...) prototype further reduces CPU
- Computing CDR
  - ➡ tracking **no longer CPU driver**





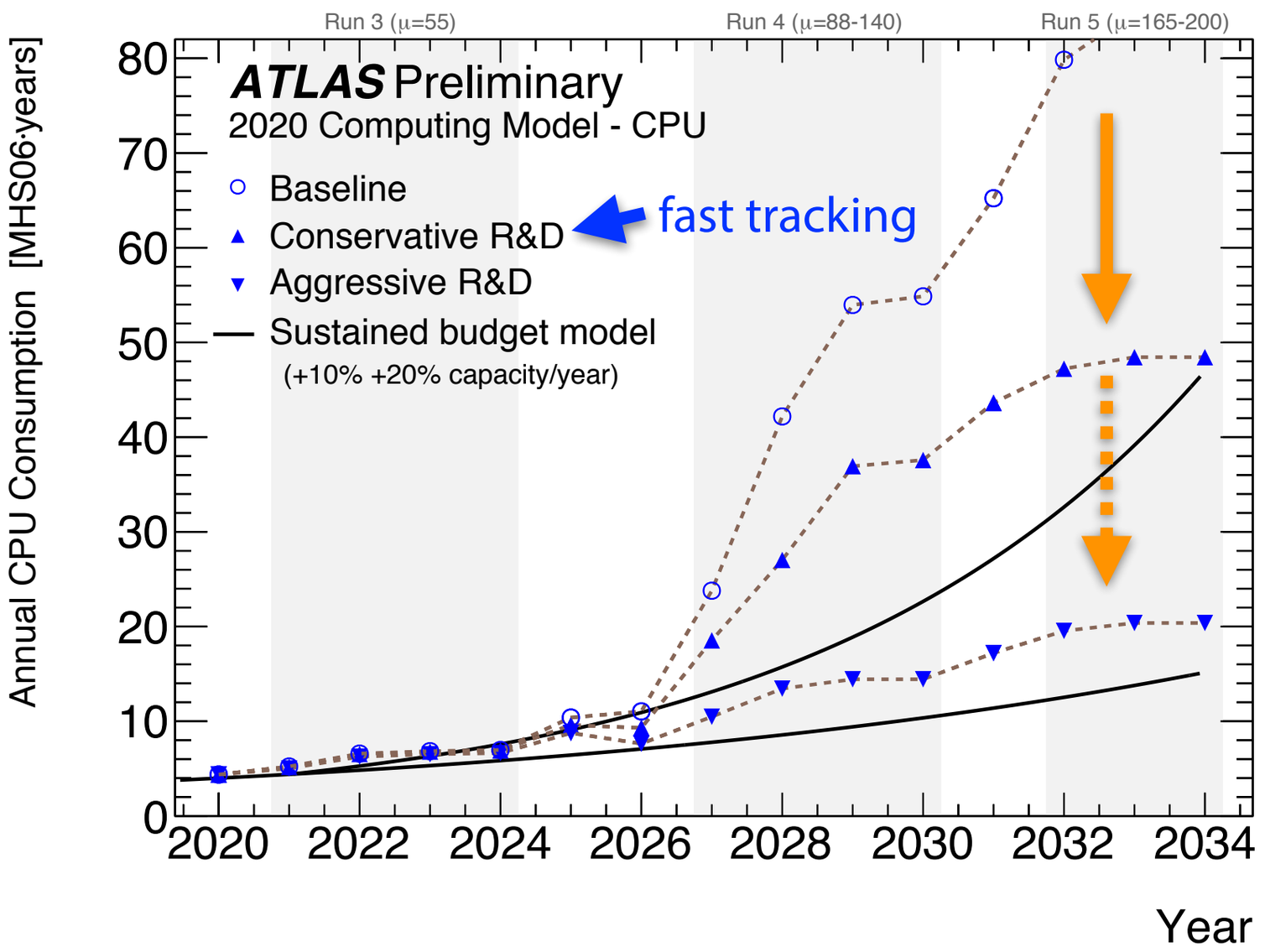
➡ for comparison: CMS CDR projection:

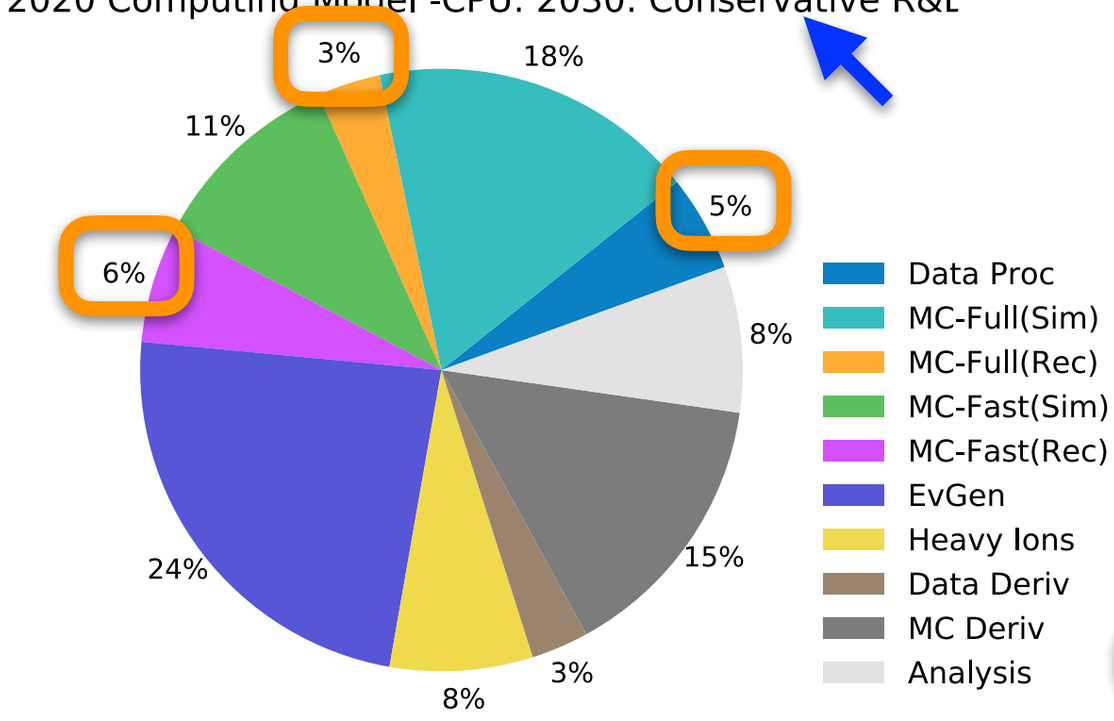


~ reconstruction

CPU Performance and Computing Model

- CPU major cost factor
  - ➡ default tracking with **ITk** reduces slope significantly
  - ➡ **optimised** ITk fast tracking (track seeding in Pixels, ...) prototype further reduces CPU
- Computing CDR
  - ➡ tracking **no longer CPU driver**
  - ➡ further **R&D** on fast simulation and physics generators needed





- constant computing budget
  - ➡ more aggressive SW R&D scenarios needed

~ reconstruction

Summary

- ATLAS Phase-2 tracker ITk is result of design process that started with the Scoping Document layout in 2015
  - ➡ challenging conditions in terms of pile-up, data rates, radiation, ...
  - ➡ ambitious physics requirements and limited computing resources
  - ➡ result is an all silicon tracker design that extends η coverage to 4 (2.5 for current ID)

- innovative Pixel support structures
  - ➡ 5 layer Pixel detector requires same Pixel sensor surface as classical 4 layer system
  - ➡ optimised hit coverage, tracking performance, efficient usage of CPU for tracking

- ITk out-performs current ID in all relevant parameters
  - ➡ high efficiency and high purity tracking, despite 200 pile-up
  - ➡ excellent d_0 and z_0 resolutions allow for excellent b-tagging and pileup jet rejection
  - ➡ fast ITk track reconstruction will not be CPU resource driver for Phase-2