

Current and future developments of CMOS pixel sensors

Focus on activities at C4PI, Strasbourg

Jerome Baudot
with Christine Hu-Guo's help



- Brief overview of activities in the past 20 years
- The spatial resolution “case”
- Sensors driven by spatial resolution

Overview: the ~10 first years

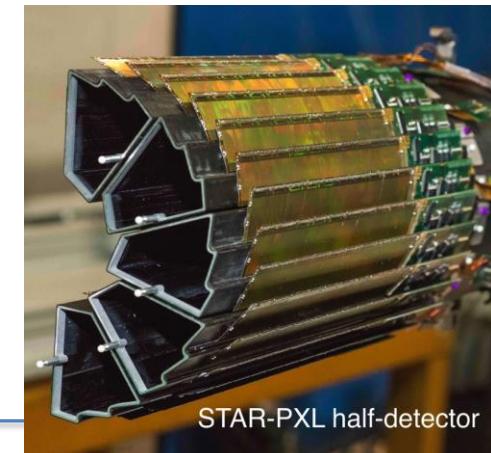
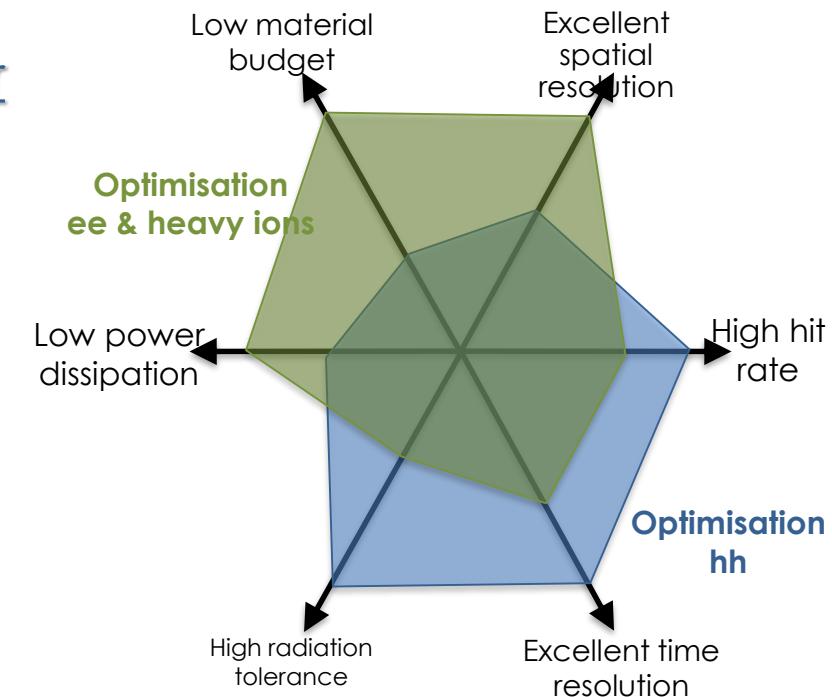
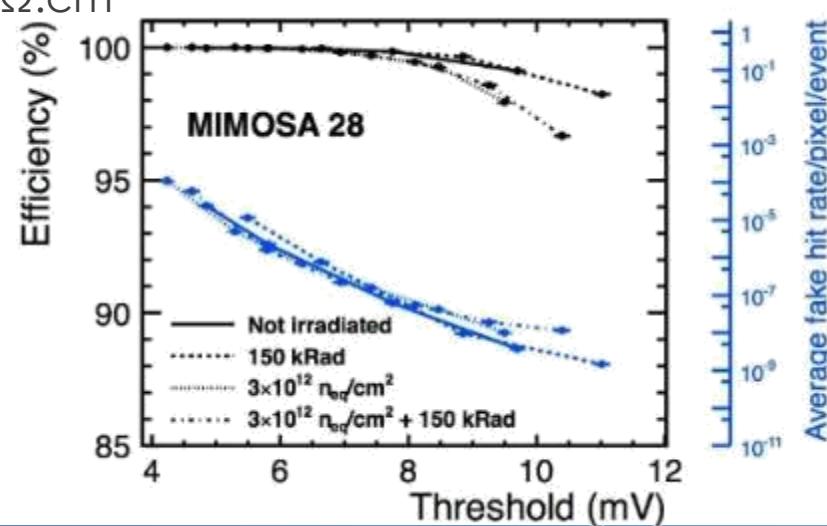
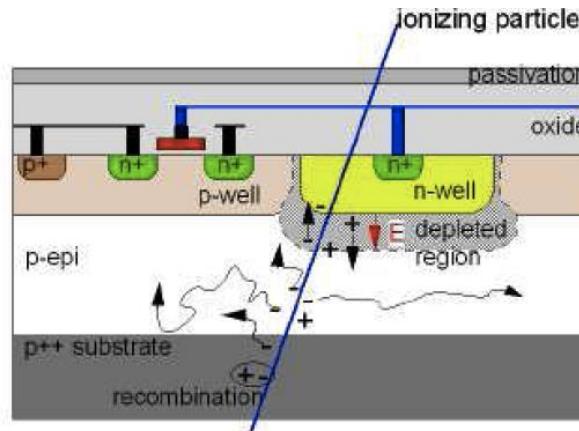
Initial motivation = new optimization for ILC vertex detector

- Late 90's
- [R.Turchetta NIM A 458 \(2001\) 677](#)



The STAR – PXL

- Collab. IPHC – BNL
- MIMOSA-28 sensor
 - AMS 350 nm technology
 - already with resistivity > 400 Ω.cm
- **50 μm thick, 20.7 μm pitch**
- 160 mW/cm²
- Hit-rate > MHz/cm²
- Operation 2014-2016
- [I.Valin JINST 7 \(2012\) C01102](#)
- [G.Conti A 907 \(2018\) 60](#)



Overview: the past ~10 year – part 1

■ Exploration of new CMOS process

- Quadruple well
- or High-voltage
 - Large collection diode
 - **See next talk by H.Zhang**

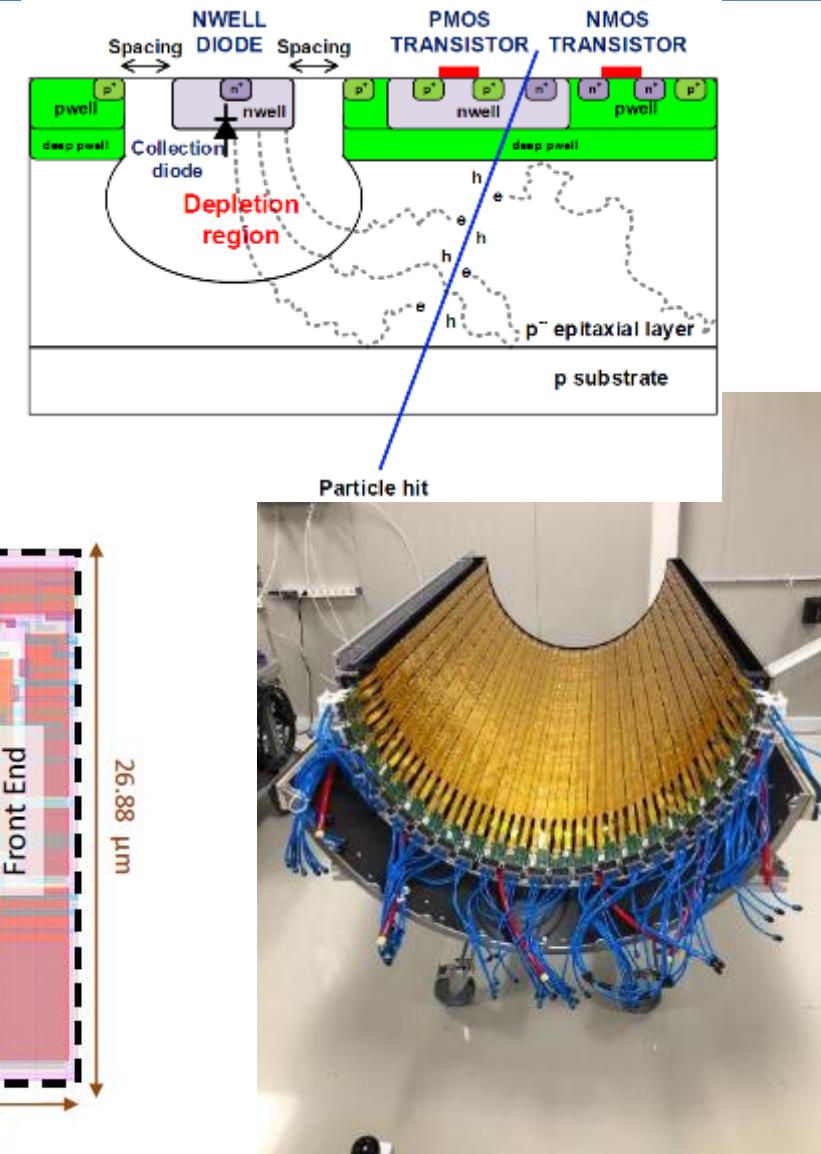


Powerful in-pixel treatment & read-out architecture



■ The ALICE - ITS2

- Large collab. around CERN
- ALPIDE sensor
 - Tower-Jazz 180 nm
- **40 mW/cm²**
- **hit rate 100 MHz/cm²**
- Total surface covered **10 m²**
- [A.Rinella NIM A 845 \(2017\) 583](#)



Overview: the past ~10 year – part 2

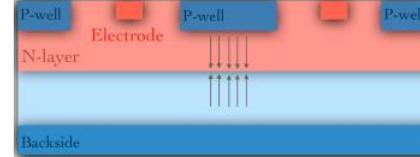
New sensitive layer

- High resistivity epitaxy combined with
- Shallow but N-implant
- [W.Snoeys NIM A 871 \(2017\) 90](#)

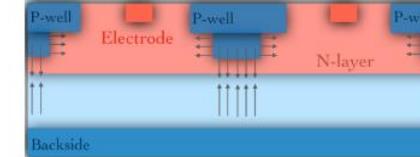
Short collect.
time ~ns



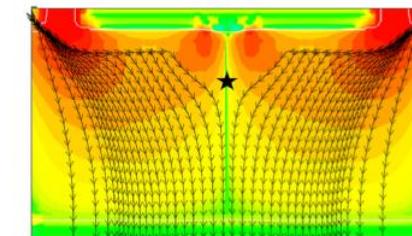
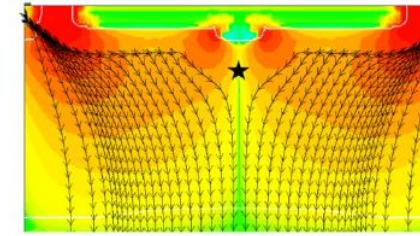
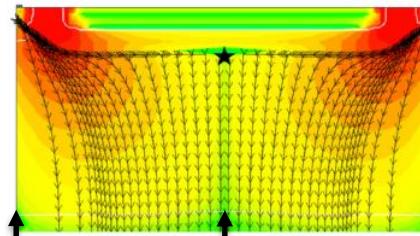
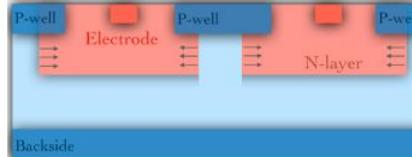
modified process (mp) – “standard”



mp + additional p-implant



mp + gap in n-layer



[M.Munker JINST 14 \(2019\) C05013](#)

Higher radiation tolerance

- Interest in ATLAS – ITK community

Toward tolerance to

- Fluence 10^{15} n_{eq}/cm²
- TID ≥ 1 MGy

- Large sensors ($\sim 2 \times 2$ cm²)
- MONOPIX-2
- MALTA
- ATLASpix3 / MuPix

Pixel pitch

33x33 μm^2

36x36 μm^2

50x150 μm^2

Not to forget, closely related R&Ds

- SEED & ARCADIA projects at INFN
 - LFoundry 110 nm, HR sensitive layers
 - See P.Giubilato's talk on Monday
- SOI technology
 - LAPIS 200 nm
 - See M.Yamada [monolithic SOI @ Vertex 2020](#)

The spatial resolution “case”

A well-known fact ⇒ Charge sharing drives heavily spatial resolution

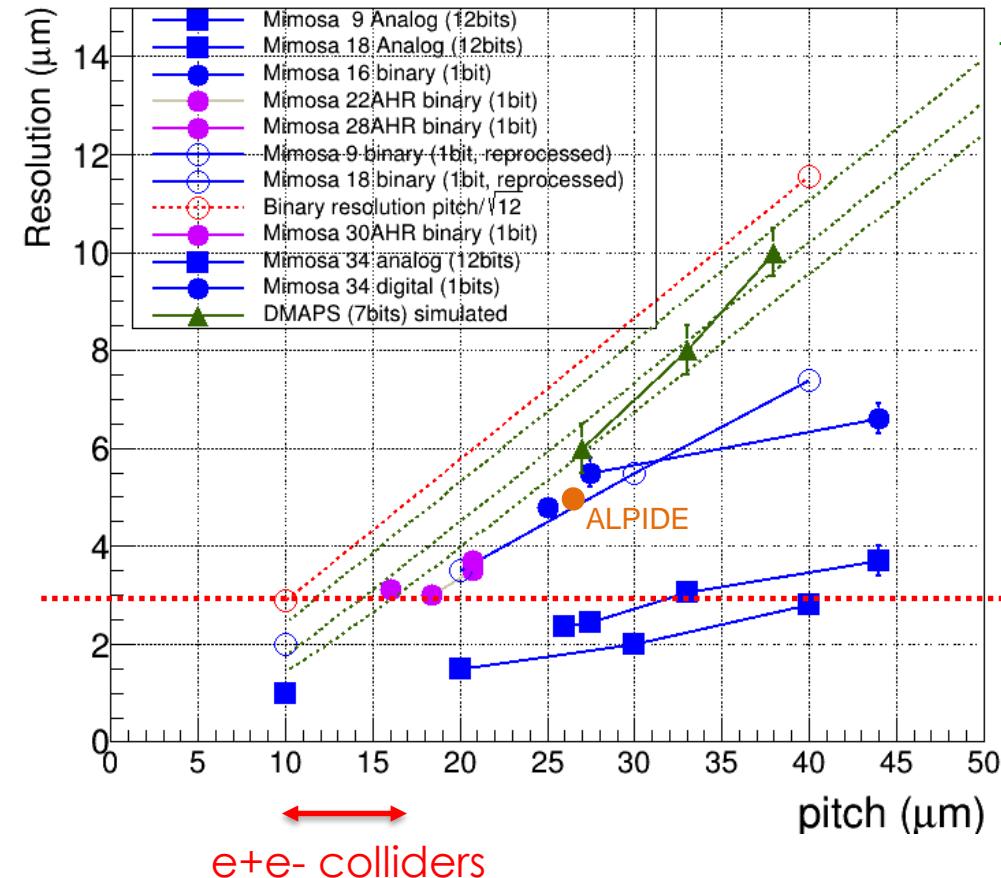
■ Partial depletion

- Charge collection shared between diffusion and E-drift
- Rather strong charge sharing ☺
- Not easy to simulate!
 - Still strong progresses: TCAD+Allpix²
 - Ex: [D.Dannheim NIM A964 \(2020\) 163784](#)

■ Full depletion

- Charge collection dominated by E-drift
- Charge sharing limited ☹
 - Still more comfortable / SNR
- Relatively easy to simulate and understand
 - Gaussian transverse diffusion ⊗ pixel size

Measurements & simu. from MIMOSA series



Simulation inspired
by Monopix-1 sensor
with **full-depletion**
thickness

- 10 μm
- 20 μm
- 30 μm

Focus on activities in Strasbourg

Scientific groups @ IPHC ⇒

	ALICE ITS3	Belle-II VXD upgrade	CBM MVD	ILC VTX	CEPC VTX	PICSEL group
Spatial res. (μm)	~5	< 10	~5	≤ 3	~3	► A.Besson M.Winter & al.
Mat. budget (%X0)	0.05	0.15	~0.3	0.15	0.15	
Hit rate (MHz/cm²)	100	100	15-70	~20	~10	
Time figure (ns)	100-10 ³	~100	5.10 ³	10 ² -10 ³	10 ² -10 ³	
Rad.hard. (kGy) (n_{eq}/cm²)		10/year 5x10 ¹² /y	5 /year < 7x10 ¹³ /y	1 /year 10 ¹¹ /y	1 /year 6x10 ¹² /y	
Common key feature →	Power diss. (mW/cm²)	20	< 200	< 200 in vaccum	~20 pow-puls.	<50

IN2P3 core facility C4PI

- Dedicated to CMOS sensors
- Tech. & Scient. direction:
Christine Hu-Guo & J.Baudot



MIMOSIS sensor - Context

■ Goal

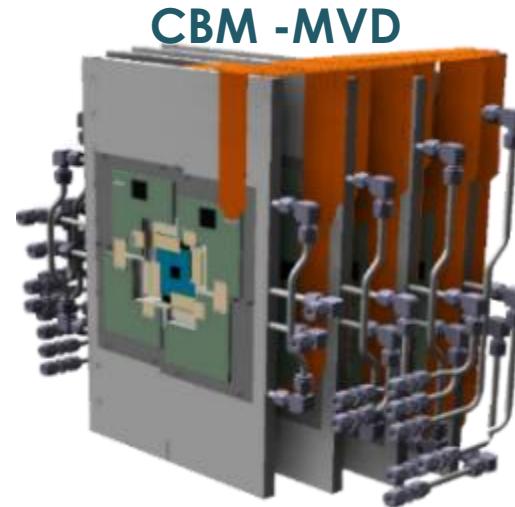
- Exploiting known TowerJazz 180 nm technology
- **combining low-power & high hit-rate**
- Follows ALPIDE FEE & priority encoder read-out

■ Dedicated experiment

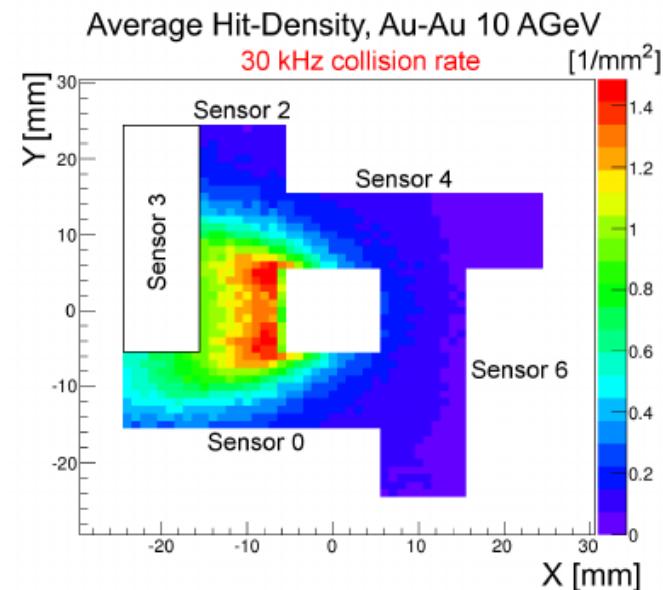
- CBM MicroVertexDetector (MVD)
- Collaboration: IPHC, IKFrankfurt, GSI, H2020-CREMLIN+

■ Timeline

- 2020: MIMOSIS-1
- 2021: MIMOSIS-2
- ~2023: final chip=MIMOSIS-3



J.Stroht Bormio 2018
M.Koziel, DPG 2017



MIMOSIS sensor - Design

■ Pixel matrix

- Pixel area = $26.88 \times 30.24 \mu\text{m}^2$
- 504×1024 pixels structured in regions
- Global shutter: $5 \mu\text{s}$ integration time

■ Read-out architecture

- Elastic memory concept (9 events storage capacity)
- 8 outputs (320 Mbps) for $\sim 2.5 \text{ Gb/s}$

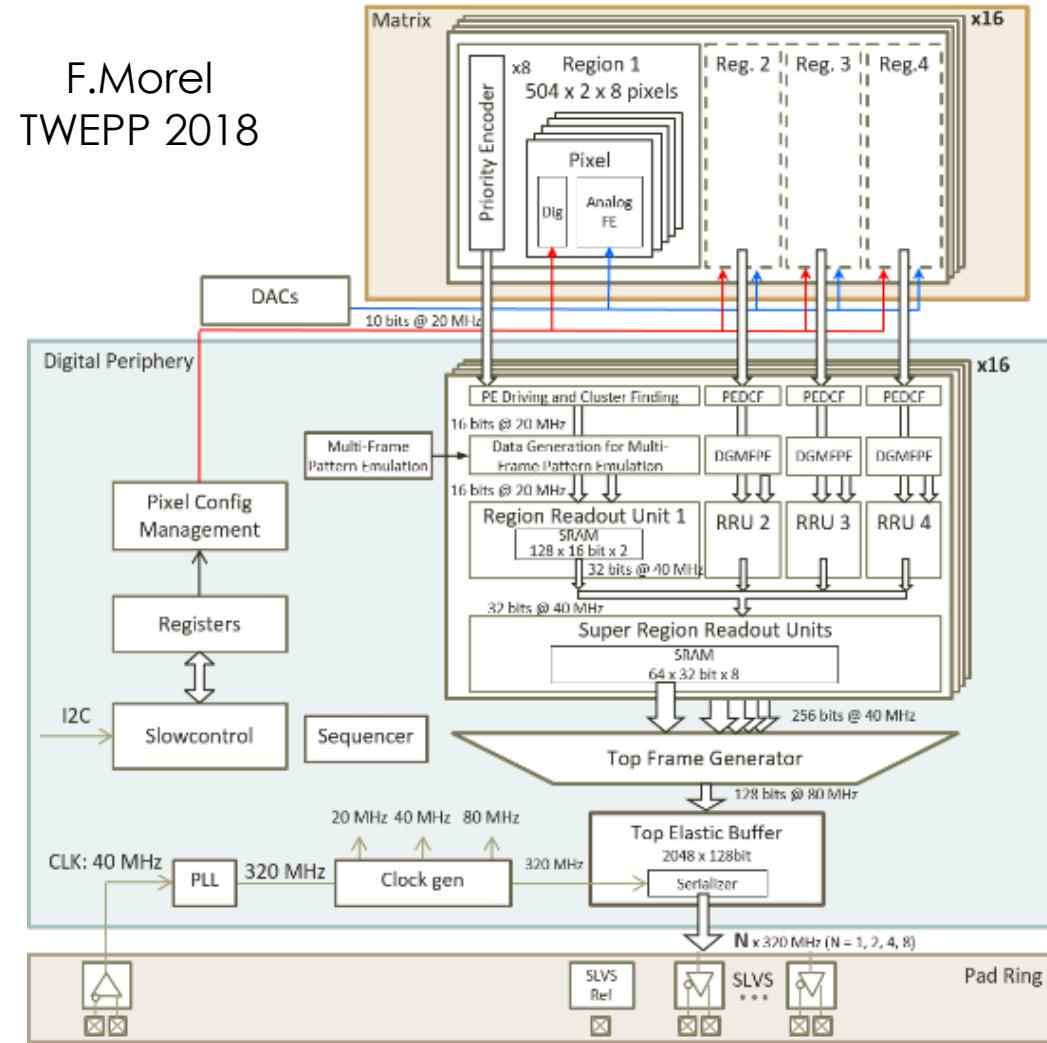
■ Single-Event-Effects resilience

- Triple Modular Redundancy
+ Error Correction Code (PhD. Y.Zhou)

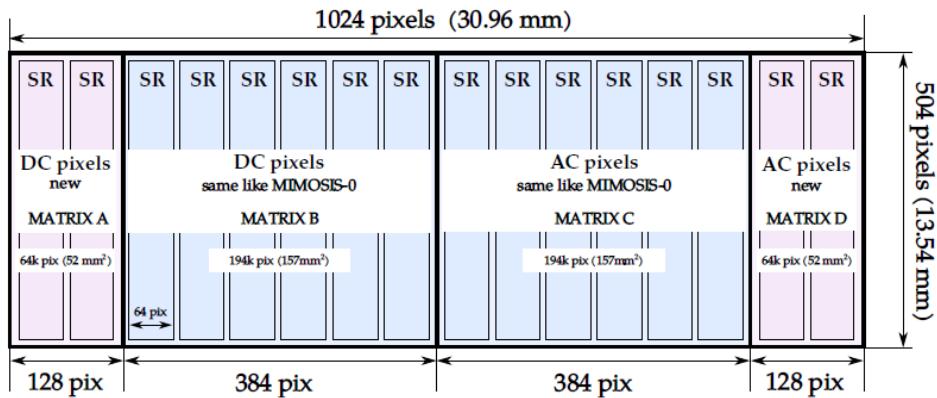
■ Power budget

Pixel/frame	1	640
Analogue (mW)	30	30
Digital (mW)	150	200
Total (mW/cm ²)	43	55

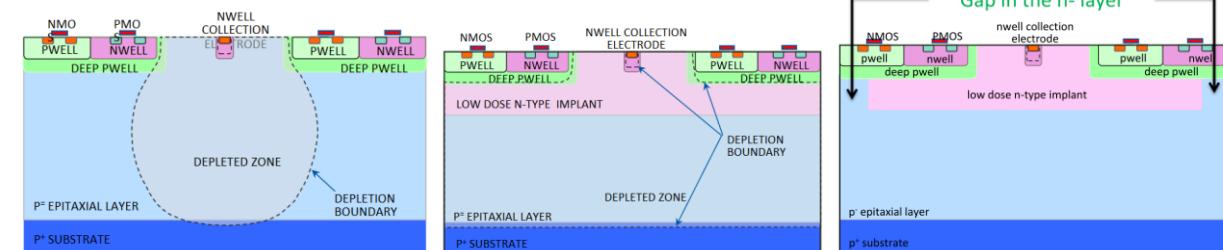
F.Morel
TWEPP 2018



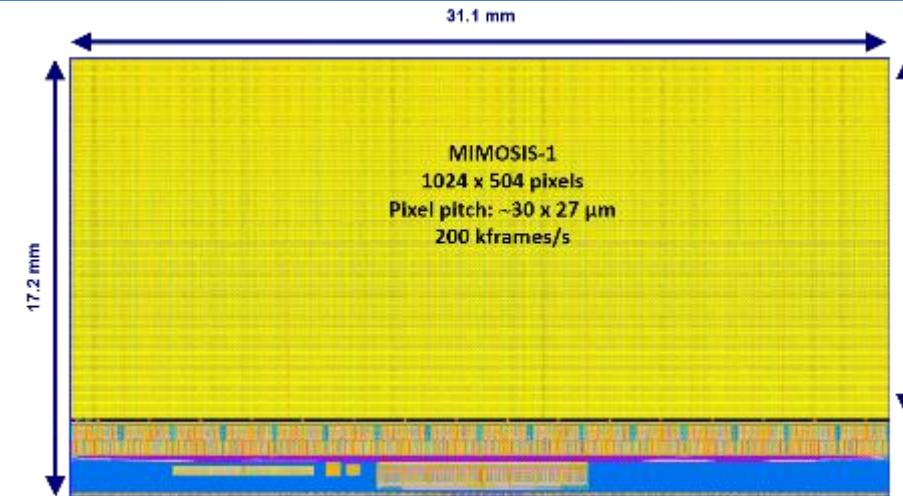
Pixel amplification



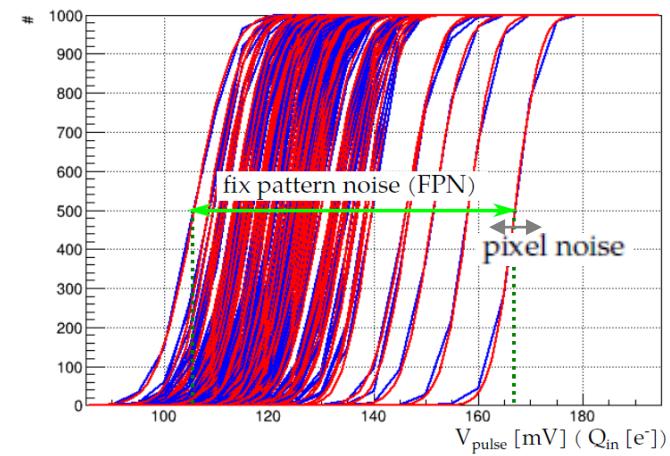
Sensitive layer



- Tint $\sim \mu\text{s}$ \rightarrow no in-time efficiency issue expected
 - Still need radiation tolerance assessment
- Careful study on spatial resolution dependence
 - With substrate modification
 - With biasing voltage
 - In connection with large analogue output sensor (Monolithic Imager, 20 μm pitch by M.Kachel)



Initial tests on-going @ IPHC



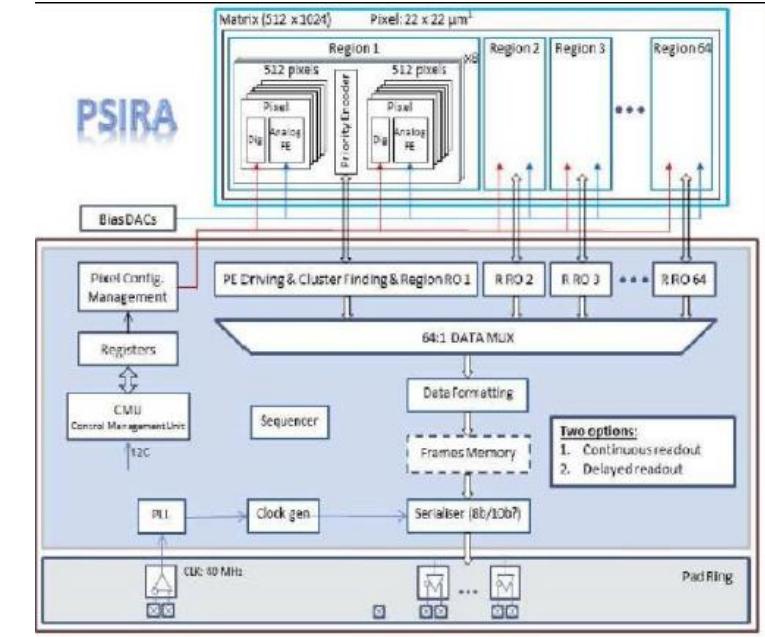
Spatial resolution $\lesssim 3\mu\text{m}$: 1st path

The 180 nm solution

- Evolution of MIMOSIS architecture for ILC → **PSIRA**
 - 4 μs integration time → 4-8 Bunch & 100 hits/cm²/ μs
 - ILC time-structure → power-pulsing
 - Interest to resolve BX
→ ~500 ns integration time
MIMOSIS-0Fast prototype (2021)
 - Minimal pitch $\sim 22 \mu\text{m}$ → spatial res. $\sim 4 \mu\text{m}$

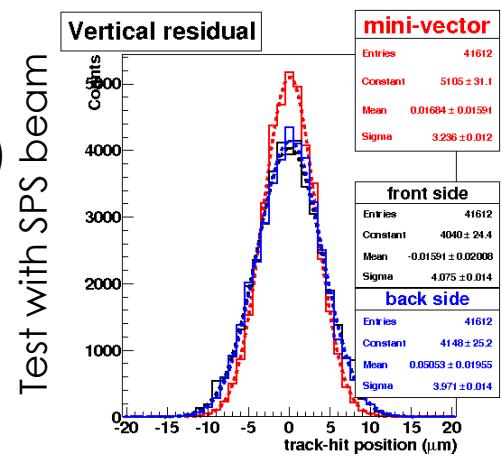
Power pulsing	Total det power
Without	100-120 W
With	15-30 W

From Auguste Besson



PLUME (2016) 0.4% X_0 (Bristol-DESY-IPHC)

Successfully operated
6 months during 2018
Belle II commissioning

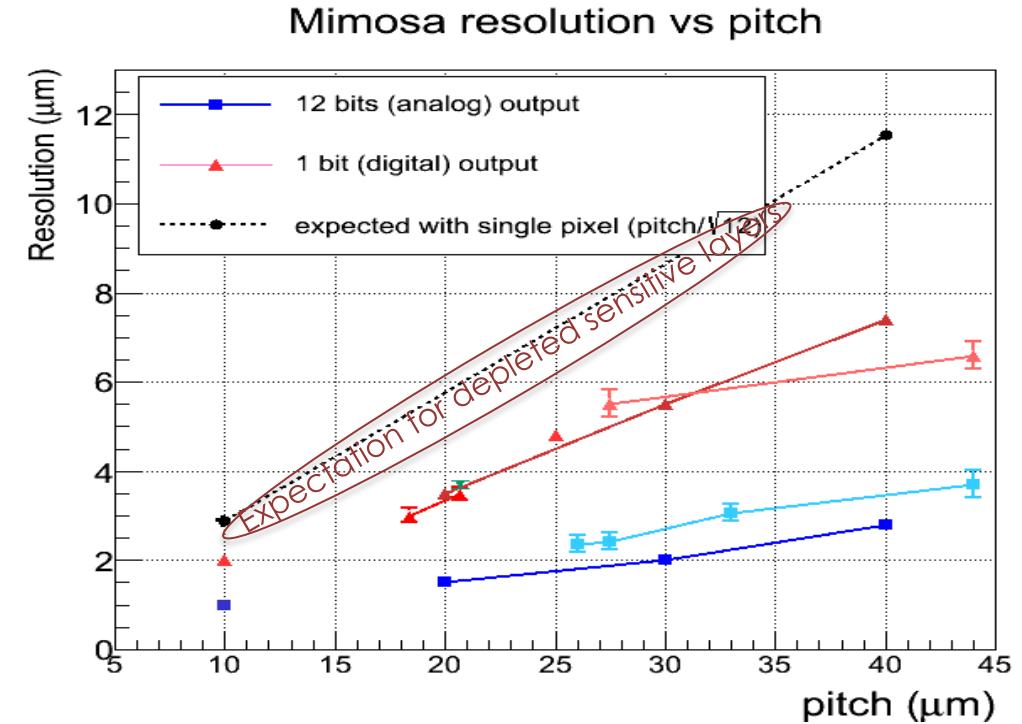


Spatial resolution $\lesssim 3\mu\text{m}$: 2nd path

■ The 65 nm solution

- The road to pixel size < 20 μm
- According to “predictions” 3 μm requires \Rightarrow
 - $\sim 10 \mu\text{m}$ fully depleted
 - $\sim 18 \mu\text{m}$ without depletion
 - Reachable assuming x2 size-reduction potential
- Current technology evaluation
 - With CERN EP-R&D Roadmap + partners
 - See Laura Gonella's talk on Monday
 - **Small exploratory matrices being submitted (Nov.2020)**
 - pixel size 10-25 μm , Various amplifications, AC/DC coupling
- Other benefits?
 - Lower power dissipation $\propto CV^2$ (power supply 1.2 V)
 - Stitching available

□ Lesson from techno 350 & 180 nm without depletion



Conclusion

■ CMOS pixel sensor: a mature technology

- Example: ALICE-ITS2 10 m² detector being commissioned
- Growing number of experiments opting for or considering the techno.
- Many active groups over the 3 regions

■ Still full potential to be further developed / explored

- Large sensors in known (TJ 180 nm & others) process pushing performances
 - However getting to 3 m with hit-rate>> MHz/cm² seems a hard limit
- A new 65 nm technology possibly a solution for the 3 μm spatial resolution
 - Should not be the only option explored
- **Not the end-of-story / colliders after 2030 ⇒ Continuous effort needed**

For full benefit



Specific integration studies required
See talks by F.Bosi & M.Mager

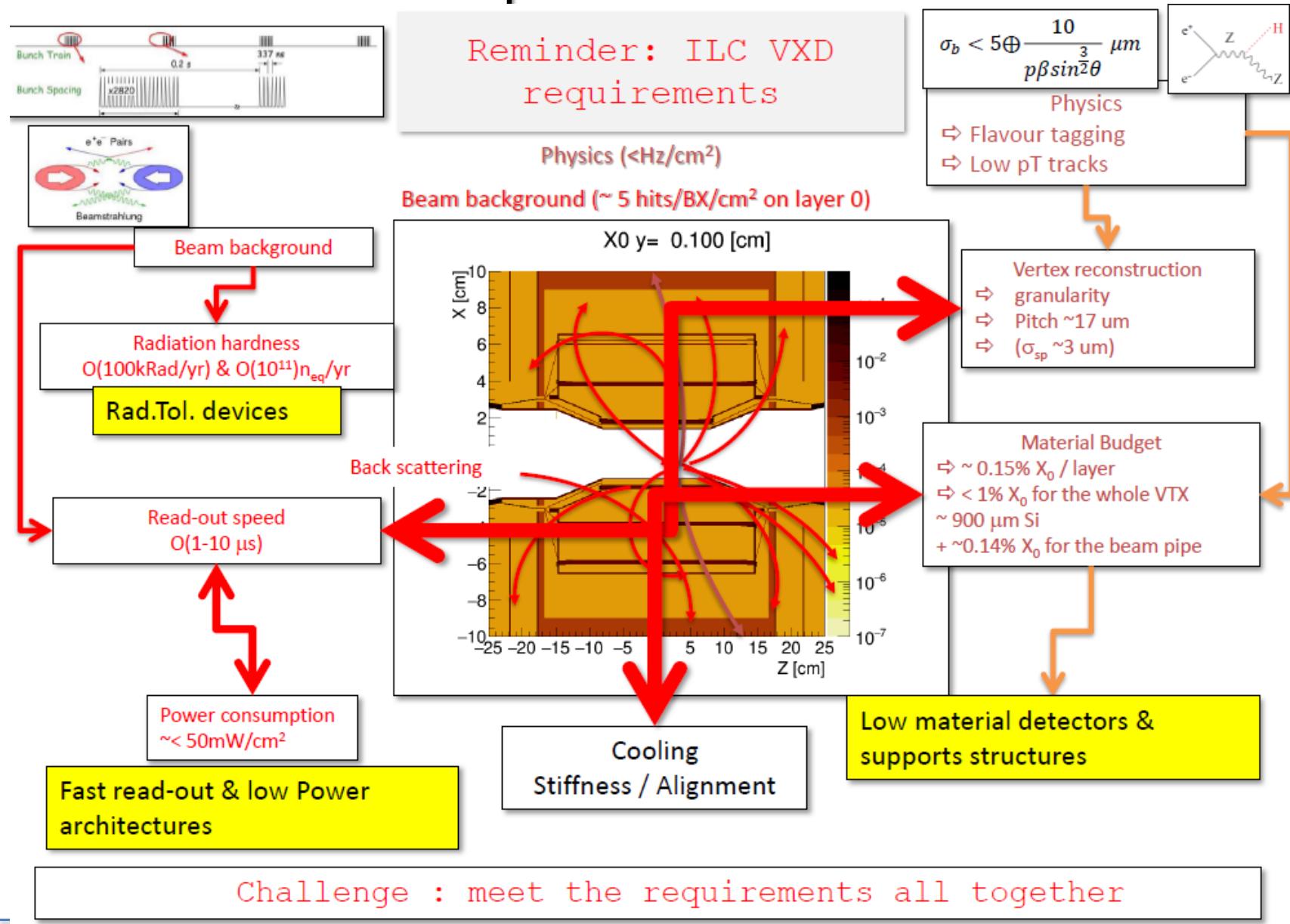


Thank you...

...bones slides

	STAR PXL	ALICE ITS2	HL-ATLAS ITK	CBM MVD	ALICE ITS3	Belle-II Lnom	ILC VTX	FCCee VTX	CLIC SiTrack	FCChh SiTrack
Spatial res. (µm)	< 10	~5	10	~5	~5	< 10	≤ 3	3 – 5	7	~10
Mat. budget (%X0)	0.37	0.35	<1	~0.3	0.05	0.15	0.15	0.15	~1	~2
Hit rate (MHz/cm²)	○(0.1)	○(1)	200	15-70	2x better / ITS2	100	20	○(20)	○(0.1)	
Time figure (ns)	200.10 ³	5.10 ³	25	5.10 ³		~100	10 ² -10 ⁴	10 ² -10 ³	5	5x10 ⁻³
Rad.hard. (kGy) (n_{eq}/cm²)	2 10 ¹²	30 2x10 ¹³	500 10 ¹⁵	30 /year < 10 ¹⁴ /y.		100 5x10 ¹³	10 < 10 ¹²	20 5x10 ¹¹	< 10 < 10 ¹²	100 5x10 ¹⁵
Sensor	MIMOSA 28	ALPIDE	R&D MONOPIX MALTA	MIMOSIS	R&D	R&D	R&D		R&D	
Techno (nm)	350	180	180 (150) modif.	180 modif.	65	180	180 / 65		180	
Pixel pitch (µm²)	20x20	28x28	33x33 36x36	27x30	target stitching	< 40x40	target 17x17		30x300	
Power (mW/cm²)	150	45	○(200)	< 55		target ~100	~3 Pow.Puls			

Scientific requirements: ILC - VTX



CEPC / FCCee

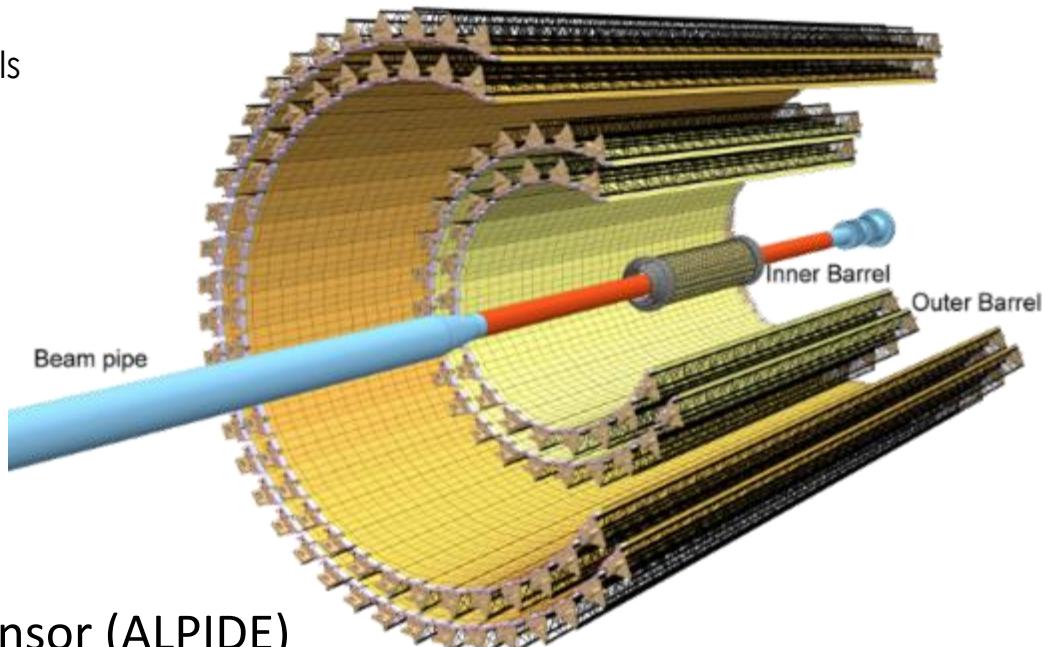
- Many similarities with ILC
 - ~ hit rates
 - granularity, mat.budget, rad.tol.
- Main difference: time structure



How to control power without power pulsing ?

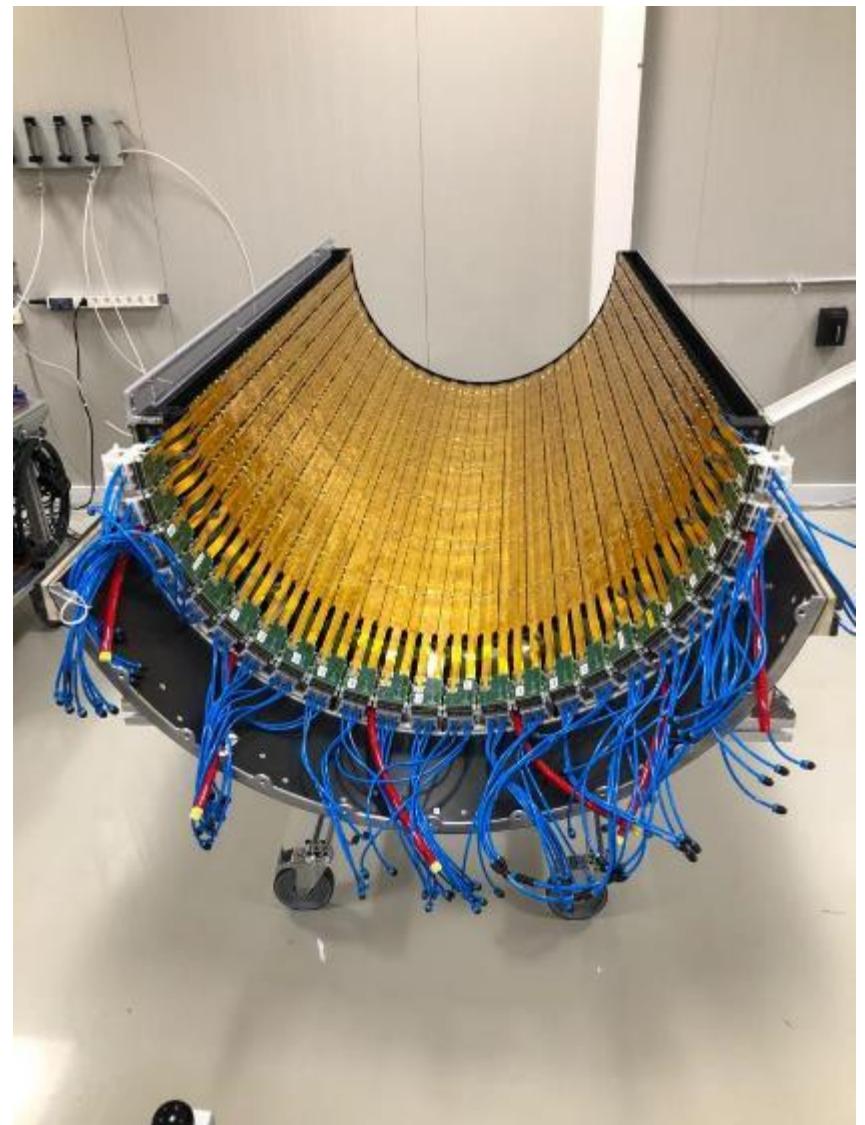
ALICE – ITS2

10 m², 12.5 Gpixels

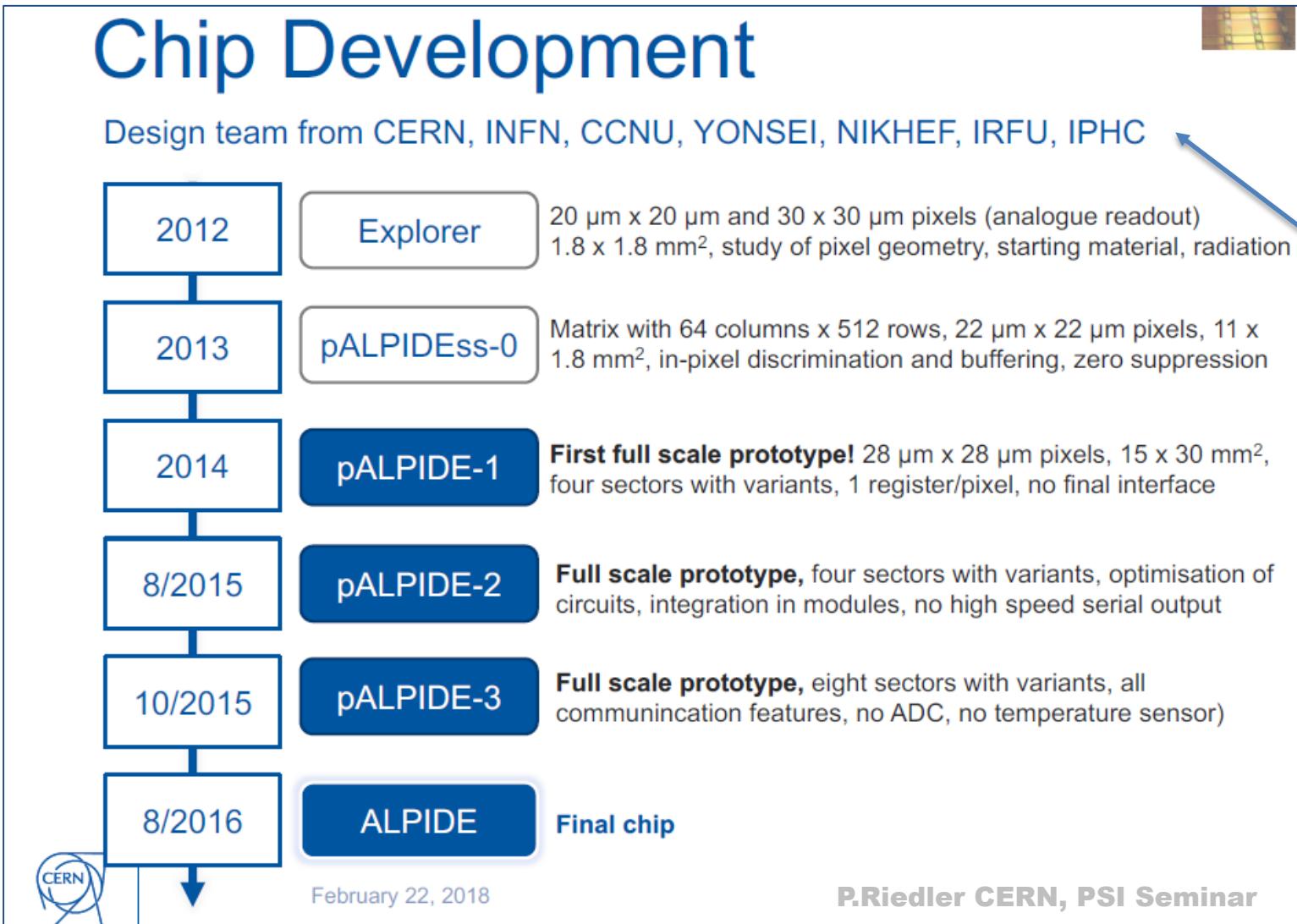


CMOS Pixel Sensor (ALPIDE)

- 10 m² active silicon area (12.5 G-pixels)
- 130,000 pixels / cm² (27x29x25 μm^3)
- Spatial resolution ~5 μm
- Power density < 40mW / cm²
- Max particle rate ~ 100MHz /cm² (pile-up)
- Max readout rate ~ 10 MHz/cm² (bandwidth)
- Fake-hit rate < 10⁻⁹ pixel/event



About timeline: the ALPIDE-ITS case



~4 years from tech-proto to final sensor

- Few remarks

- TJ180 nm exploration started in 2011
- This is not a small team

+3 years for assembly
(ALICE-ITS ~10 m²)

+

Belle II-VXD potential upgrade

Motivations

- $\sim 10^{36} \text{ cm}^2 \cdot \text{s}^{-1}$ luminosity → serious beam induced backgrounds
 - Might challenge current VXD operation & performances
 - All the more true if lumi upgraded x5
- => Consider/prepare for upgrade for ~2026 or beyond

Requirements

- Safe side of current extrapolation: hit-rate $\sim 100 \text{ MHz/cm}^2$
- Full-pixelated system → more robust/precise track reconstruction
- Difficult to get smaller/thinner beam-pipe ($\text{mm} / 0.5\% X_0$)
 - Limit interest for small pixels
 - Still lighter layers useful

Current VXD		Upgraded VXD
2 DEPFET layers	4 DSSD layers	5 to 7 full-pixel layers
$50 \times 70 \mu\text{m}^2$	$25 \times 60000 \mu\text{m}^2$	30×30 to $40 \times 40 \mu\text{m}^2$
$20 \mu\text{s}$	$\sim 5 \text{ ns}$ (offline)	50 to 100 ns
$0.2 \% X_0$	$0.7 \% X_0$	0.1% (inner) - 0.3% (outer) X_0

⇒ J.Baudot
[VERTEX 2020](#)

