



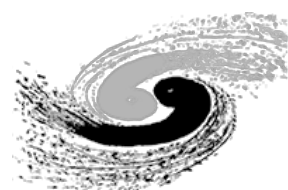
山东大学
SHANDONG UNIVERSITY

Physics | Lancaster University 

The Silicon Tracker Project

 Queen Mary
University of London

 UNIVERSITY OF
LIVERPOOL



Institute of High Energy Physics
Chinese Academy of Sciences

 清华大学
Tsinghua University

 **KIT**
Karlsruhe Institute of Technology

李政道研究所
Tsung-Dao Lee Institute

 上海交通大学
SHANGHAI JIAO TONG UNIVERSITY

 The
University
Of
Sheffield.

 University of
BRISTOL

 中国科学技术大学
University of Science and Technology of China



 哈尔滨工业大学 (威海)
HARBIN INSTITUTE OF TECHNOLOGY

 **UKRI**
Science and
Technology
Facilities Council

 西北工业大学
NORTHWESTERN POLYTECHNICAL UNIVERSITY

Progress and developments since the first idea was presented by at CEPC workshops in Oxford and Beijing:

https://indico.cern.ch/event/783429/contributions/3379826/attachments/1831027/2998576/Muenstermann_CMOS-for-CEPC.pdf

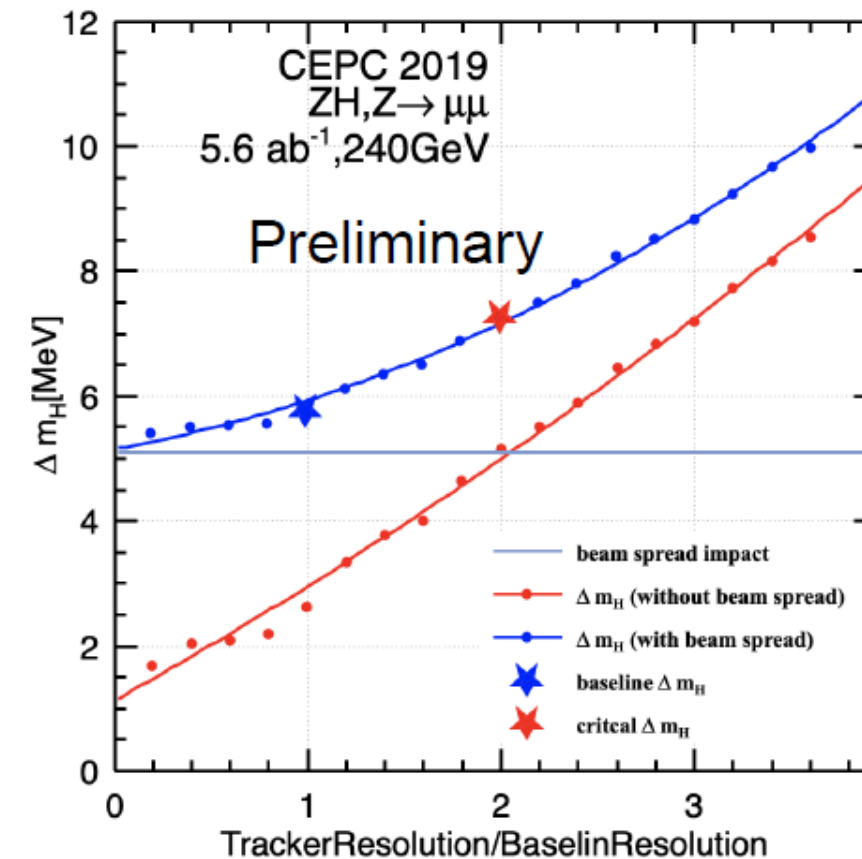
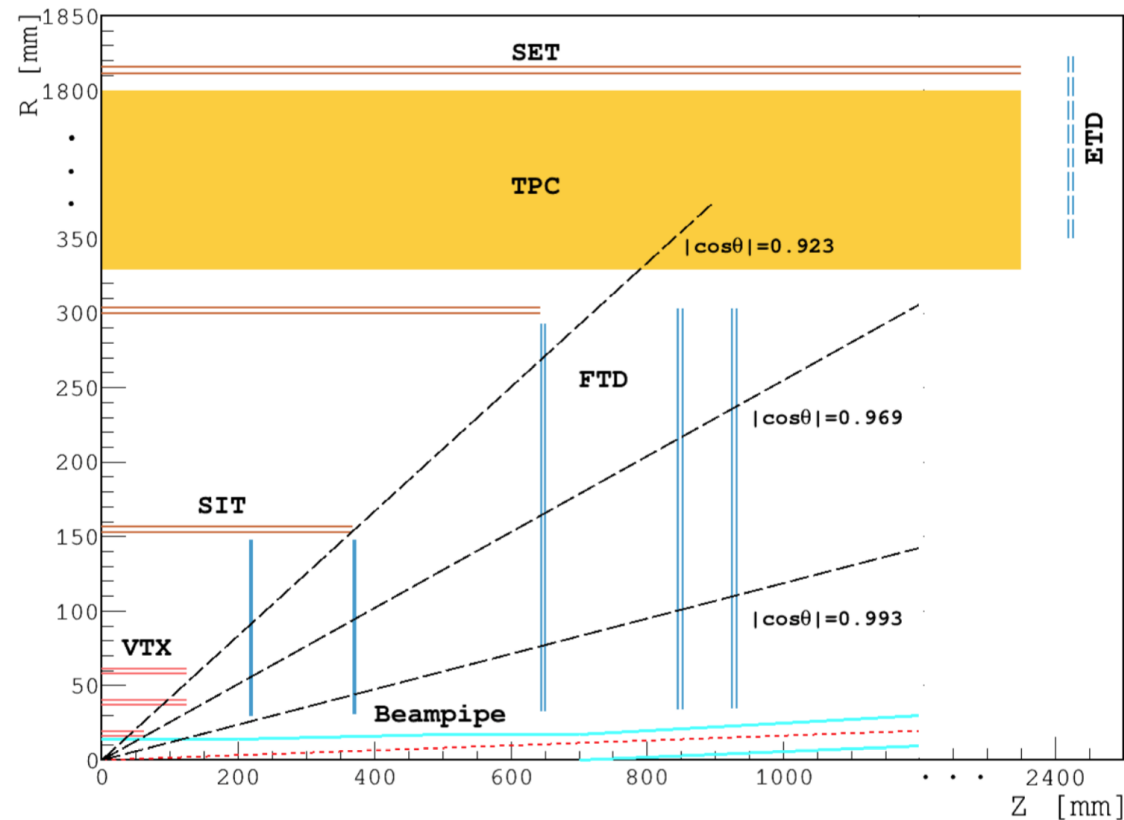
<https://indico.ihep.ac.cn/event/9960/session/13/contribution/231/material/slides/0.pdf>

In this talk:

1. Introduction
2. Sensor: ATLASPix3
3. Flex, Modules and Staves
4. Readout Systems
5. Conclusions and summary

CEPC tracker designs: TPC/Si

Baseline tracker design: TPC
and 3 layers / 5 disks of silicon sensors,
50 m² (33 w/o ETD) if built in CMOS pixels



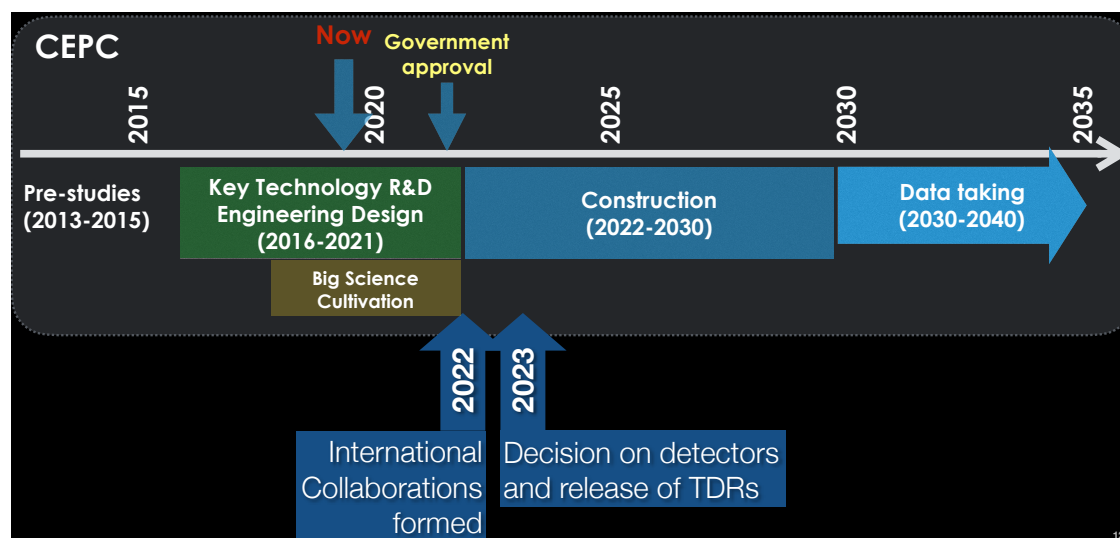
Resolution / multiple scattering requirement:

Single layer of thin **silicon pixel** preferred
(strips require thick double layers)

Tight schedule: Use/adapt an **existing solution**

there is little time for a custom solution from scratch

Financial constraint: Use an industrial process where possible (**CMOS**)



Comparison:

25ns bunch spacing (Z-mode): same for ATLAS

O(100 m²) of silicon tracker: comparable for the ATLAS ITK
(8.8+4.4 m² pixel, 105+165 m² strips for barrel/disk)

pitch/resolution: 50 μ m in ϕ

ALICE ITS: 29 μ m x 27 μ m monolithic CMOS

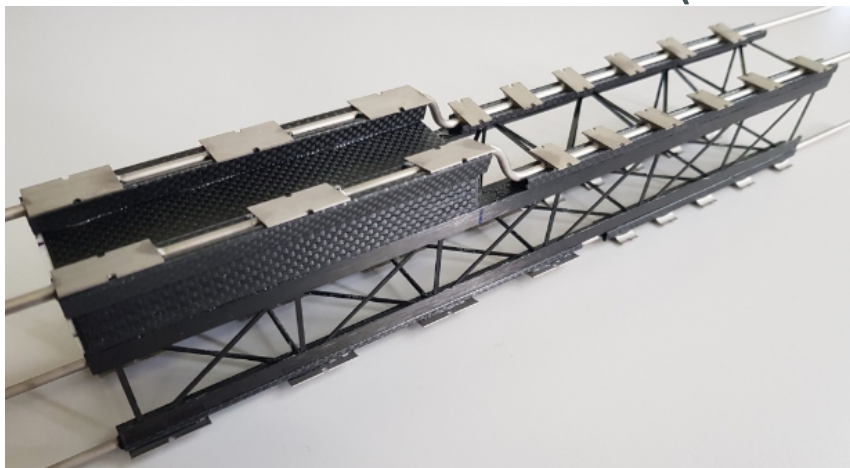
ATLAS ITK Pixel CMOS: < 50 μ m x 150 μ m

material budget for tracker layers:

0.65% (TPC/Si)/~1% (Full Si) X/X_0 / layer

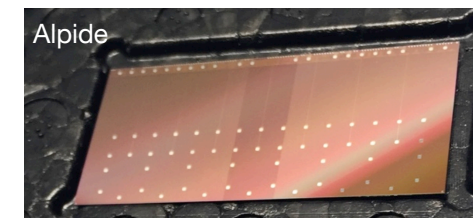
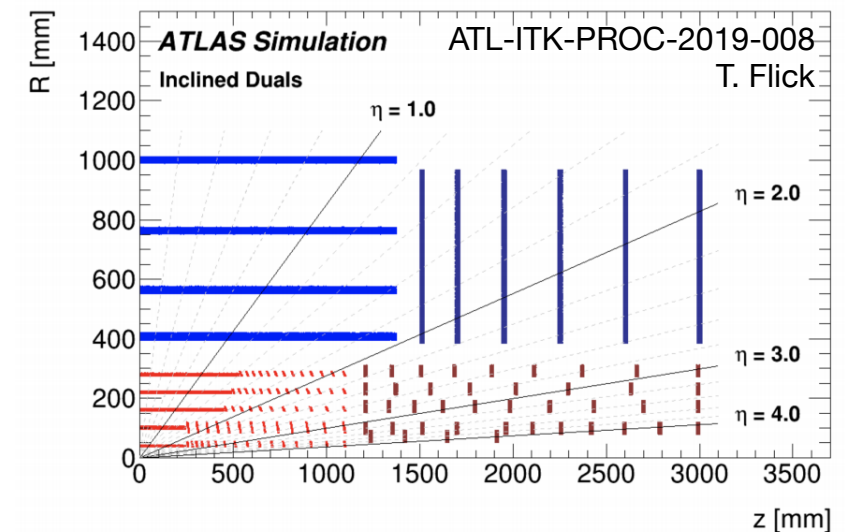
ALICE: 0.8%/layer outer barrel staves

ATLAS: ITK Pixel <1 X_0 total (standard hybrid)

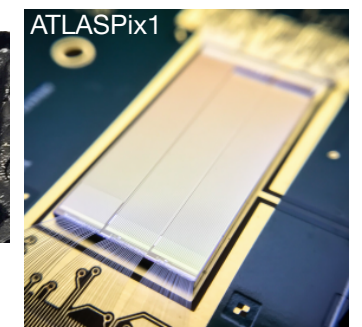


<https://www.unige.ch/dpnc/en/groups/giuseppe-iacobucci/research/slim-mechanics/>

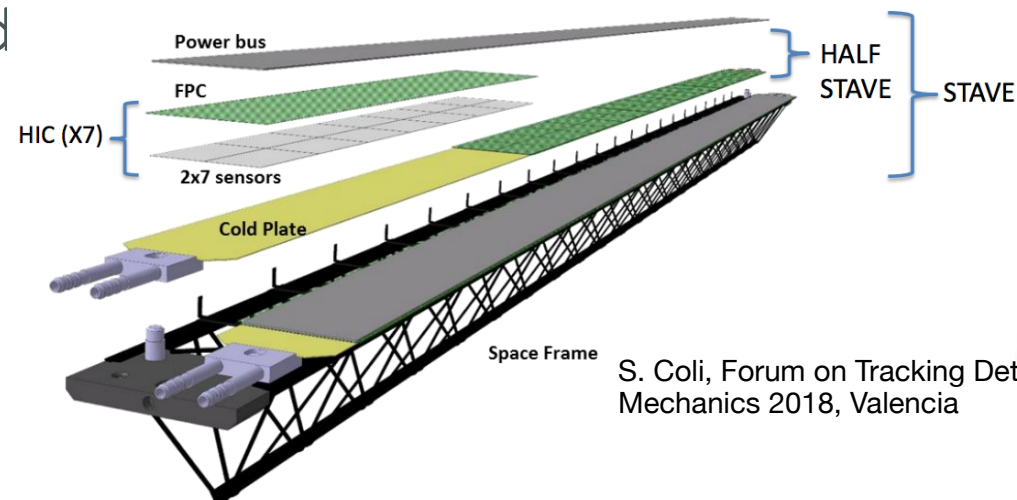
H. Fox



L. Musa, ECFA HL-LHC workshop



H. Augustin eg. al.,
Uni Heidelberg



S. Coli, Forum on Tracking Detector
Mechanics 2018, Valencia

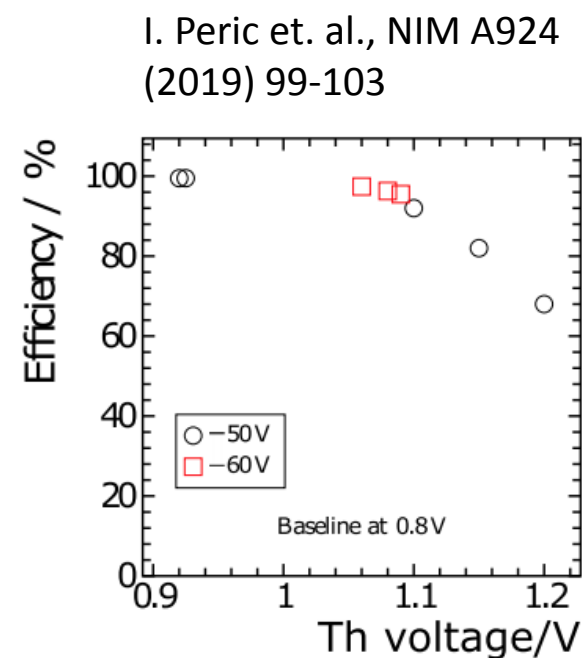
Sensor proposal: ATLASPix

ATLASPix is a CMOS sensor developed to fulfil the requirements for the ATLAS upgrade

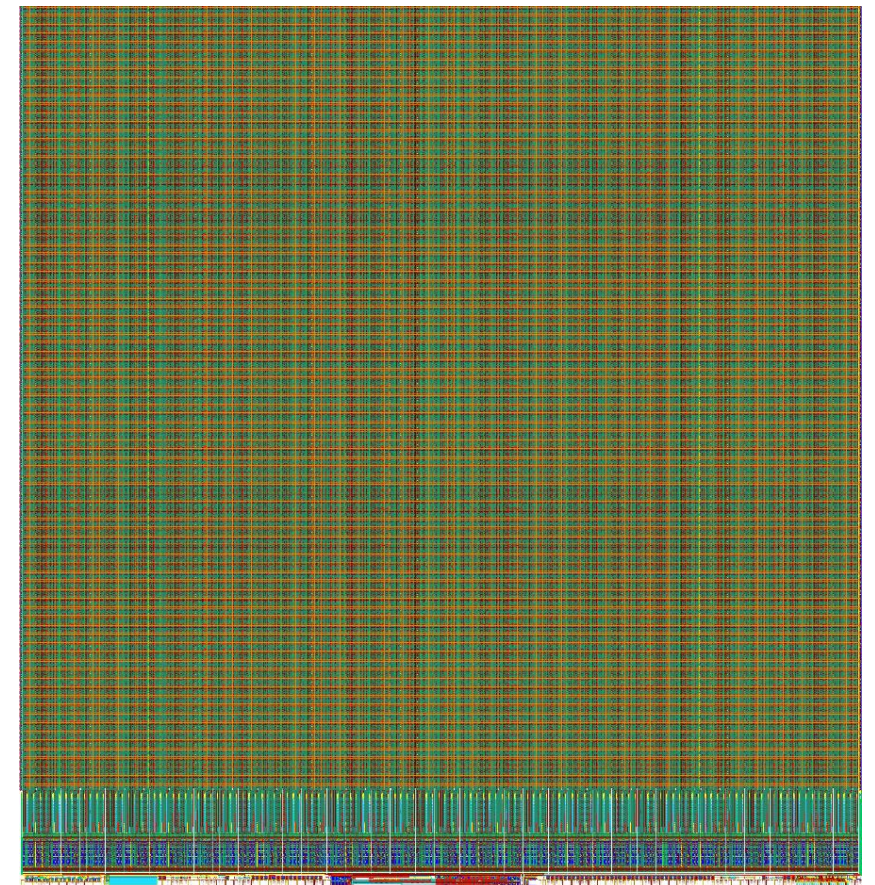
- Not strictly an ATLAS development
- **Monolithic CMOS** allows to produce **large** areas **fast** and **cheap**
- No hybridisation – wirebonds or C4NP bumps possible
- **25ns timing** compliant
- Hit efficiency 99.5% (ATLASPix1)
- Pixel size **150 μm by 50 μm** (or smaller)
- Triggered or triggerless readout possible
- 1.28 GBit/s downlink

ATLASPix3

- Reticule size: **2.02 cm by 2.1 cm**
- Full-size sensor, ATLASPix3 (TSI, 200 Ωcm , 180nm) **available**
- 132 columns with 150 μm pixel
- One column contains 372 pixels, a configuration register block, 372 hit buffers, 80 trigger buffers and two **end of column (EoC) blocks**. EoC1 is attached to hit buffers and EoC2 to trigger buffers.



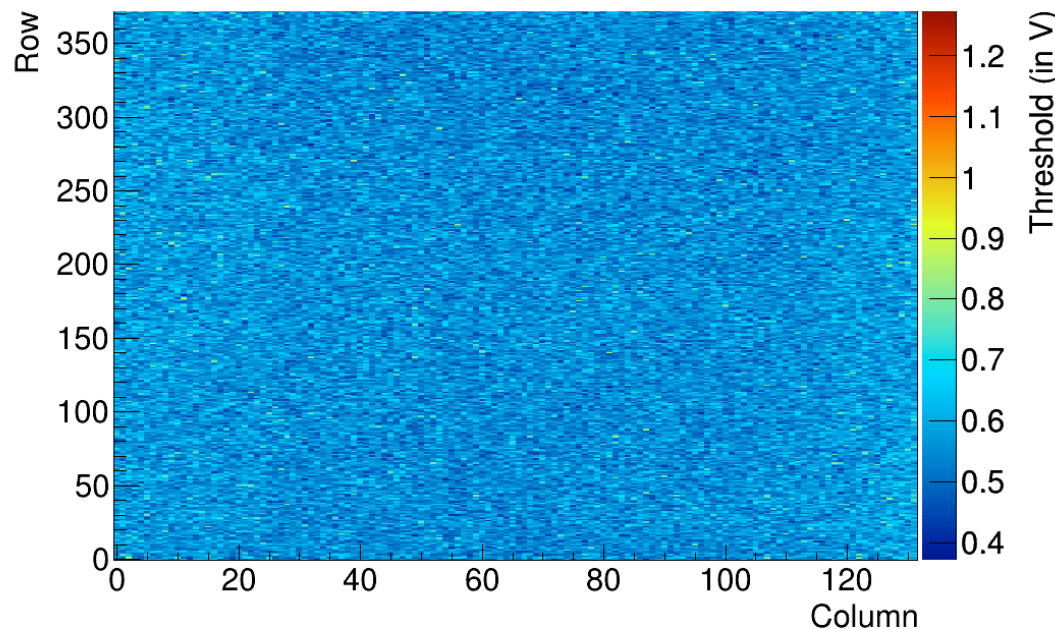
ATLASPix3



Sensor: Tuning of Pixel Matrix

Threshold map,
untuned sensor

**All 49104
pixels work !**



Each pixel contains a **3 bit tuning DAC (TDAC)** and a disable bit

Writing of the pixel memories is working and the detection **threshold changes linearly** with the TDAC setting

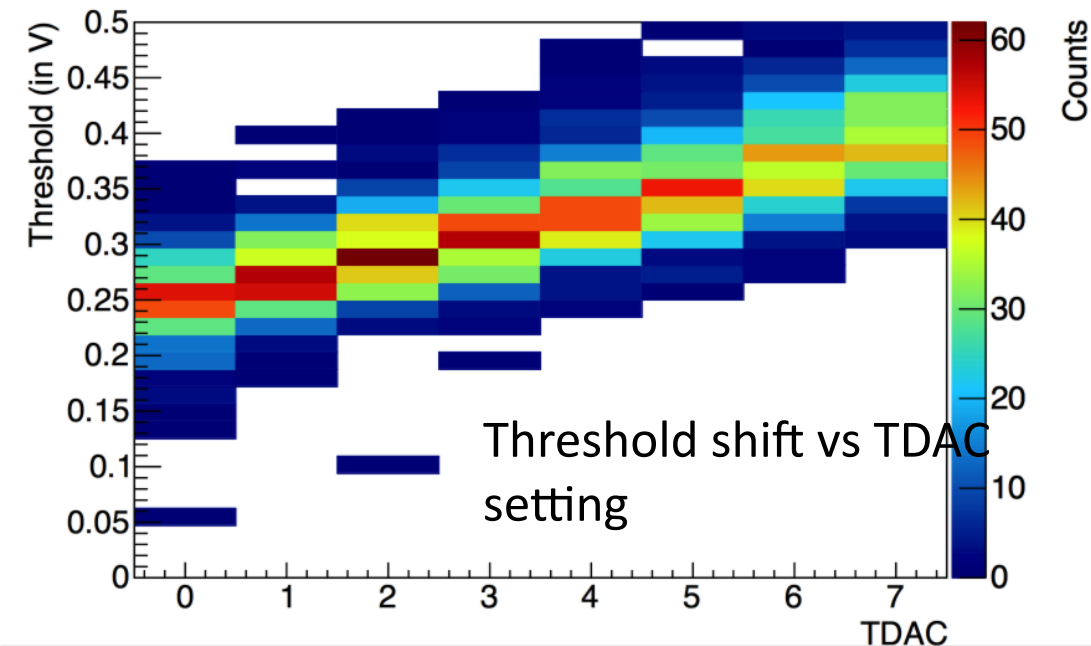
Threshold tuning:

Detection thresholds are adjusted to **$\mu+3\sigma$ of untuned** distribution

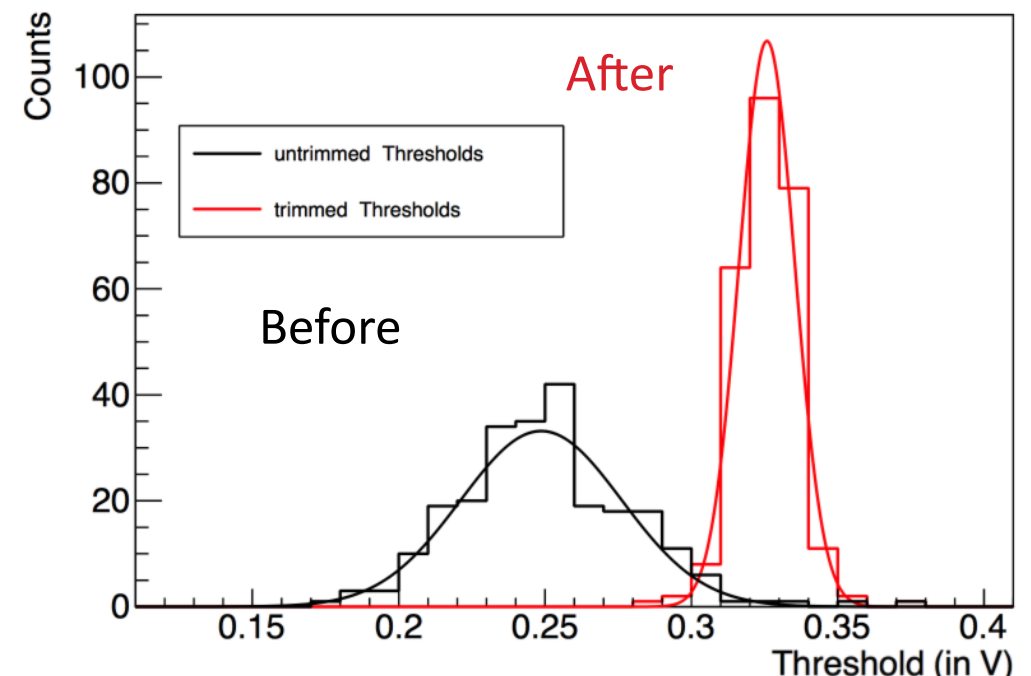
Subset: conducted for 2 rows (in total 264 pixels):

Distribution width $\sim 3\times$ smaller

$$\sigma_{\text{trimmed}} = 9.5\text{mV} \leftrightarrow \sim 50 e^-$$

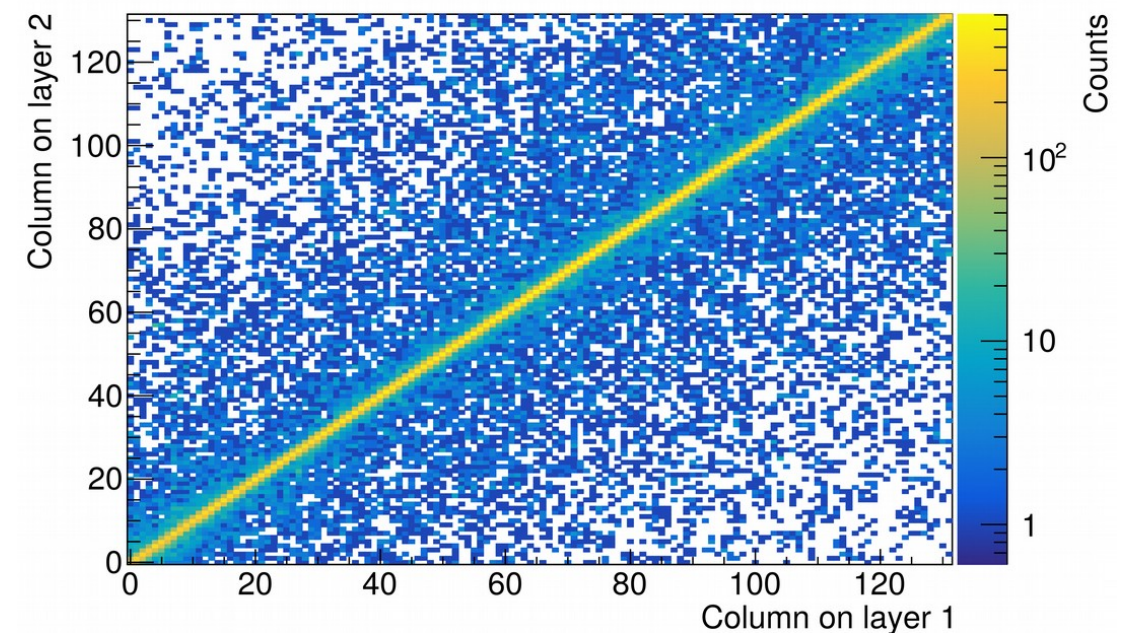
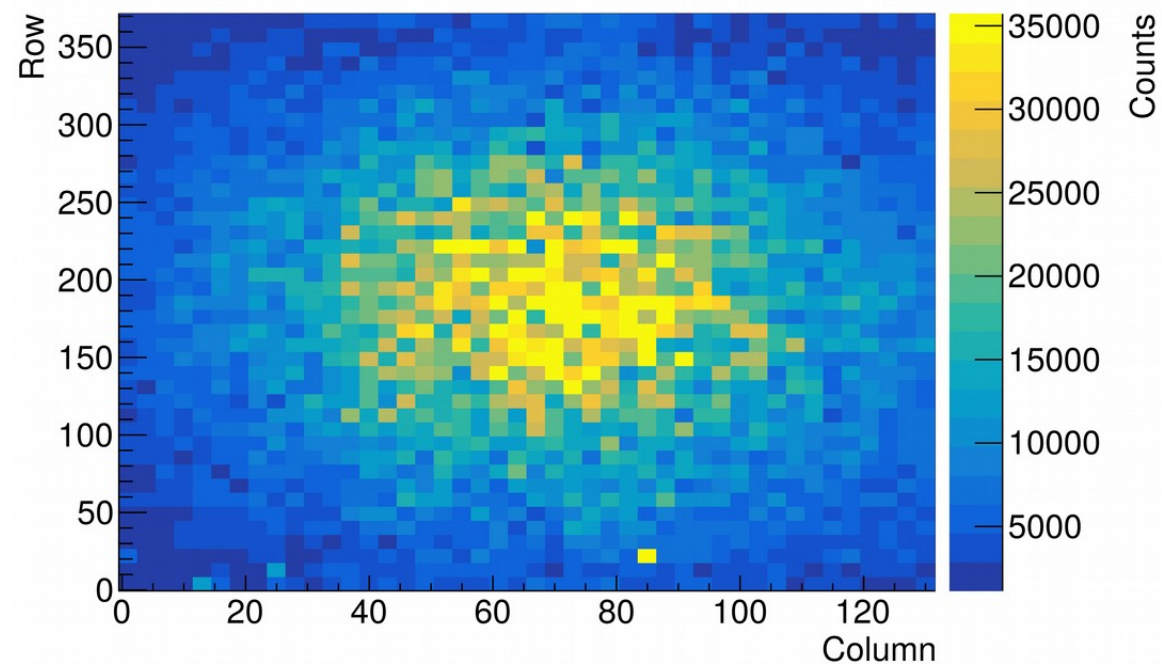


Pixel Trimming

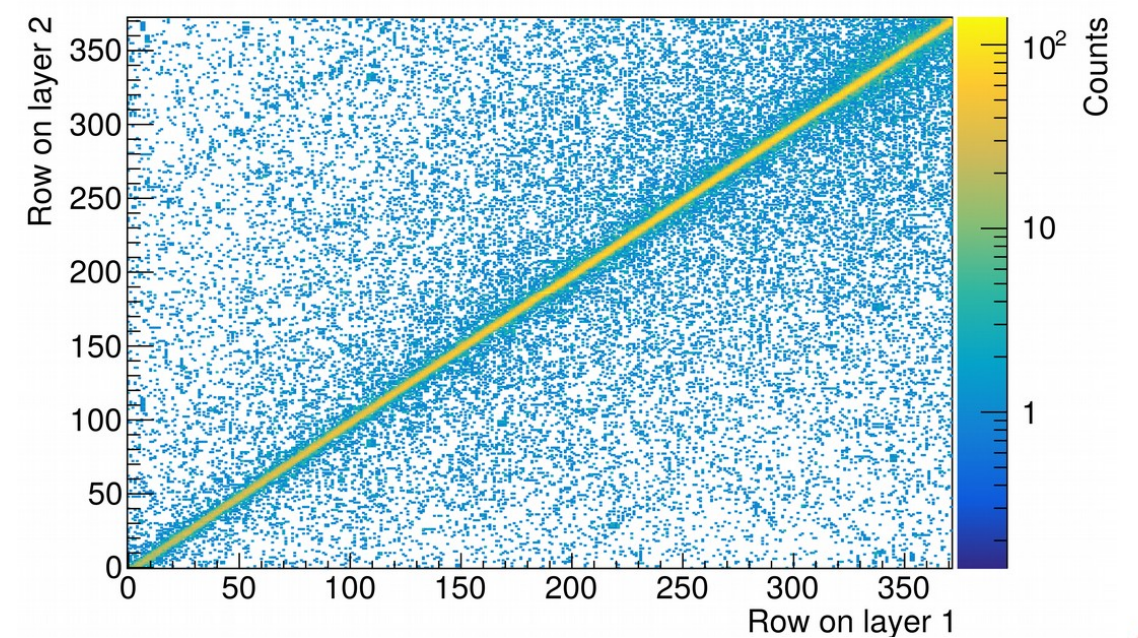
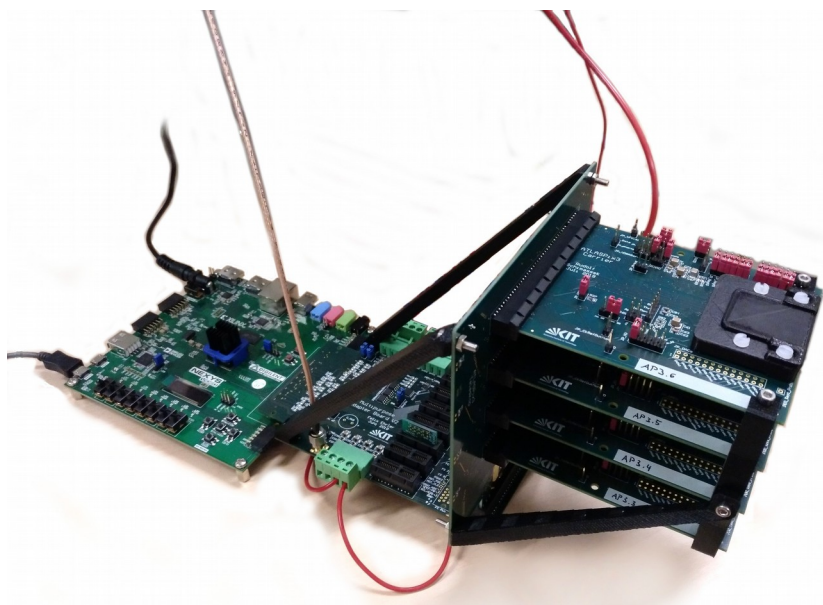


Sensor: Signal Detection

A **^{55}Fe source** was held over the ATLASPix3 sensor:

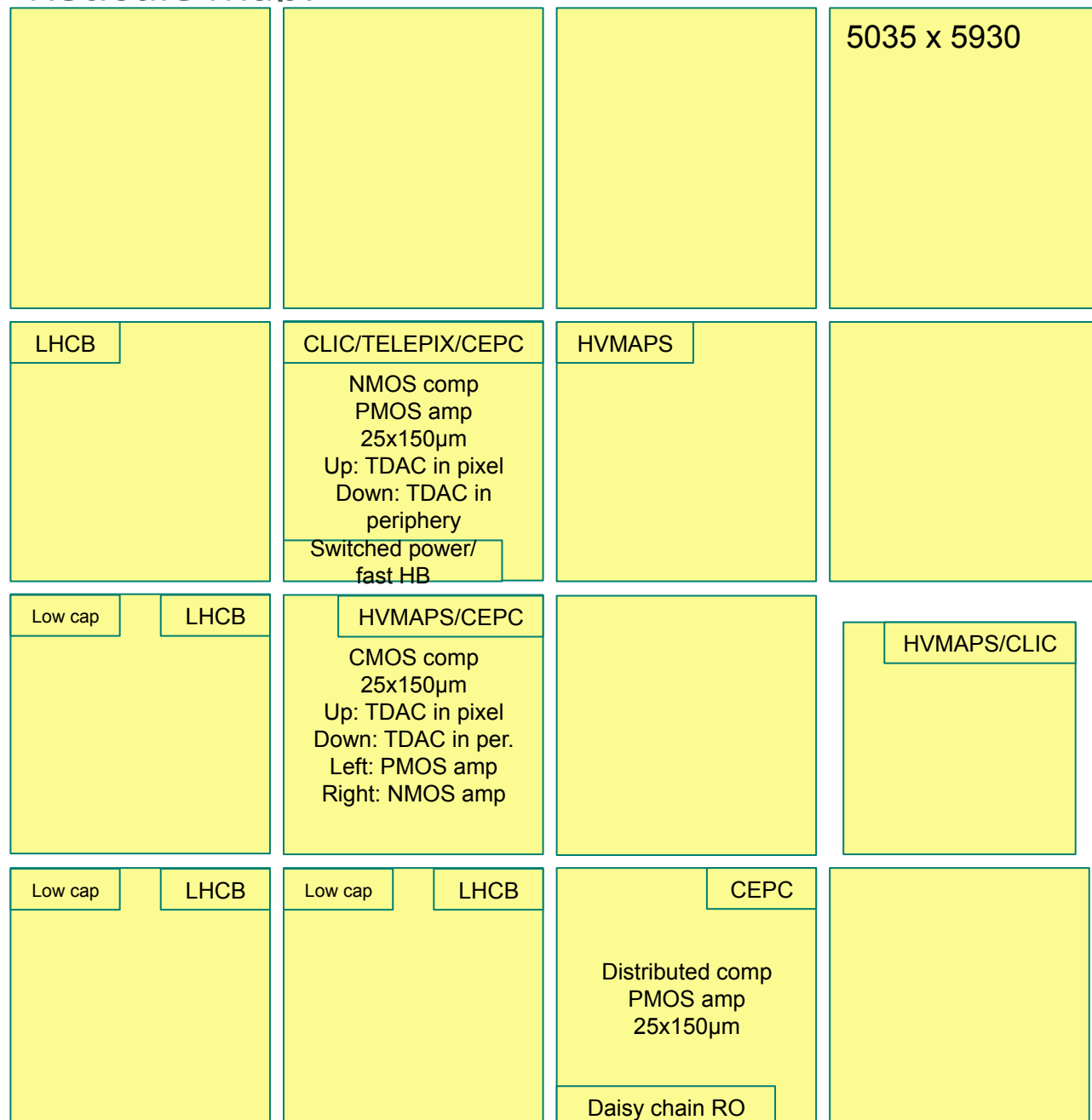


Four layer **telescope** at DESY testbeam:



Engineering run planned for April this year(?)

Reticule map:



Collaboration with **LHCb Mighty Tracker** and other projects.

CEPC institutes make a **significant contribution** to the cost of the submission.

Test evolvement of ATLASPix3:

Smaller pixel size (**25µm**) in ϕ direction

Lower capacitance

Amplifier and comparator design

Electronics in **pixel or periphery**

Daisy chain of readout

Looking at processes with Chinese vendors **HHGrace**, Non disclosure agreement in preparation.

SMIC; talk to agency. 40nm and 55nm processes very interesting.

Flex: Milano Design for a Quad Module



ATLASPix3 Flex V1.0

Title ATLASPix3 Flex		Istituto Nazionale di Fisica Nucleare Via G. Celoria, 16 20139 Milano ITALY	
Size: A3		Revision: 1.0	
Date: 04/12/2019		Sheet 1 of 6	
Author: F. Sabatini	Email: fabrizio.sabatini@mi.infn.it	Tel: +390250317390	



Chip #1

Page 1 Main

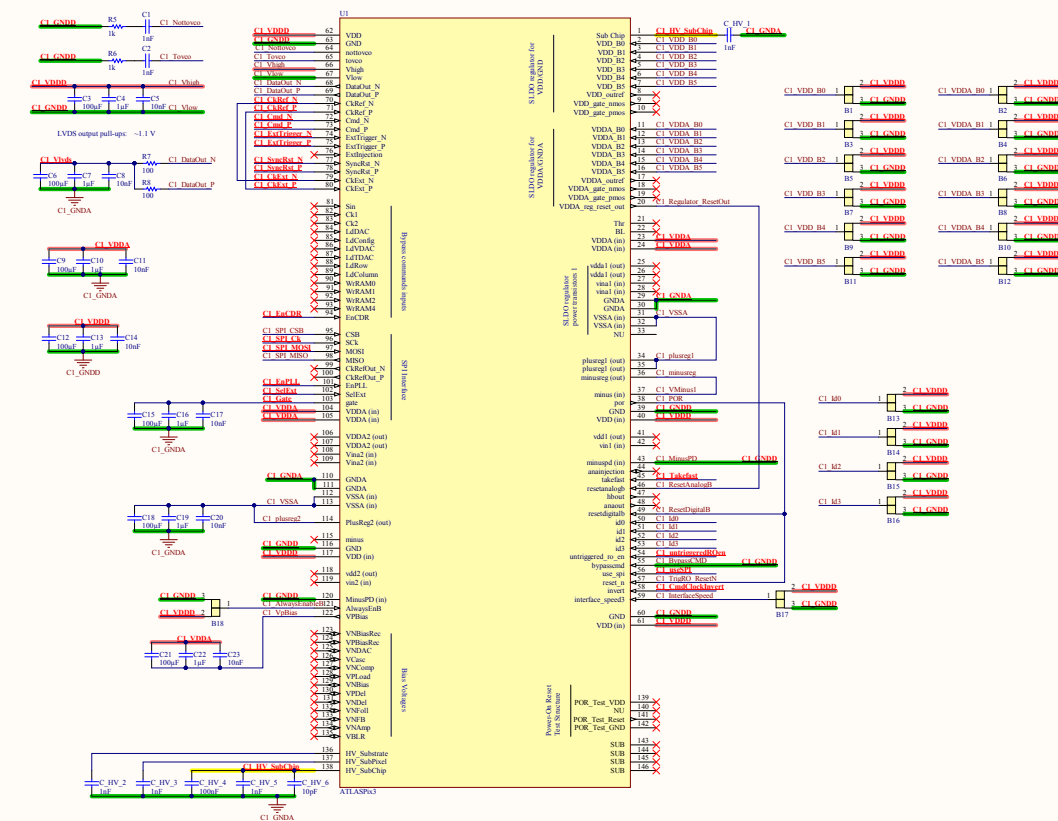
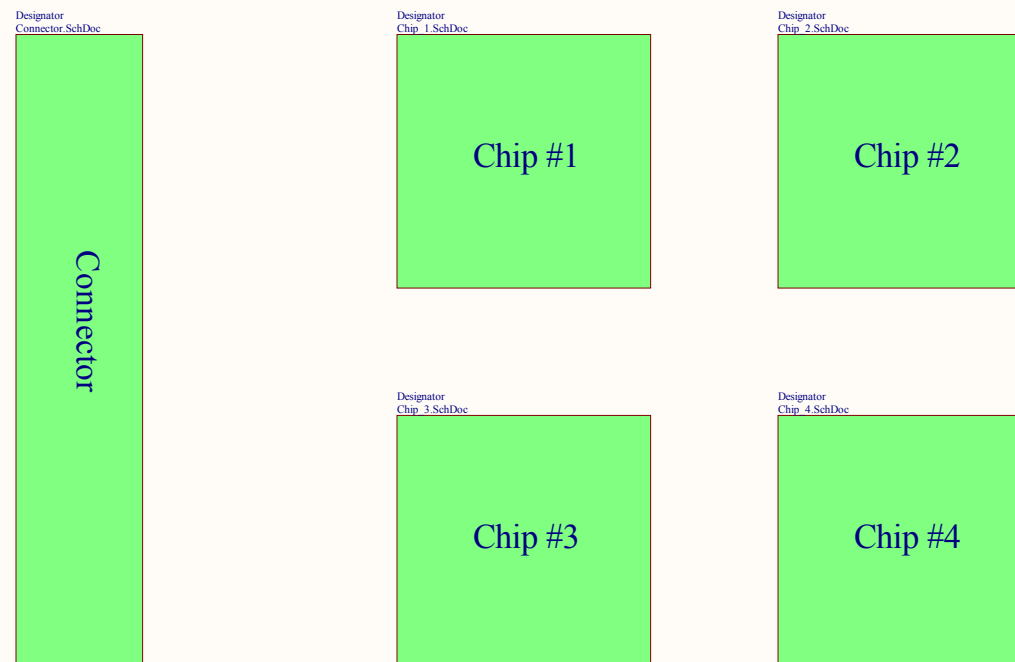
Page 2 Connector

Page 3 Chip #1

Page 4 Chip #2

Page 5 Chip #3

Page 6 Chip #4



Fully functional design for readout.

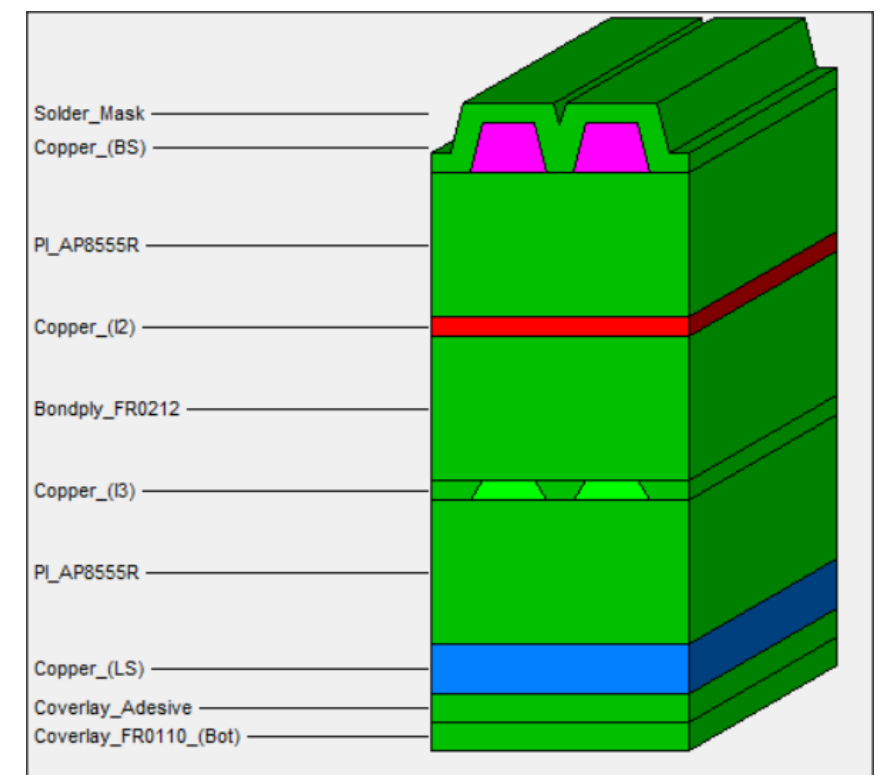
KISS (Keep It Simple and Safe) for first attempt:

Direct powering

Not optimised for low material

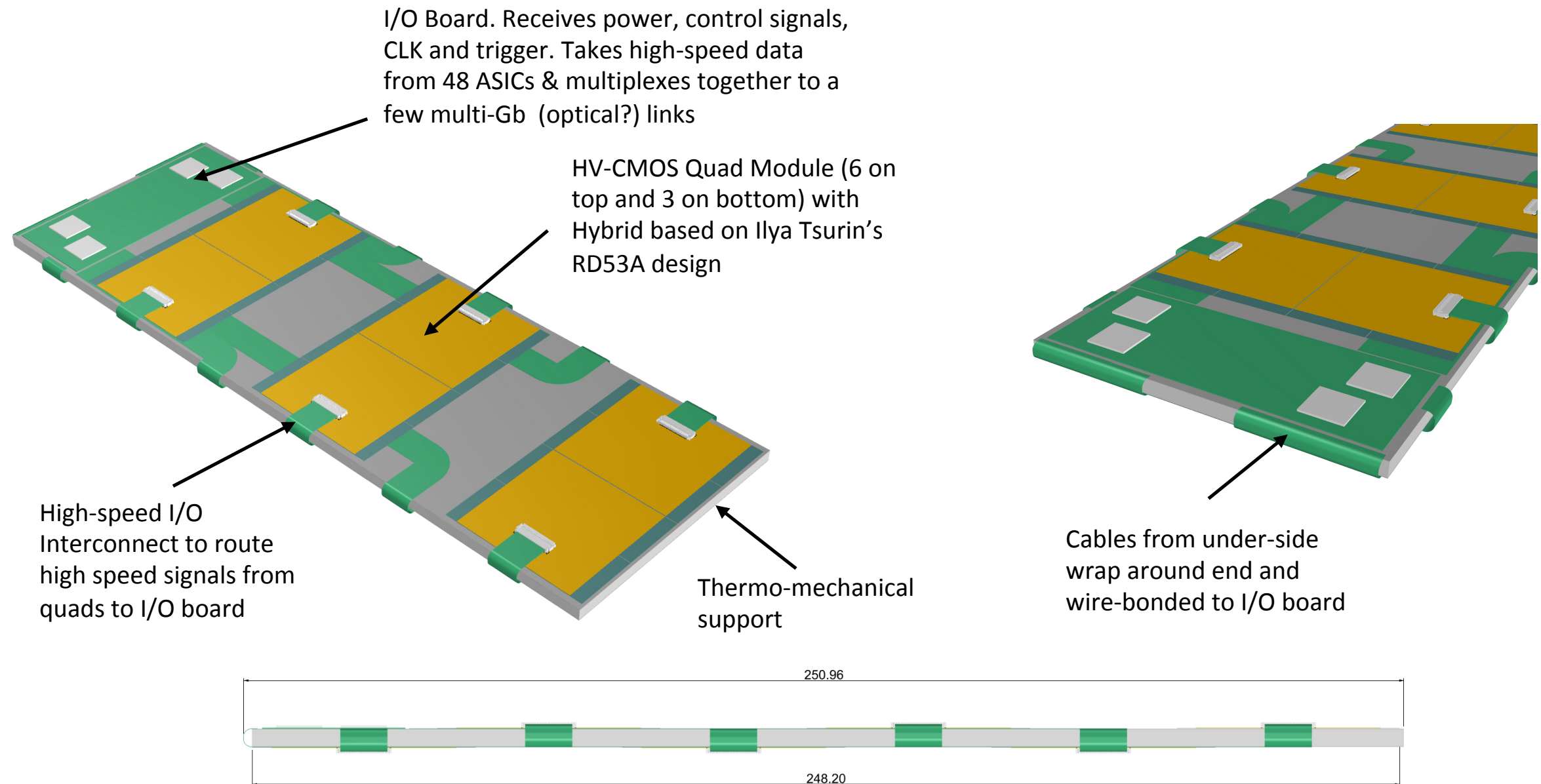
Reduced configuration parameters

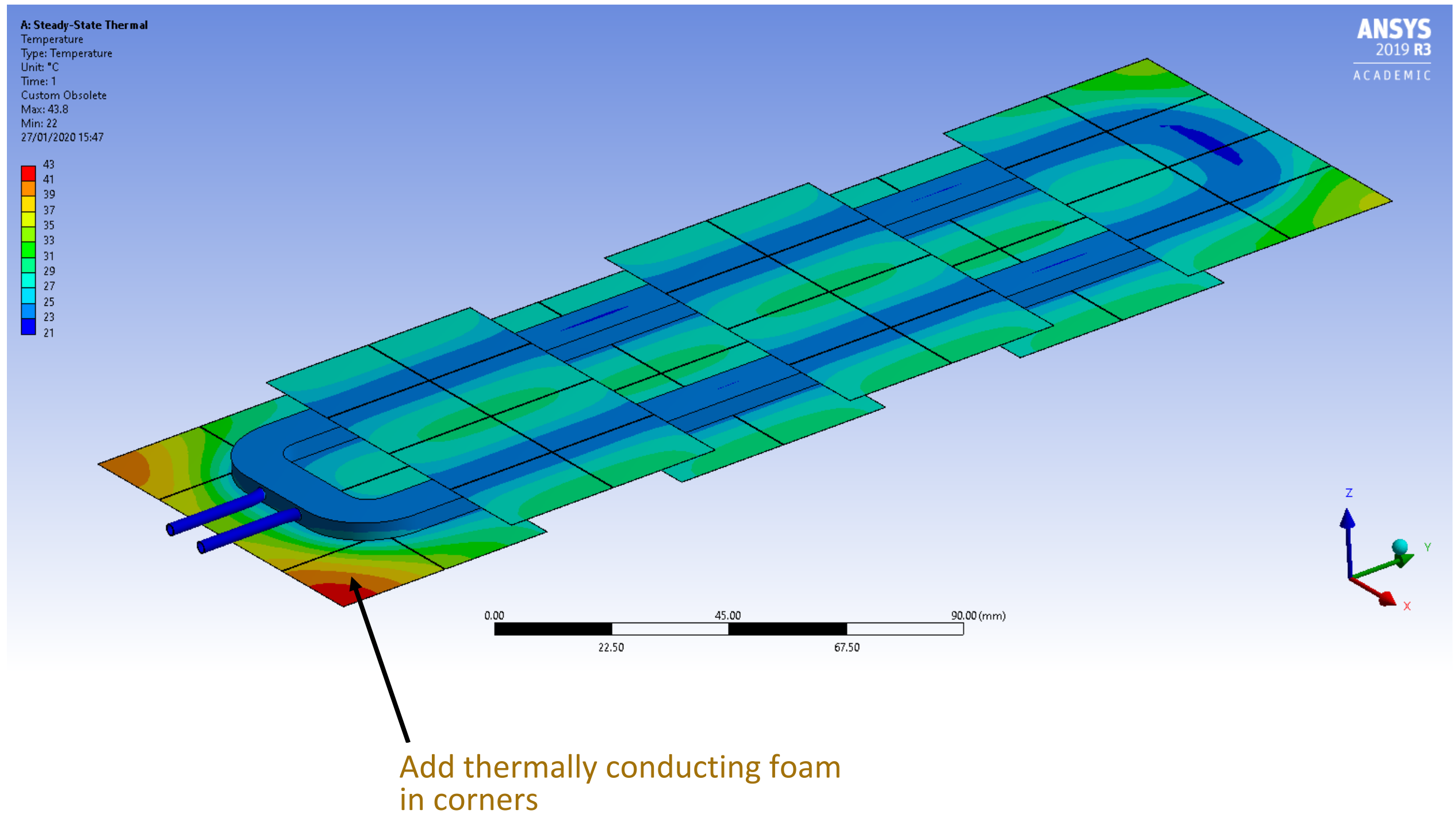
Look at **serial powering** in parallel





Tile Conceptual Design





Stave: ATLAS Pixel Carbon Fibre Support Structure

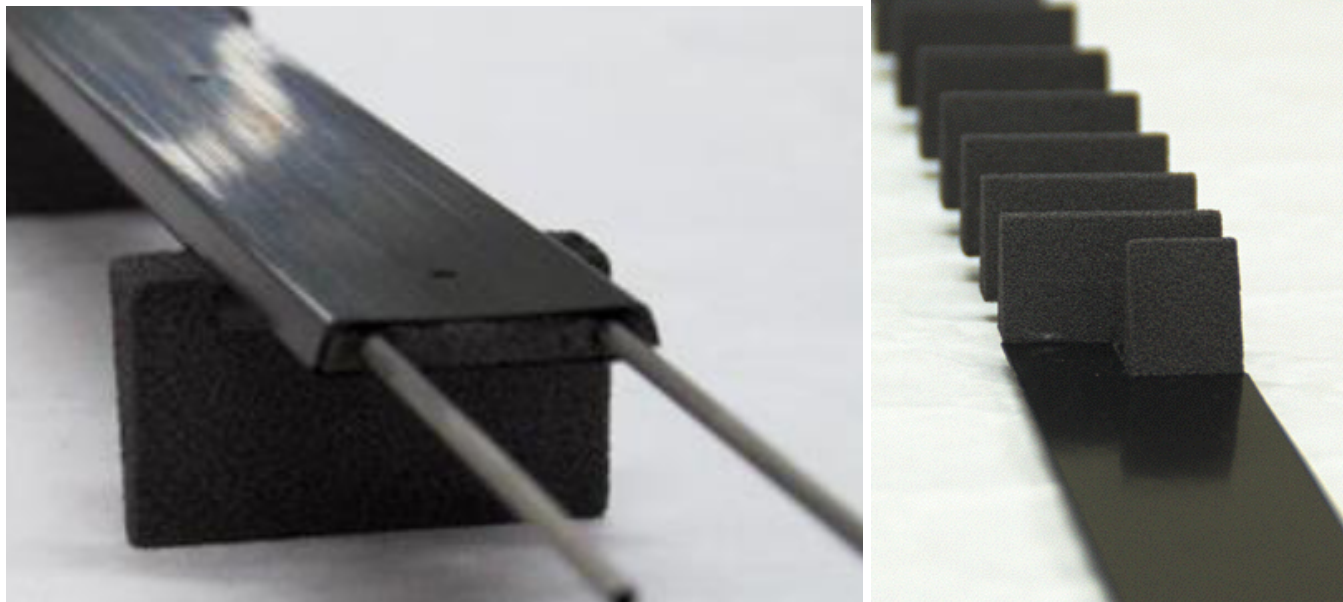
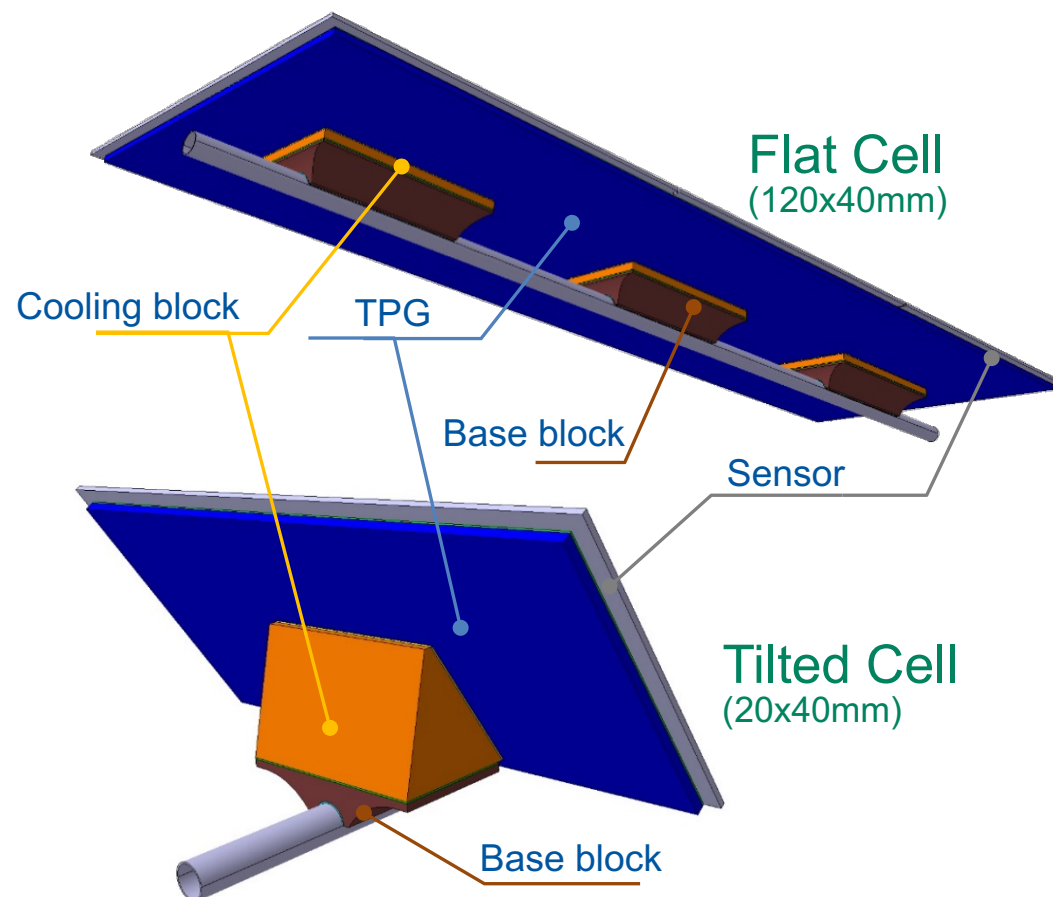
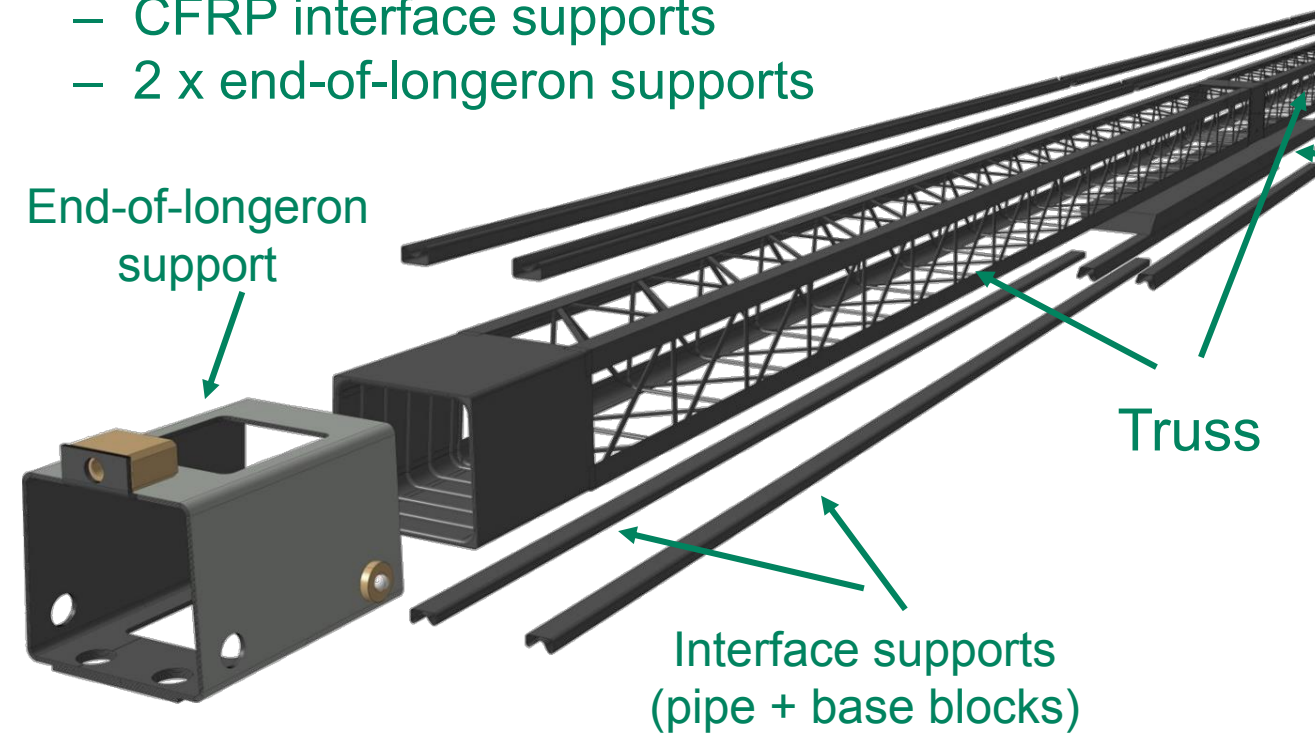


Figure 15.19: ALPINE design for the inclined layout.

- 2 x TRUSS + Central sandwich step
- CFRP interface supports
- 2 x end-of-longeron supports



Layer	TFM ($\text{K}\cdot\text{cm}^2\cdot\text{W}^{-1}$)		
	Conductive	Convective	Global
0	11	4.3	15
1	16	8.6	25
2	12	8.6	21
3	15	8.6	24
4	18	8.6	27

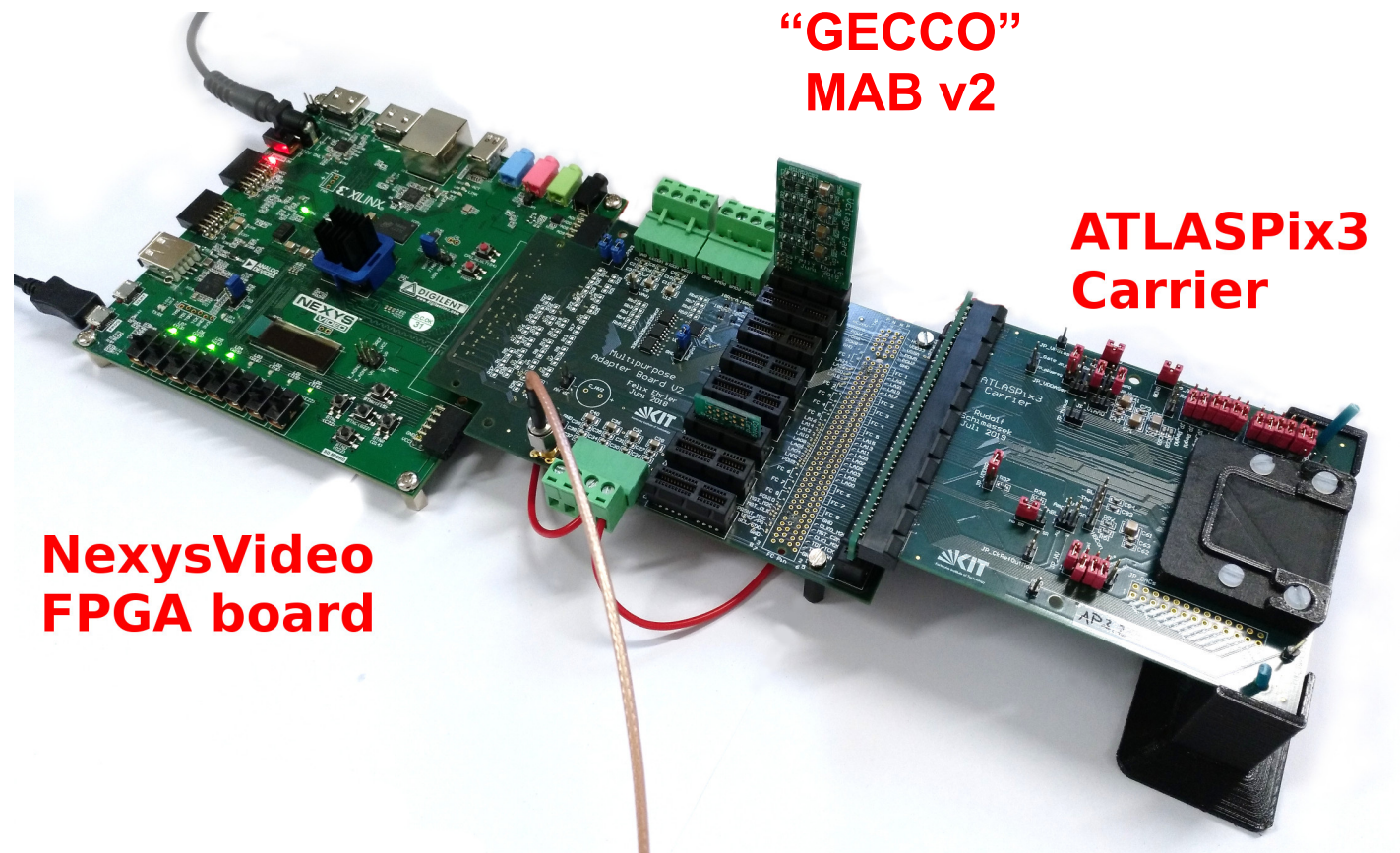
We are in contact with a Beijing company for production of staves.

D. GIUGNI



Readout Systems: KIT single chip board

Starting point is the **ATLASPix3 single-chip card** produced by KIT and used for the tests



Gerber files for GECCO and function cards are available. Looking for a vendor (in China) for **production of more readout systems.**



DAQ: YARR

Yet Another Rapid Readout

<https://iopscience.iop.org/article/10.1088/1742-6596/898/3/032053>

YARR is a small **self-contained DAQ system**.

Linux PC with a x4 **PCIe slot for the FPGA card**

FPGA card: e.g. **Trenz TEF1001**, XpressK7,...

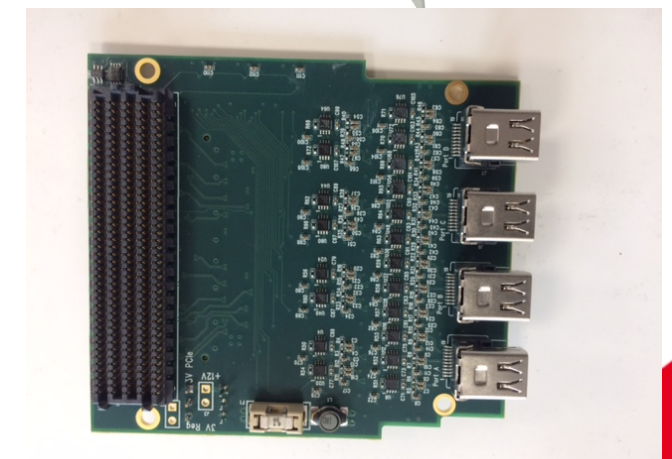
FMC cards for FE-I4 and RD53A

Up to **1.6GBit/s possible** with this setup.

We have used the YARR readout with a digital RD53A module in **Lancaster & Edinburgh**.

Todo: Adaptation to ATLASPix3 necessary:

- **FMC**
- **Software**



CaRIBou Readout System

UniGe+BNL development

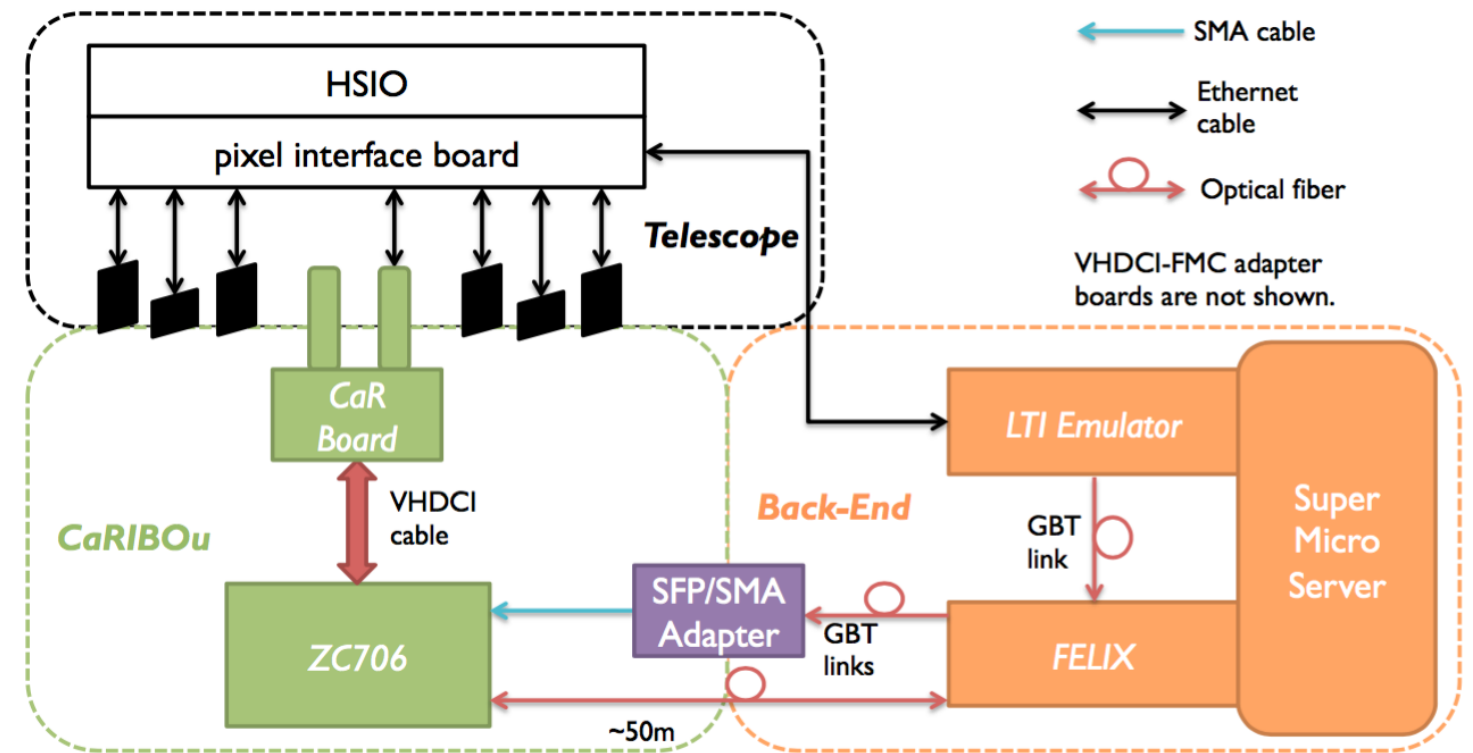
ZC706 + CaR-board based

ATLASPix3 is implemented,

Continued support thus unclear

Comparatively expensive (~4kEUR)

Integrates with **FELIX**



Mathieu Beliot, AMSH18 results

Currently an **order for more** (and slightly updated) **CaR**-boards is prepared by CERN.

4 CaR boards have been requested for us.

A long-term major redesign of CaRIBou is underway, with the goal of replacing the (comparatively expensive) KC706 board.

Summary and Conclusion

Sensor:

Functional ATLASPix3 sensor available for prototyping

Optimisation for a (Chinese) e^+e^- collider

- Power consumption
- Investigate and work with Chinese foundry

Readout:

Flex design well progressed

Follow up with all three alternatives.

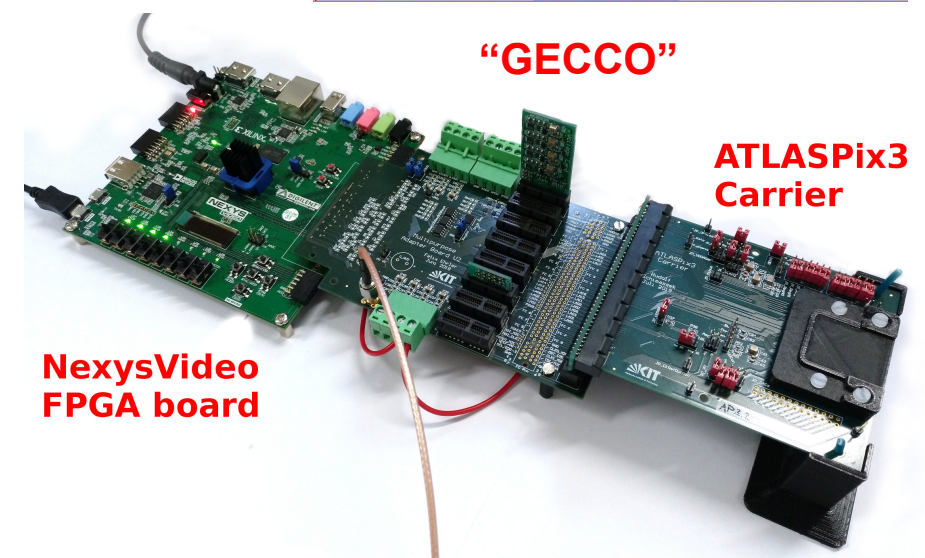
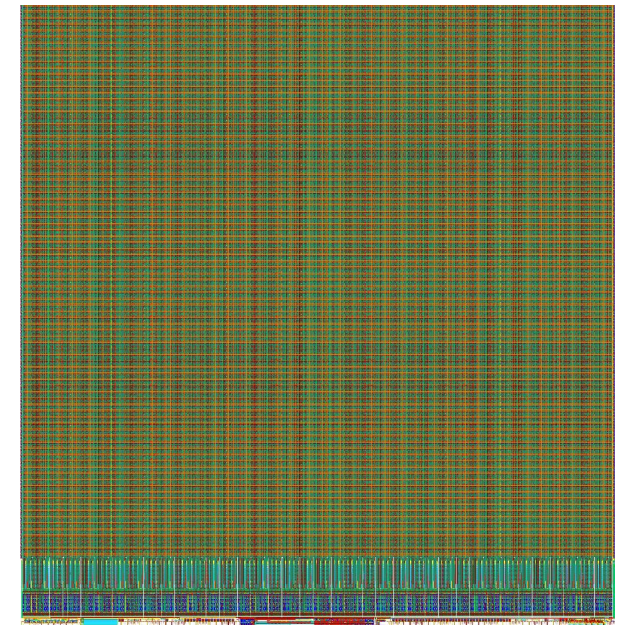
Distributions of readout systems to interested institutes

Staves:

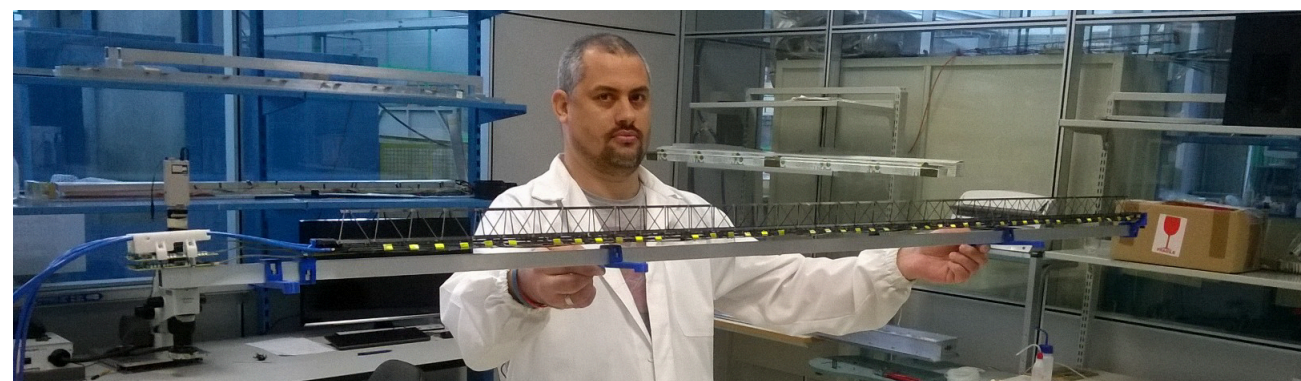
Experience with ALICE (and ATLAS) module staves

We need a new stave design for the ATLASPix modules, geometry and material requirements

We have approached a local (Beijing) company to design & fabricate the **truss supporting structure with carbon fibre**

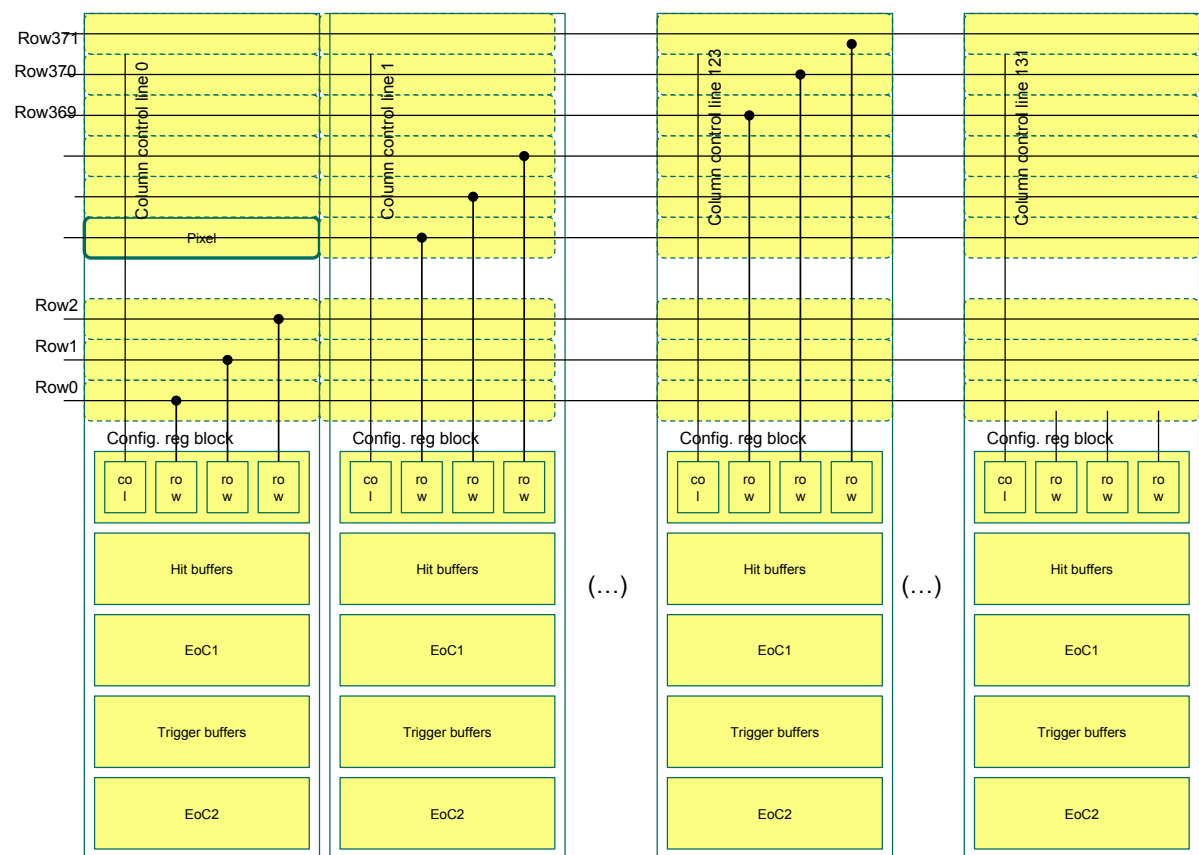


ALICE stave at Daresbury

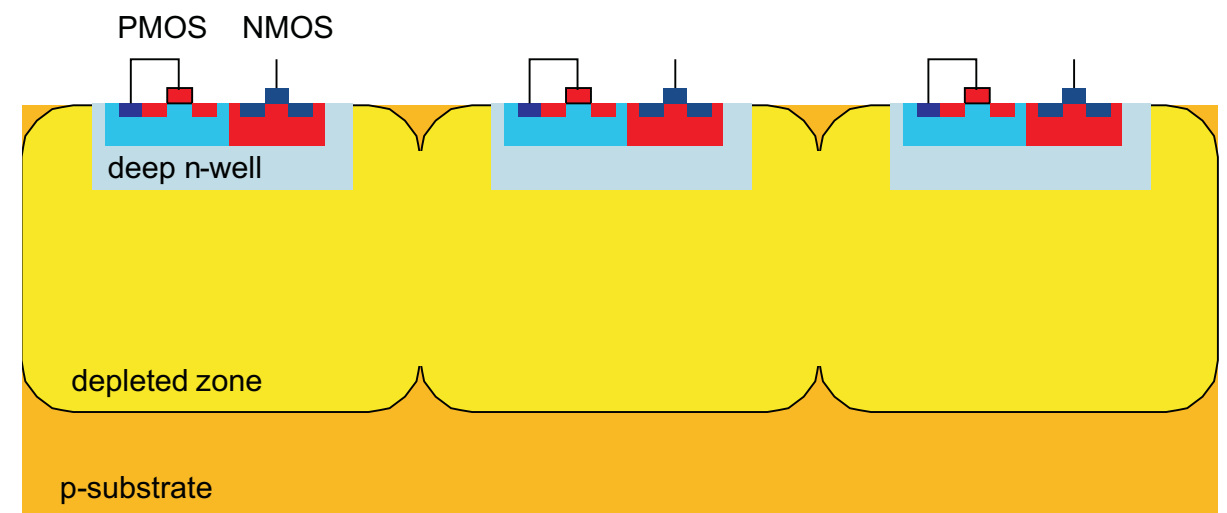


Backup

Block scheme of the pixel matrix and column circuits



HV-CMOS structure



Pixel Schematics

