Post layout simulation of Digital Pixels of TaiChuPix2

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Simulation of power density
(Schematic level/ Martrix:512x1024)

Simulation condition: Both of schemes are based on pull up transistors, without latch part.

Average Power	FEI3 upgrade	ALPIDE upgrade
Initialization phase	161.366uA	211.13uA
Readout phase(max)	271.516uA	353.08uA
Static phase	47.4nA	3.43uA
Average current (every 8.3us)	8.786uA	12.846uA
Power density during readout phase	76.36mW/cm2	99.303mW/cm2
Power density average	2.46mW/cm2	3.61mW/cm2

Calculation of Power density:

Power density(FE-I3)= 271.516uA*1.8V / (512x25umx50um) =76.36mW/cm2

Simulation of power density

(Post layout / Martrix:64x192)

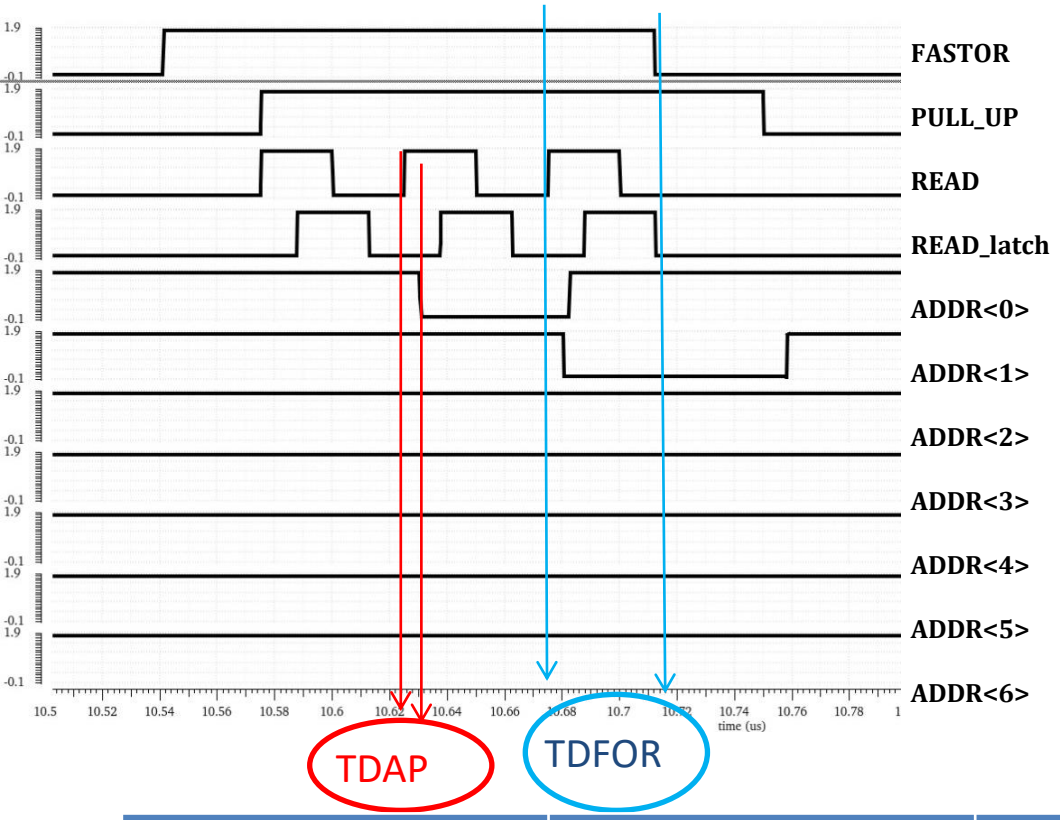
Simulation condition: Both of schemes are based on pull up transistors, with latch part.

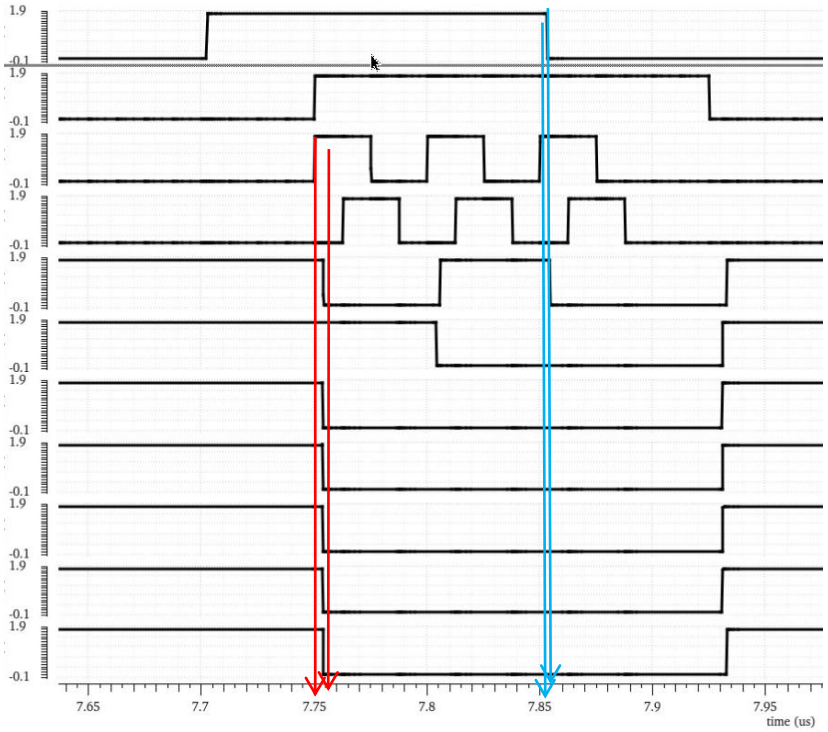
Average Power	FEI3 upgrade	ALPIDE upgrade
Initialization phase	58.53uA	52.73uA
Readout phase(max)	69.19uA	79.38uA
Static phase	120 nA	670 nA
Average current (every 8.3us)	2.262uA	14.21 uA
Power density during readout phase	155.68mW/cm2	178.60mW/cm2
Power density average	5.09mW/cm2	32.06mW/cm2

Calculation of Power density:

Power density(FE-I3)= 69.19uA*1.8V / (64x25umx50um) =155.68mW/cm2

Post Simulation of FE-I3 like V1





	TT 27℃ 1.8V	SS 50℃ 1.6V
TDAPmax	5.45ns	9.10ns
TDAPmin	3.93ns	6.55ns
TDFORmax	37.15ns	17.46ns
TDFORmin	3.17ns	5.60ns

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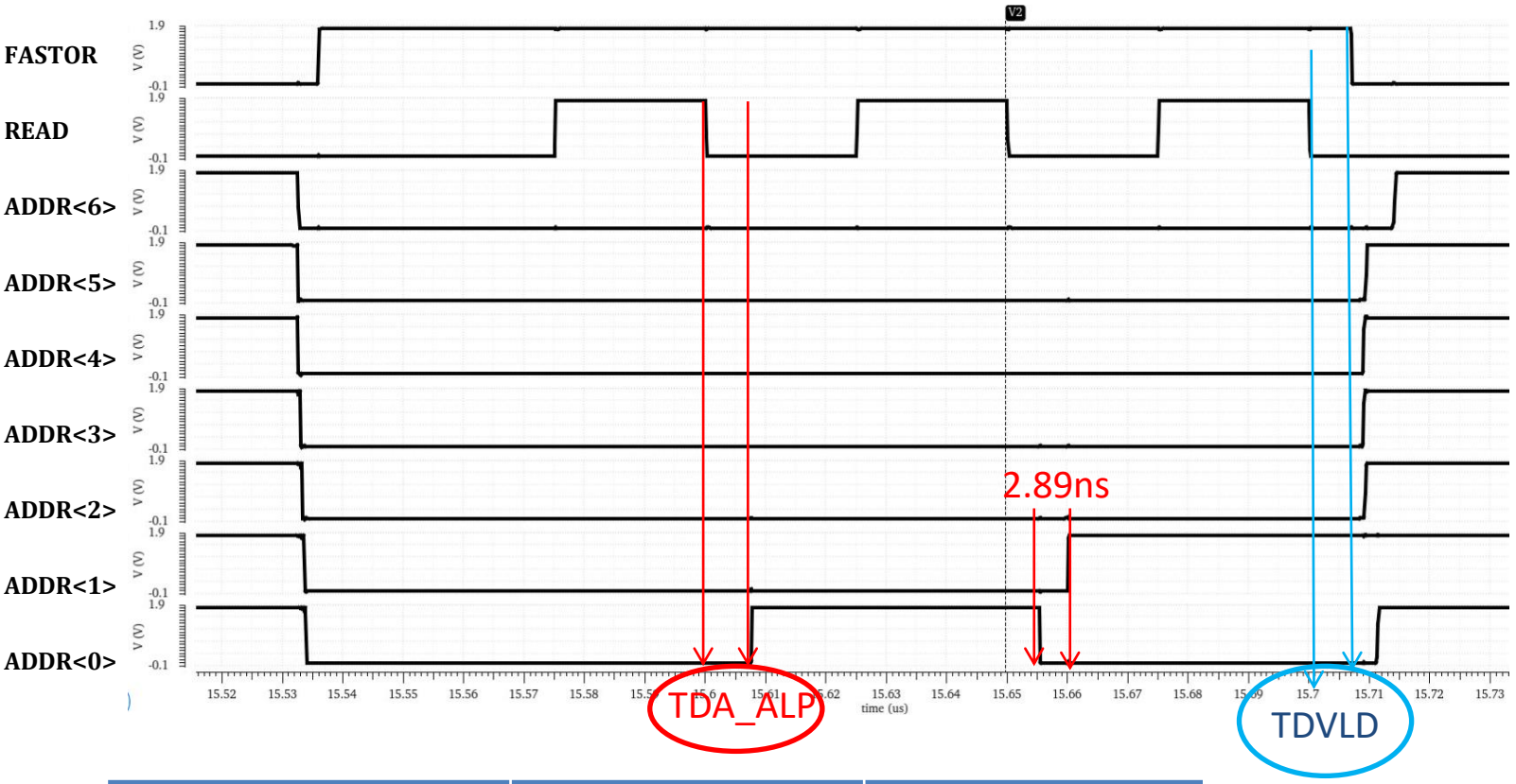
Post Simulation of ALPIDE like



	TT 27℃ 1.8V	SS 50℃ 1.6V
TDA_ALPmax	7.40ns +4.64n	14.21ns+5.89n
TDA_ALPmin	5.25ns +2.89n	8.01ns+10.86n
TDVLDmax	7.16ns	12ns
TDVLDmin	6.82ns	10.97ns

RED value is the difference between ADDR<1> and ADDR<0>

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Thanks for your attention.

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