Status of CEPC DHCAL

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CEPC Day
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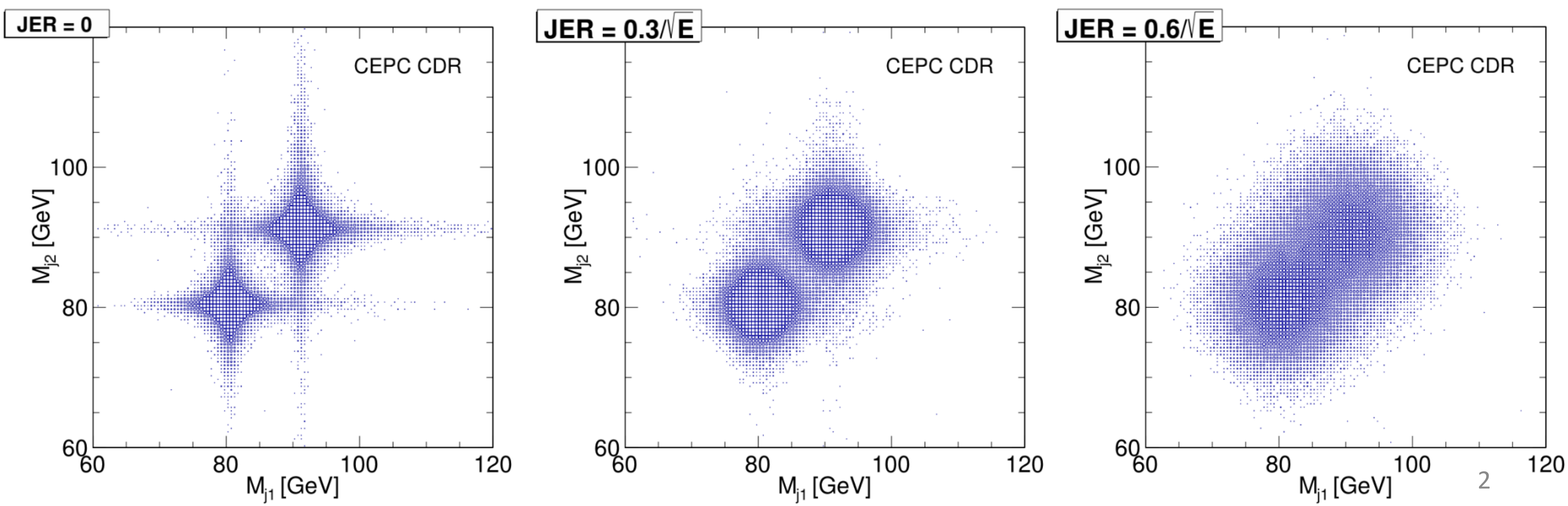
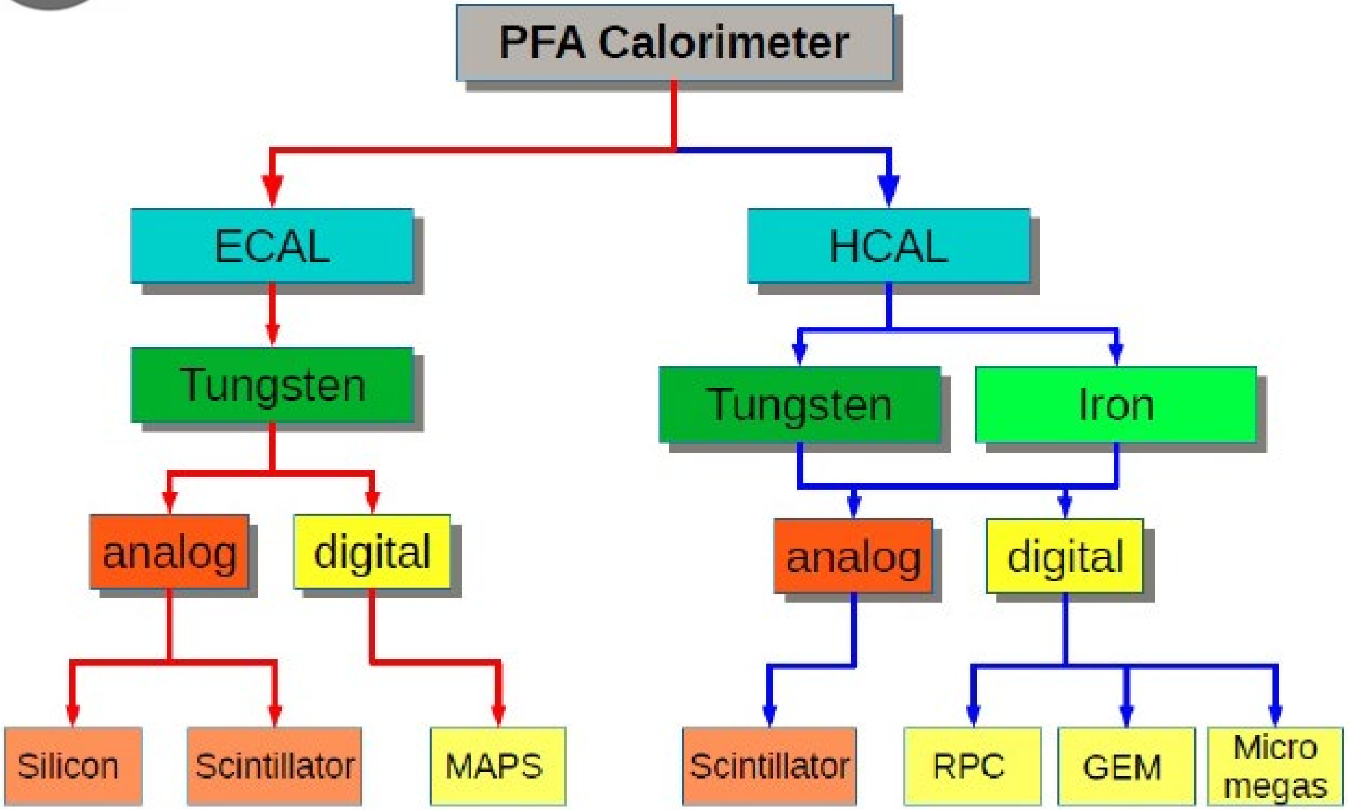
Requirements of CEPC Calorimeters

Physics process	Measurands	Detector subsystem	Performance requirement
$ZH, Z \to e^+e^-, \mu^+\mu^-$ $H \to \mu^+\mu^-$	$m_H, \sigma(ZH)$ $\mathrm{BR}(H \to \mu^+\mu^-)$	Tracker	$\Delta(1/p_T) =$ $2 \times 10^{-5} \oplus \frac{0.001}{p(\mathrm{GeV}) \sin^{3/2}\theta}$
$H \to b\bar{b}/c\bar{c}/gg$	$\mathrm{BR}(H \to b\bar{b}/c\bar{c}/gg)$	Vertex	$\sigma_{r\phi} =$ $5 \oplus \frac{10}{p(\mathrm{GeV}) \times \sin^{3/2}\theta} (\mu\mathrm{m})$
$H \to q\bar{q}, WW^*, ZZ^*$	$\mathrm{BR}(H \to q\bar{q}, WW^*, ZZ^*)$	ECAL HCAL	$\sigma_E^{\mathrm{jet}}/E =$ $3 \sim 4\%$ at 100 GeV
$H \to \gamma\gamma$	$\mathrm{BR}(H \to \gamma\gamma)$	ECAL	$\Delta E/E =$ $\frac{0.20}{\sqrt{E(\mathrm{GeV})}} \oplus 0.01$



PFA Calorimeters

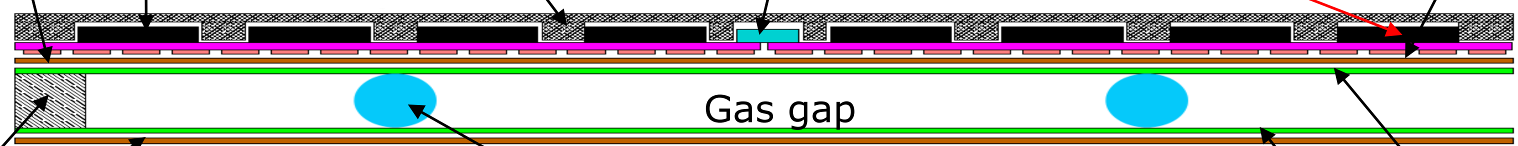
https://twiki.cern.ch/twiki/bin/view/CALICE/CalicePapers



SiW ECAL
ScW ECAL

AHCAL: Scintillator + SiPM
SDHCAL: RPC & MPGD

SDHCAL based on RPC

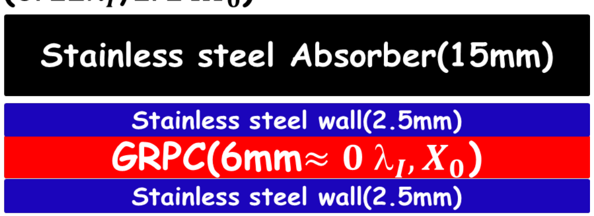


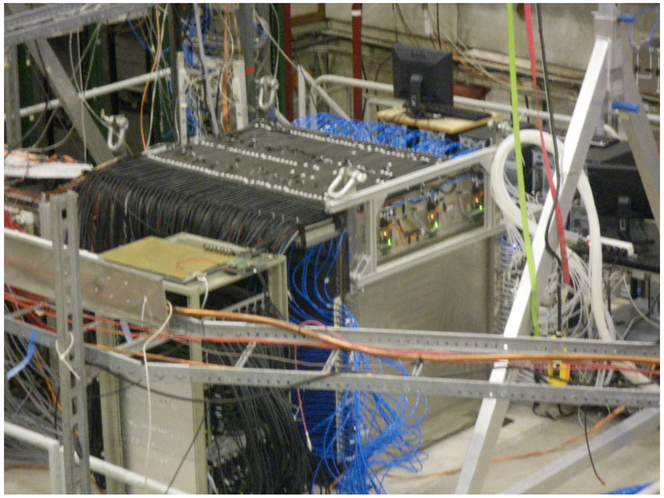
SDHCAL prototype
Size: 1m x 1m x 1.4m
No. of layers: 48
Cell size: 1cm x 1cm
No. of channels: 440K
Power: 1mW/ch

Large GRPC R&D

- ✓ Negligible dead zone
- ✓ Large size: 1 x 1 m^2

$(0.12\lambda_I, 1.14X_0)$





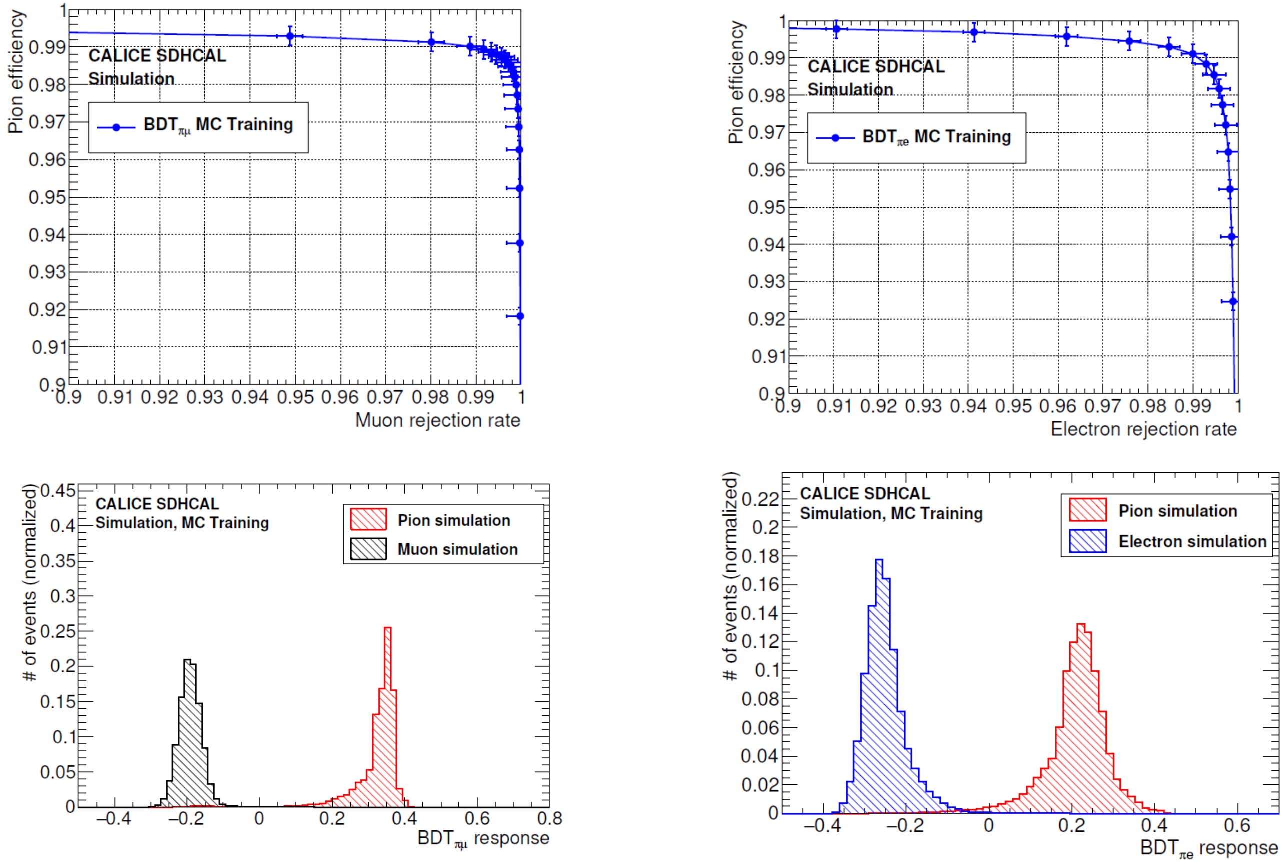
ASIC HARDROC (64 ch)
3-threshold: 110fC, 5pC, 15pC

SDHCAL TB: Particle identification

BDT: Boosted Decision Tree

arXiv:2004.02972

- ➔ **BDT helps to improve the hadron/e/mu PID, purify TB samples.**
- ➔ **Keep 99% of pion efficiency and to reject >99% of e/mu.**

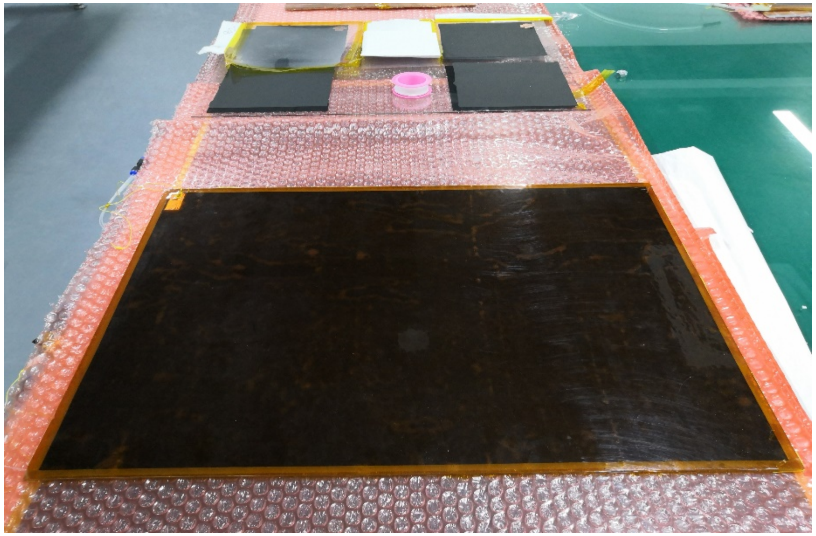


Cleanroom for GRPC Manufacture

Cleanroom has been built for GRPC manufacture at SJTU in January, 2020.

- Class 10000
- Room Size: 6m × 7m

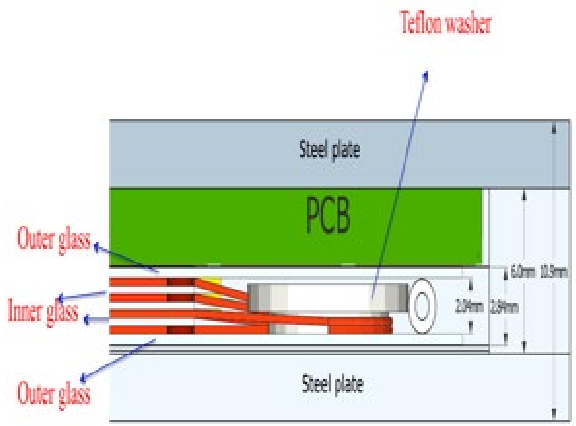
GRPC construction in Cleanroom

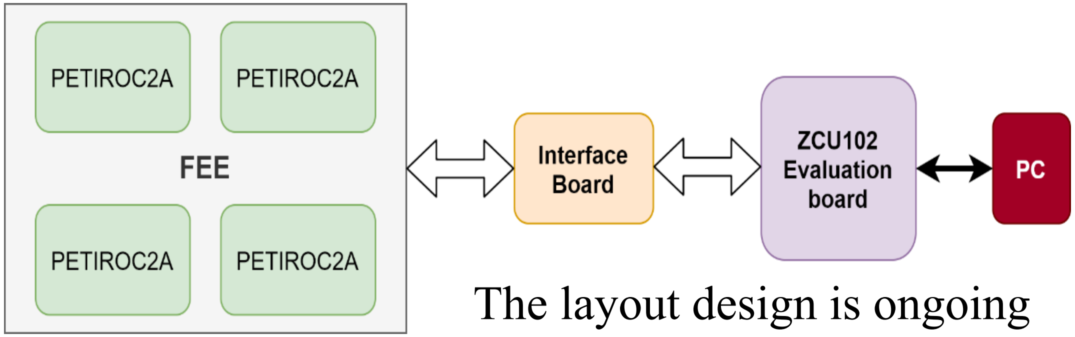


- Several GRPC prototypes have been made and tested.
  - Size: 35cm × 50 cm
  - Successful cosmic ray test
- Next Step:
  - Design a full size of 1m × 1m.

Timing Measurement in SDHCAL

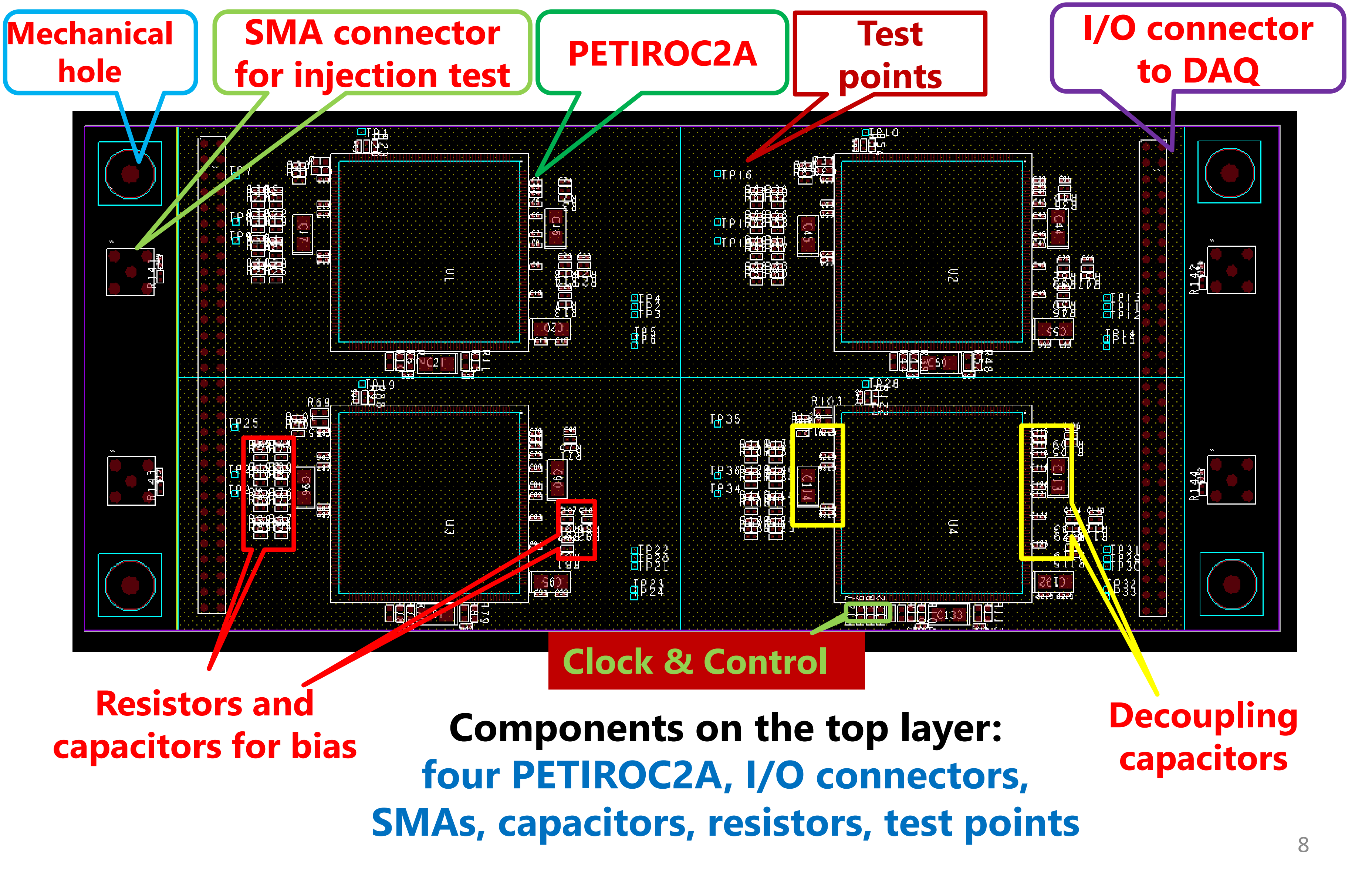
- Five dimension (5D) SDHCAL:
  - Energy, position, timing
- Add several MRPC layers in SDHCal prototype
  - Fast timing detectors
  - Same size as standard RPC
- New electronics
  - Front-end electronics with timing and hit information measurement
  - New DIF hardware and a DAQ system





The layout design is ongoing

Timing Measurement in SDHCAL

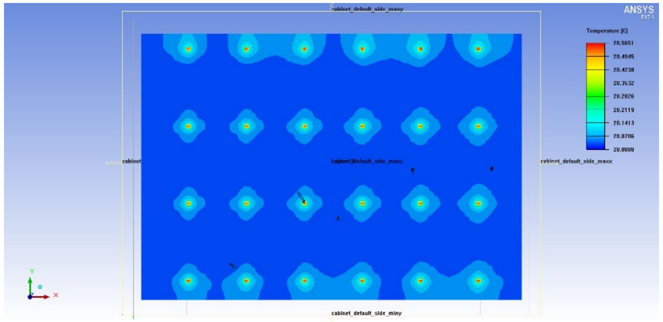


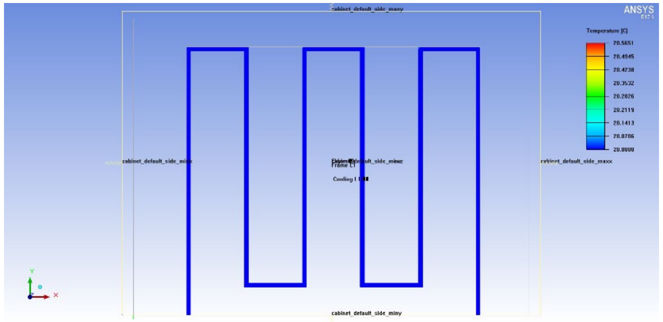
Components on the top layer:
four PETIROC2A, I/O connectors, SMAs, capacitors, resistors, test points

Active Cooling

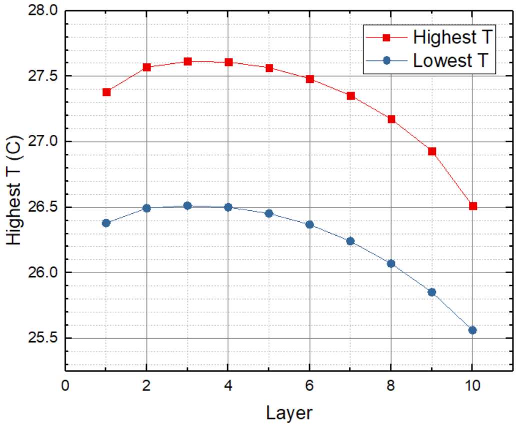
Cooling system is very important

- With cooling at 6th layer:
- With cooling each layer:
  - uniform among layers
  - cooling power: ~1.53W/layer

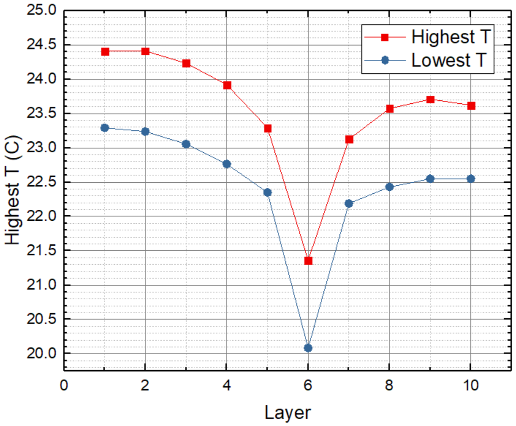




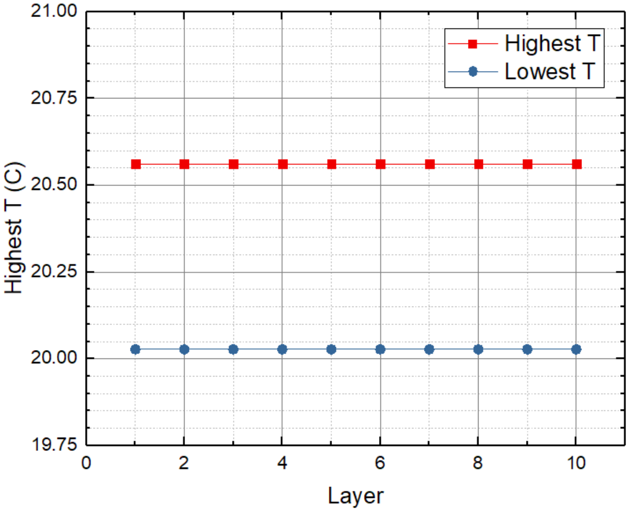
cooling pipes



no cooling



cooling at 6th layer



cooling at each layer

Active Cooling

PCB with resistors to mimic HARDROC ASIC heat source for cooling design and test.

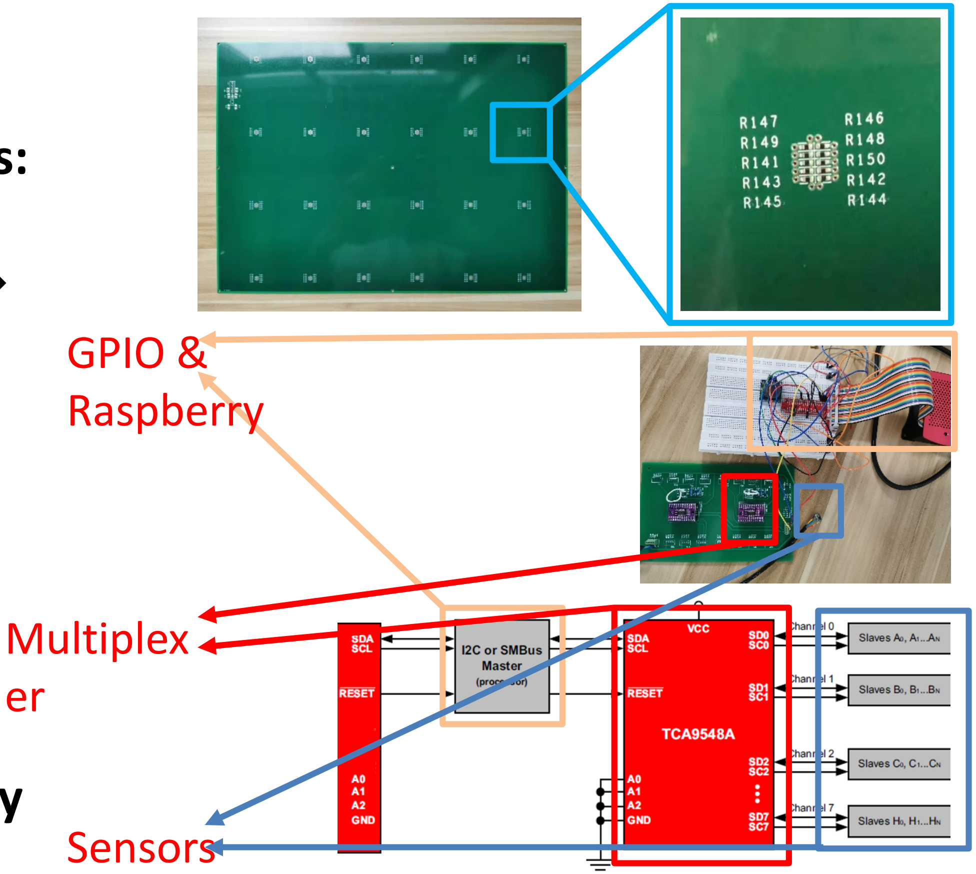
Use resistors substituting for ASICs

- **Resistors: 4*6*10 per PCB**
- **Total resistance of a group of 10 parallel-connected resistors: 470Ω**
- **ASICs in SDHCAL: ~1mW/ch → ~5.5V on resistors**

Sensor: Si70xx, high precision temperature & humidity sensor

- **range: -40~125℃**
- **accuracy: 0.1℃ at most**

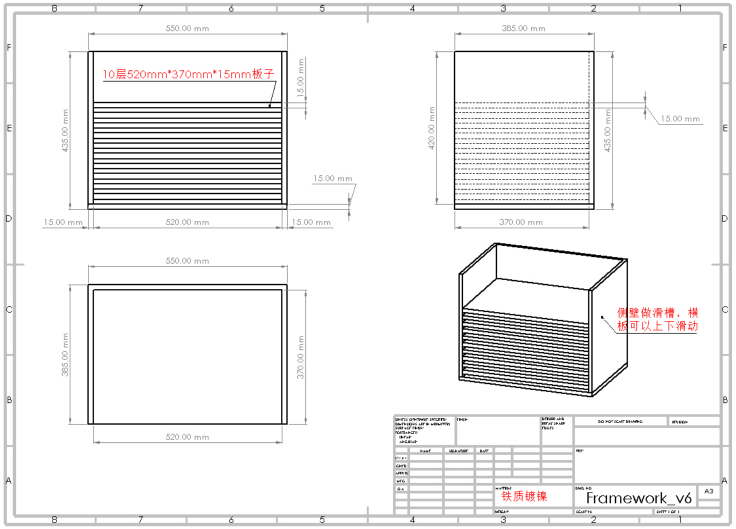
8*8 sensors monitored simultaneously with multiplexers based on I²C



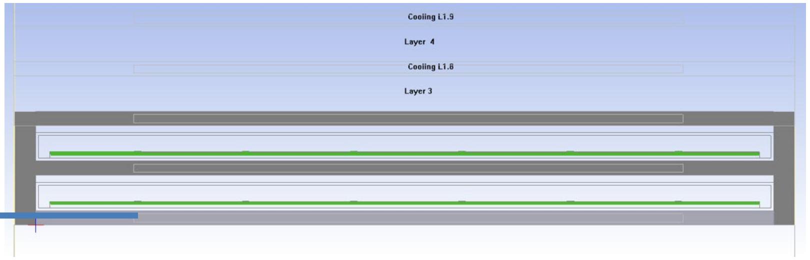
Active Cooling

- Cooling plates: water pipes imbedded in metal plates
  - cooling ability: ~kW/m^2
  - safety(water is not so good)
- Stainless steel
  - poor heat transmission
  - difficult to produce → high cost
  - can work as the absorber
- Aluminum
  - good heat transmission
  - easy to produce
  - 5 times the radiation length than steel

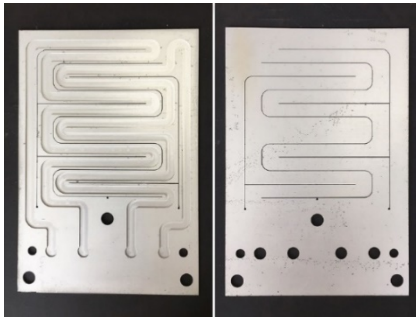
Cooling Test Module



Cooling plate
PCB
RPC
Stainless steel



Cooling plates



PFA Calorimeters

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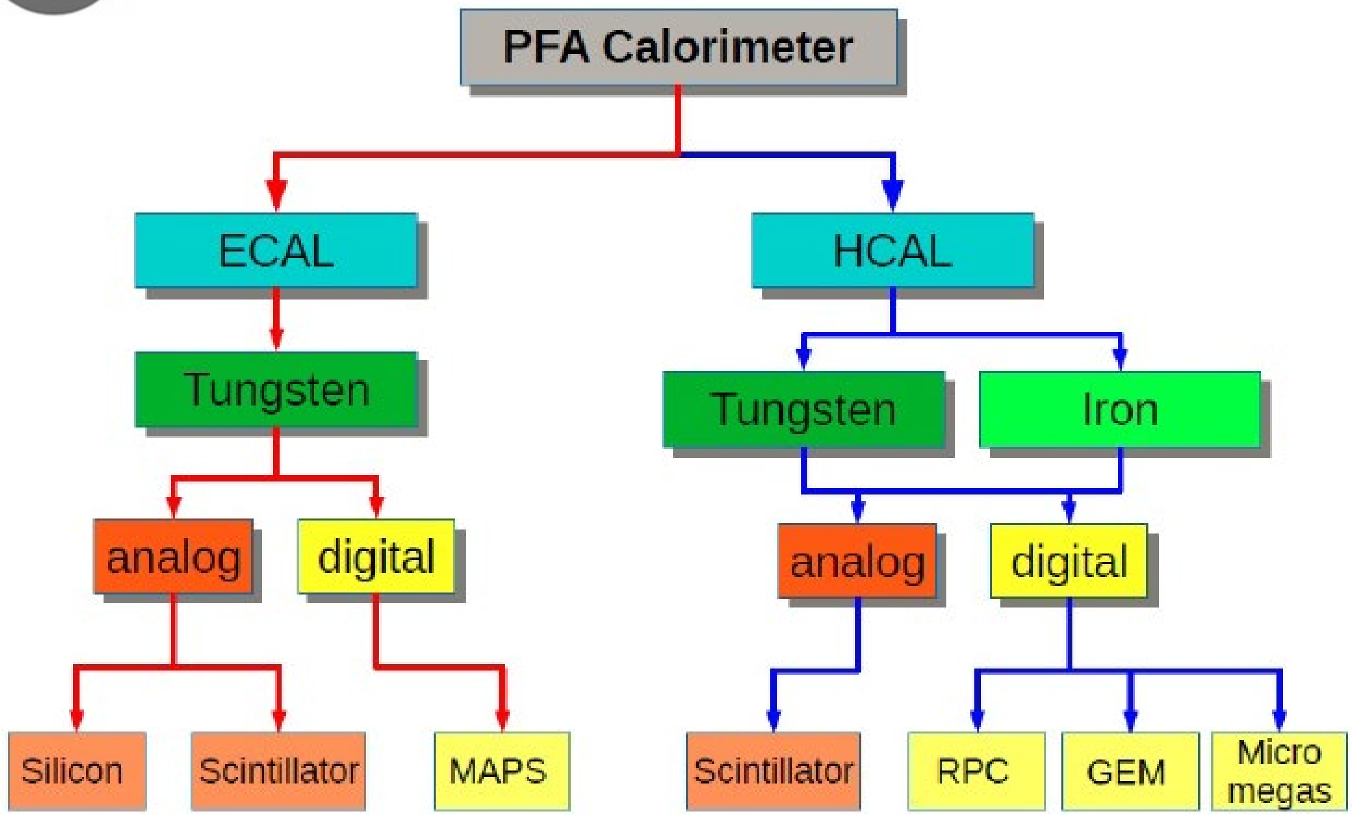
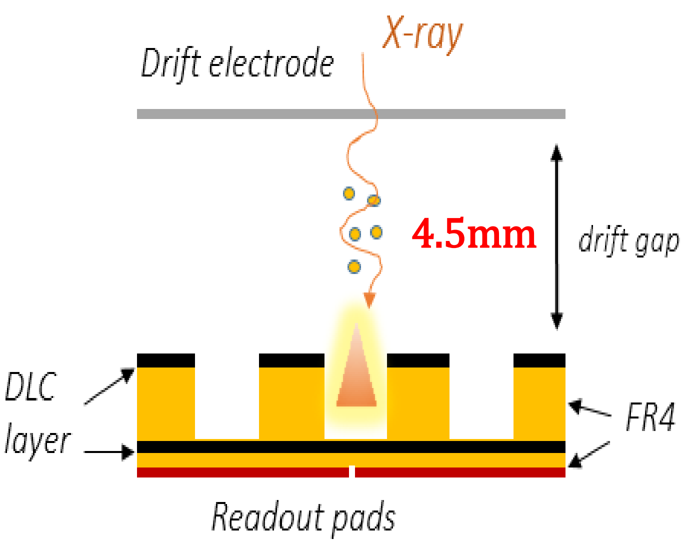


SiW ECAL
ScW ECAL

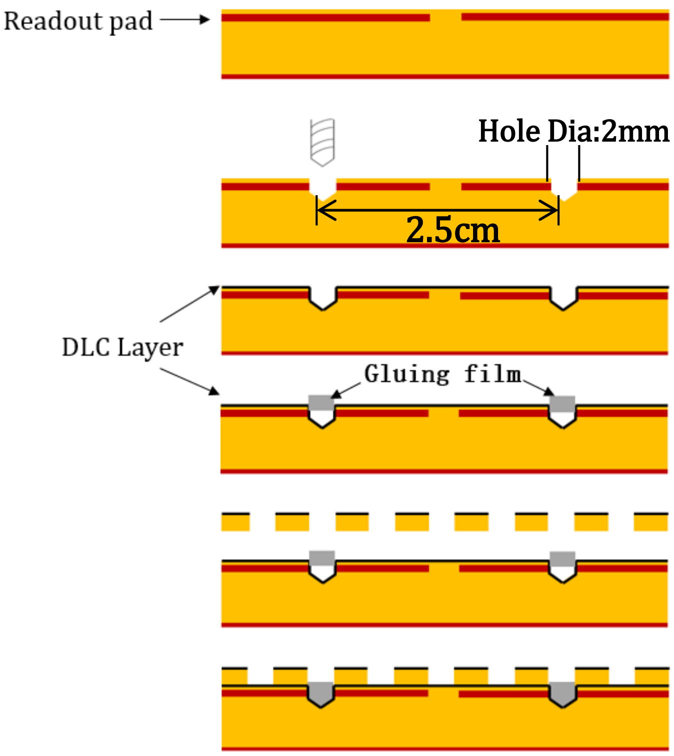
AHCAL: Scintillator + SiPM
SDHCAL: RPC & MPGD

RWELL Detector development

RWELL: Resistive WELL



a) Hole Diameter: 500μm
b) Pitch: 1mm
c) Thickness: 400μm
d) Sensitive area: 25cm× 25cm

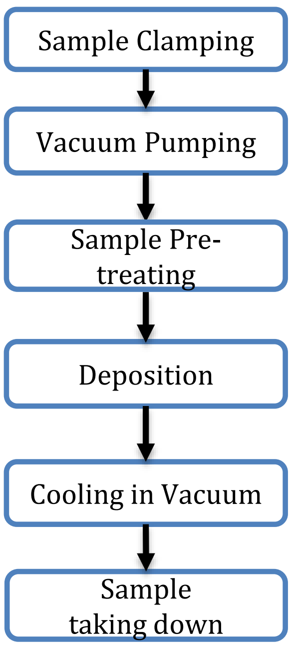


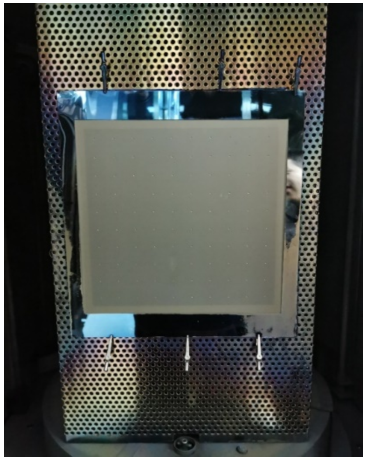
From USTC group

DLC deposition and Thermal bonding

- Key issues for RWELL:
  1. **Resistive layer-DLC(Diamond like carbon)**
  2. **Bonding method**

DLC is deposited on a PCB substrate by the magnetron sputtering method

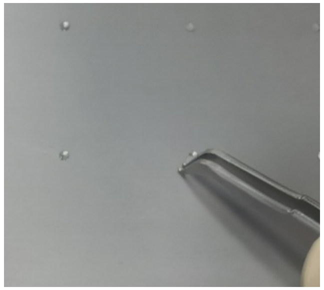




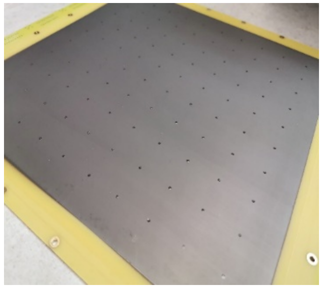
A DLC-coating Readout Board

Surface resistivity :>100MΩ/SQ

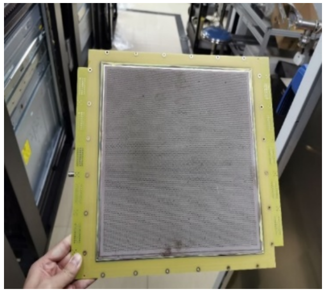
DLC deposition procedure



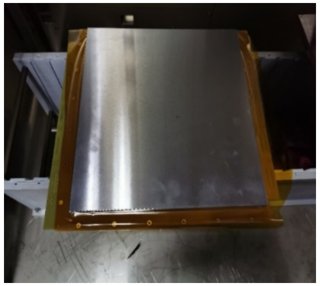
Step 1，Place the gluing film



Step 2，Pre-heating



RWELL Detector

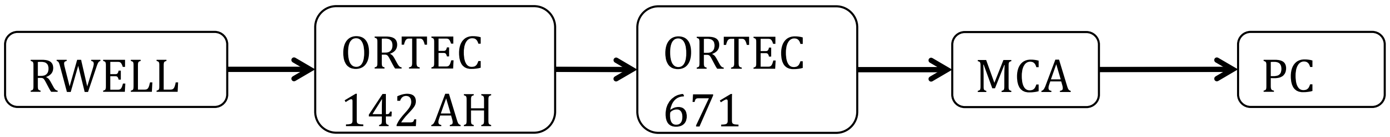


Step 3，Thermal boding

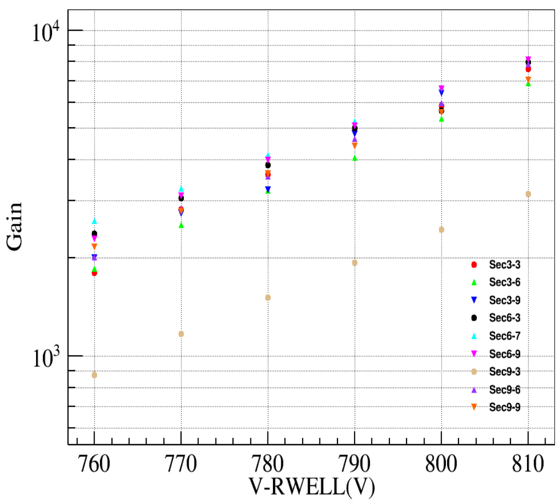
Thermal bonding procedure

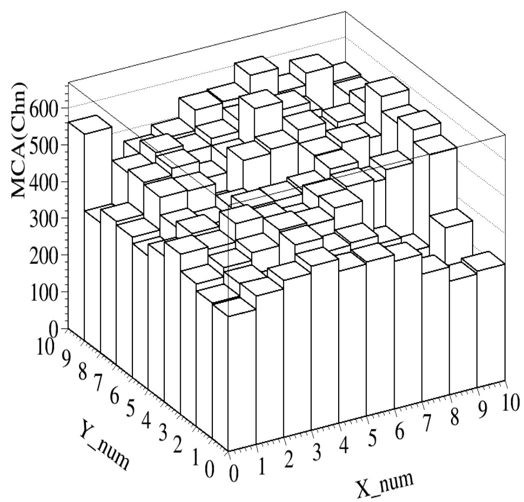
Gain Test

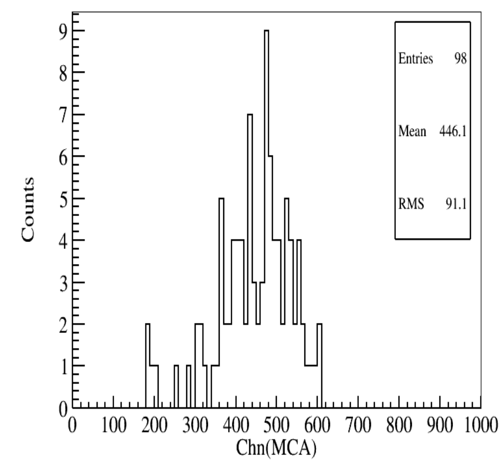
- Test setup :



(pre-amplifier) (Spectroscopy amplifier)







Gain : ~8000

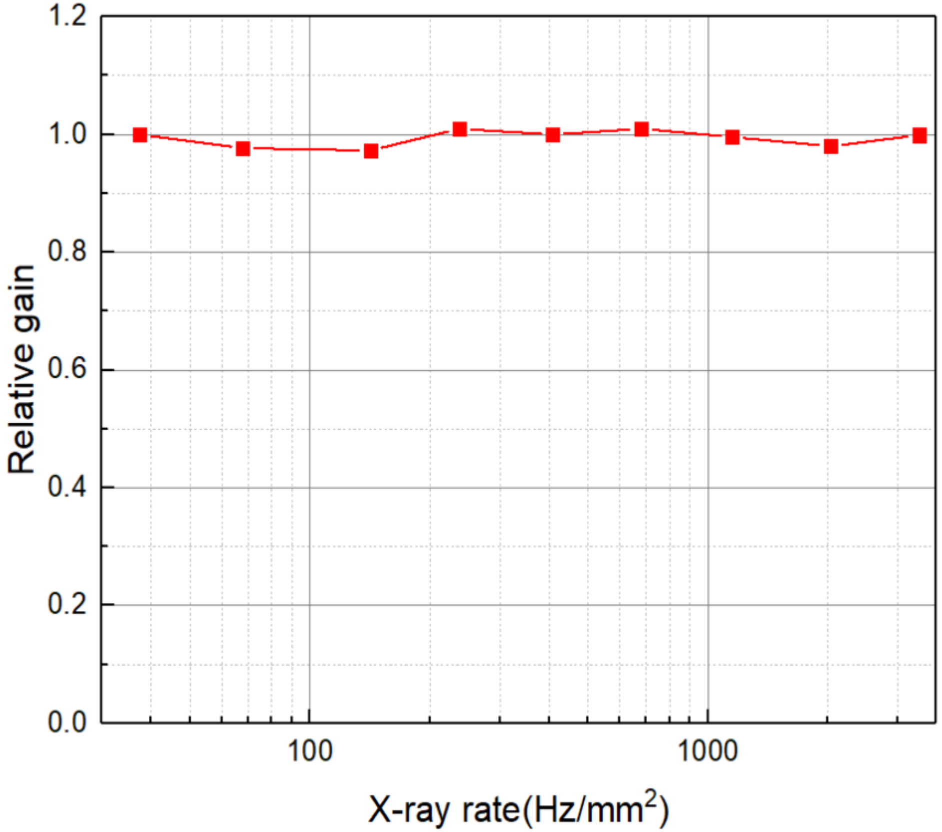
Gain uniformity :RMS/Mean ～20.4%

- Gain uniformity is not good. Possible reason:

    1. Gas flow
    2. Uniformity due to the thermal bonding procedure

Rate Capability

- RWELL is irradiated with 8 keV X-ray, and gain of the detector is almost no reduction@300kHz/cm^2 (Initial gain G0:～5500).



- Detector discharge while irradiated at a higher rate

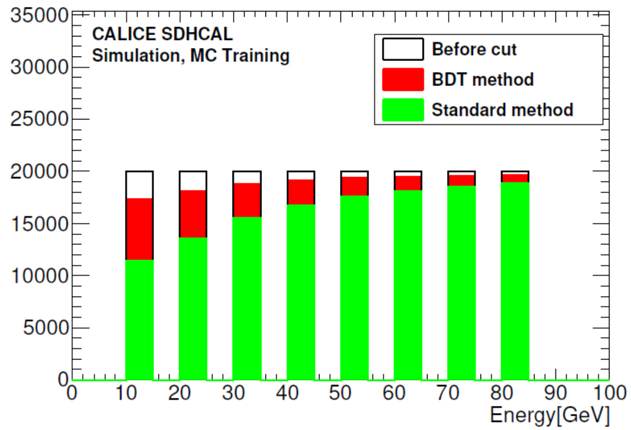
Summary and Future Plans

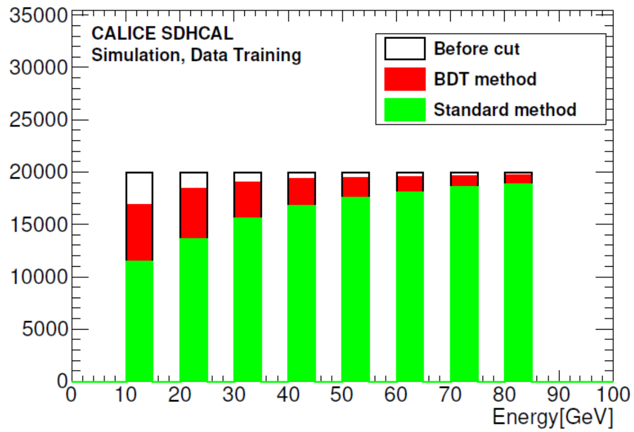
- SDHCAL prototype constructed and made several TB at CERN.
- The TB data analysis using BDT method has been submitted to JINST.
- Cleanroom has been built for RPC construction at SJTU.
- The design of electronics and PCB for MRPC readout is ongoing
  - Timing measurement
- The simulation and test module for active cooling is progressing.
- The R&D of RWELL detector goes well and several tests have been carried out successfully.
- Close collaboration with several international research institutes (eg. IPNL, Weizmann, Israel Inst. of Tech.)

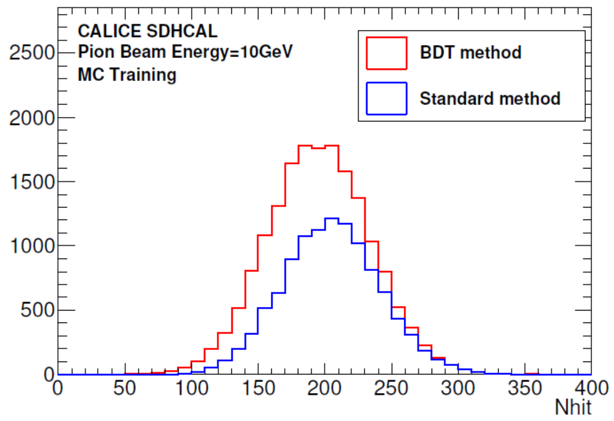
Thanks for your attention !

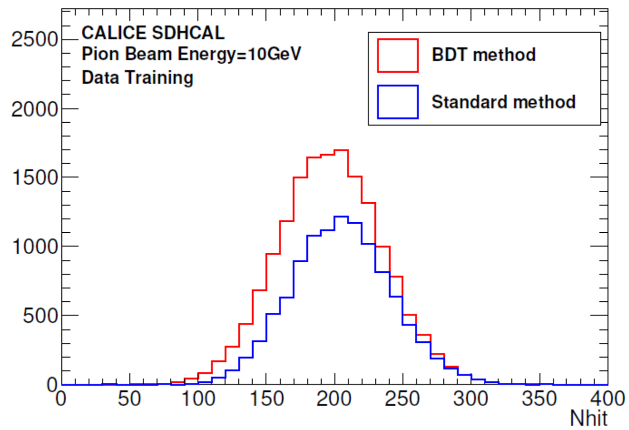
Backup

SDHCAL: Particle identification

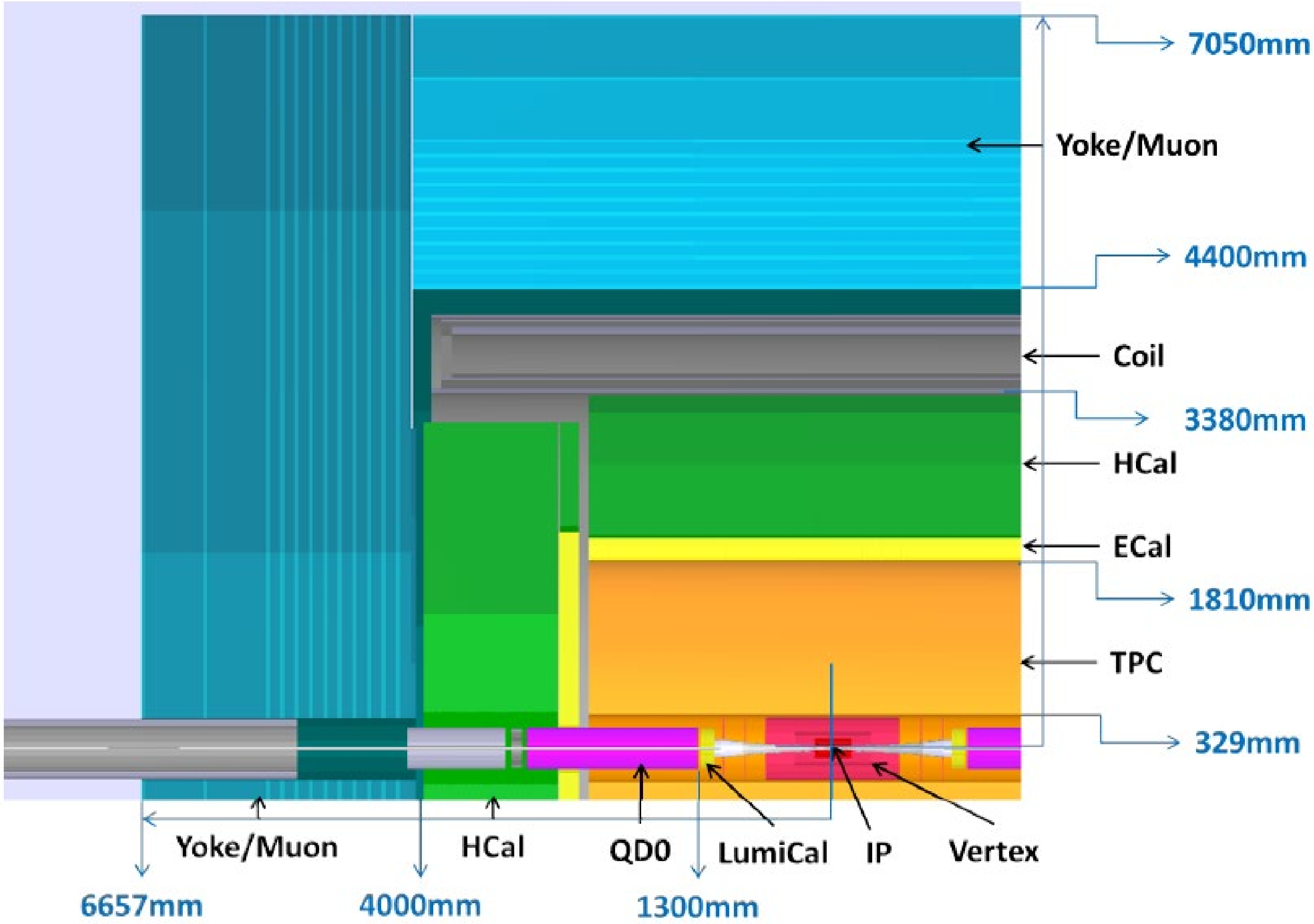




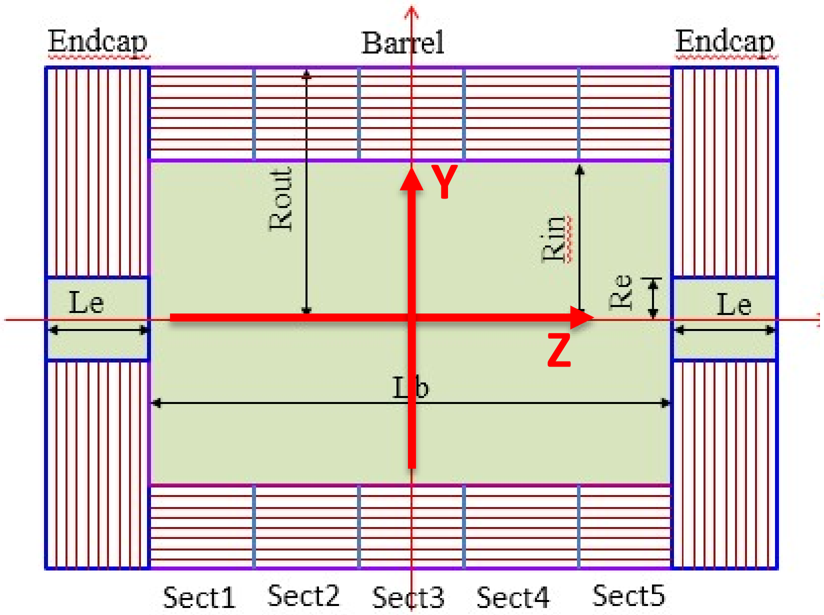


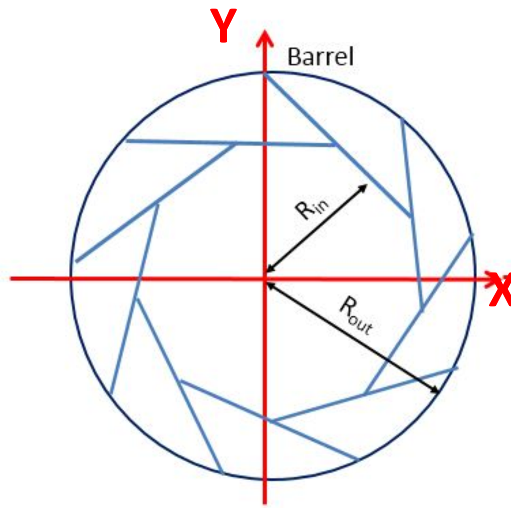


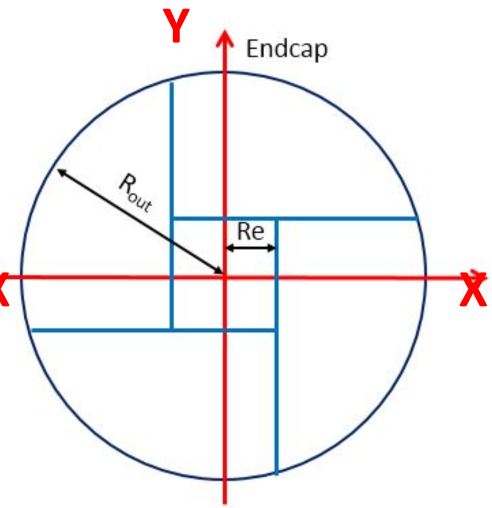
Schematic of CEPC Detector



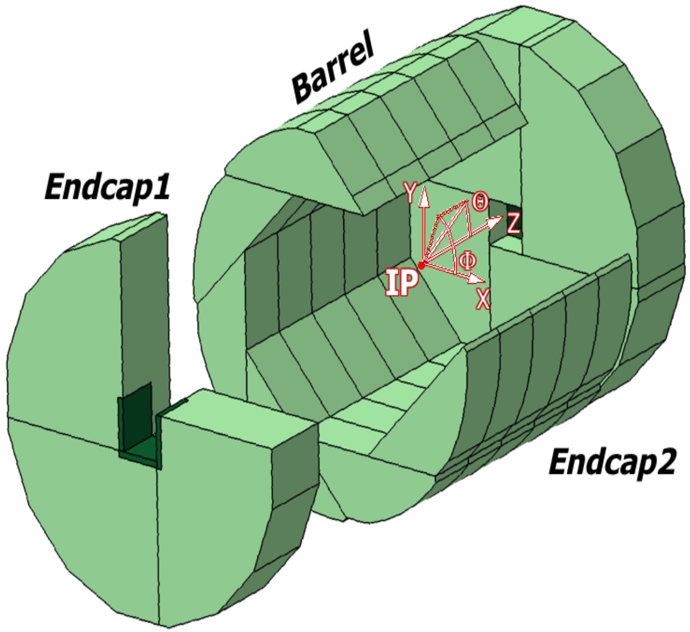
CEPC HCAL Geometry





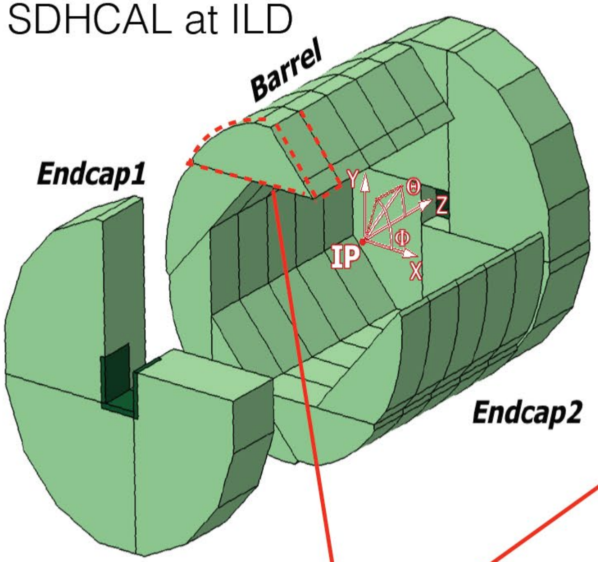


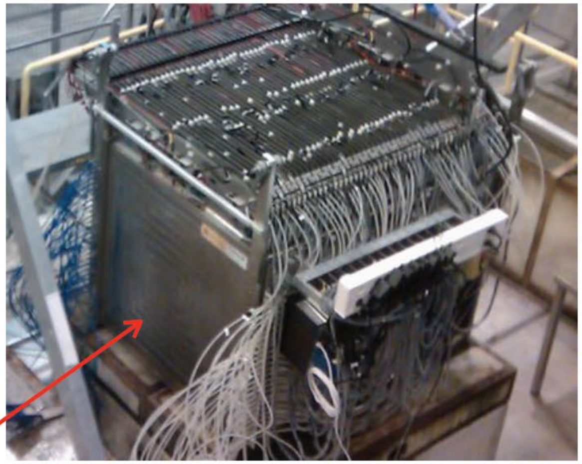
- Inner radius in X-Y plane R_{in} = 2300mm
- Outer radius R_{out} = 3340mm
- Inner & outer of HCAL endcap in Z-axis are 2670mm and 3710mm



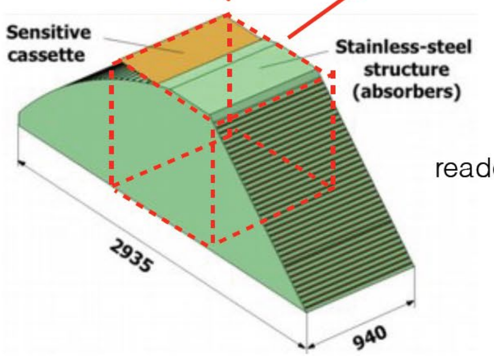
SDHCAL based on RPC

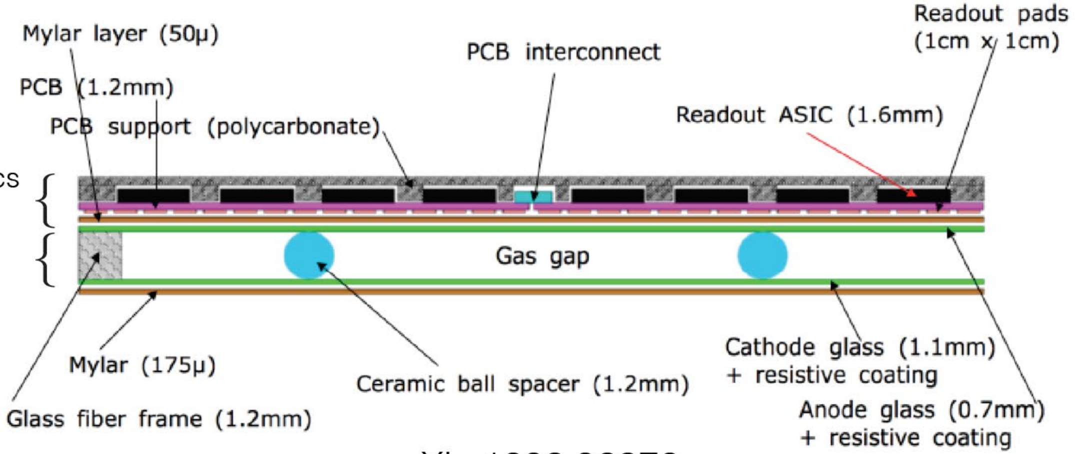
SDHCAL at ILD





- 48 layers, 6 λ_I
- GRPC (1×1 m²)
- Cell pads:1×1 cm²
- On each layer, ASIC: 12 x 12; 64 ch. on each ASIC; 9612 ch. in total
- Three thresholds readout (2 bits): (0.11, 5, 15) pC
- Power-pulsing electronics
- Self-supporting mechanical structure as absorber as well





- Very compact with negligible dead zones
- Eliminates projective cracks
- Minimizes separation of barrel and endcap

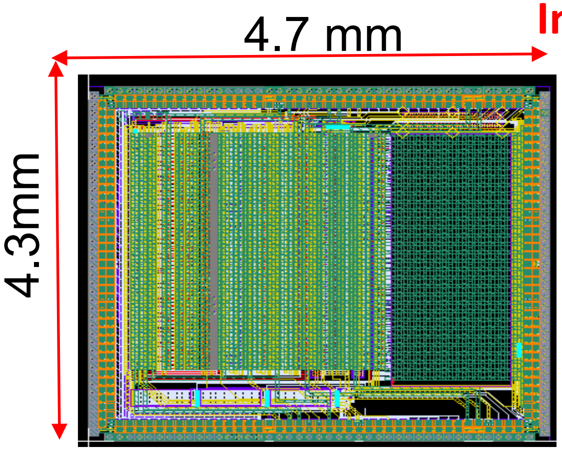
arXiv:1602.02276

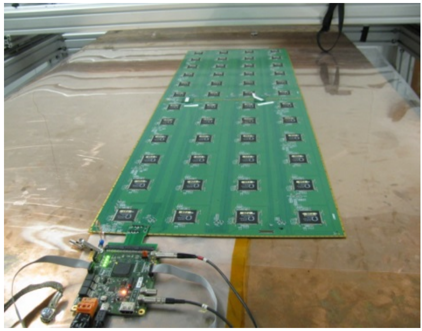
JINST 10 (2015) P10039

Electronics Readout

Imad Laktineh (IPNL)

ASICs : HARDROC2
64 channels
Trigger less mode
Memory depth : 127 events
3 thresholds
Range: 10 fC-15 pC
Gain correction → uniformity

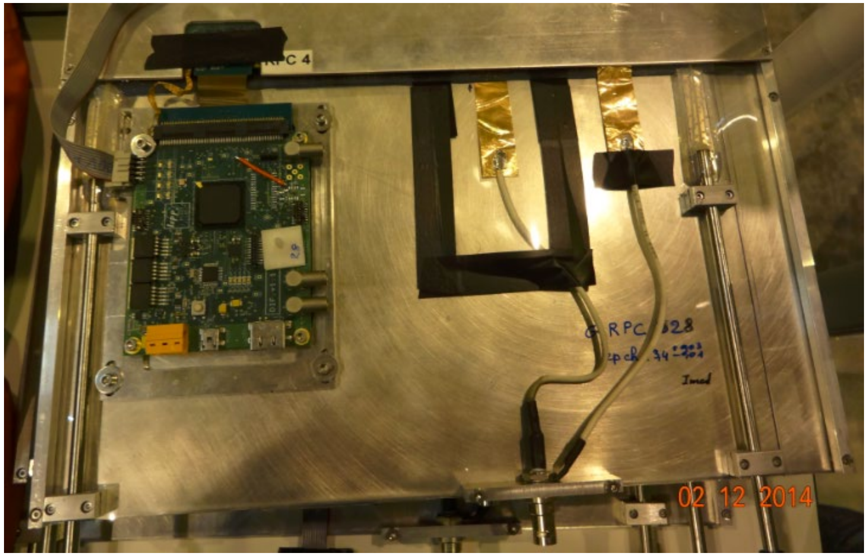




Printed Circuit Boards (PCB) were designed to reduce the cross-talk with 8-layer structure and buried vias.

Tiny connectors were used to connect the PCB two by two so the 24X2 ASICs are daisy-chained. 1×1m^2 has 6 PCBs and 9216 pads.

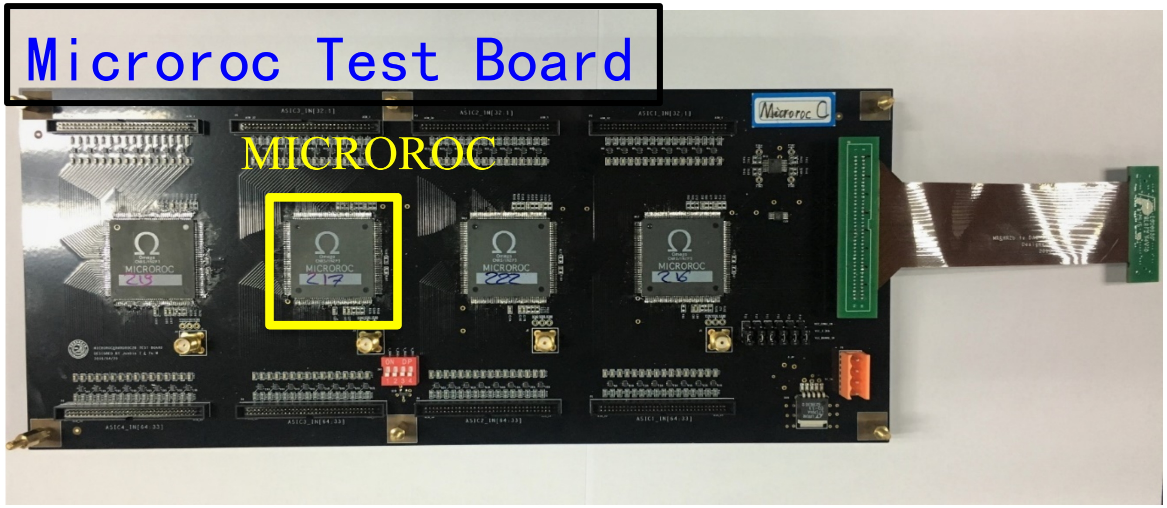
DAQ board (DIF) was developed to transmit fast commands and data to/from ASICs.



Readout ASIC

Readout ASIC	Channels	Dynamic Range	Threshold	Consumption
GASTONE	64	200fC	Single	2.4mW/ch
VFAT2	128	18.5fC	Single	1.5mW/ch
DIRAC	64	200fC for MPGD	Multiple	1mW/ch, 10μW/ch
DCAL	64	20fC~200fC	Single	——
HARDROC2	64	10fC~10pC	Multiple	1.42mW/ch,10μW/ch
MICROROC	64	1fC~500fC	Multiple	335μW/ch, 10μW/ch

Considered the multi-thresholds readout, dynamic range and power consumption, MICROROC is an appropriate readout ASIC



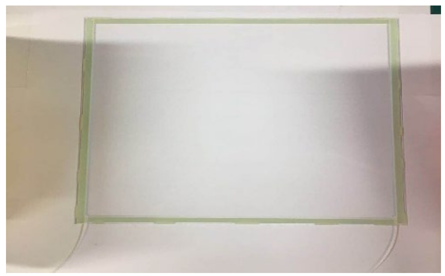
MICROROC Parameters

- Thickness: 1.4mm
- 64 Channels
- 3 threshold per channel
- 128 hit storage depth
- Minimum distinguishable charge:2fC

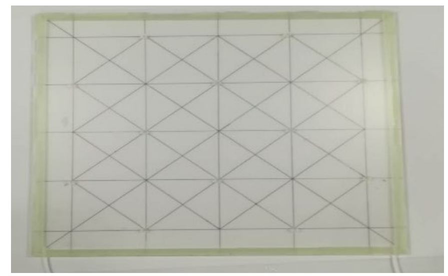
SDHCAL: RPC Construction at SJTU

1.Position the walls and pipes

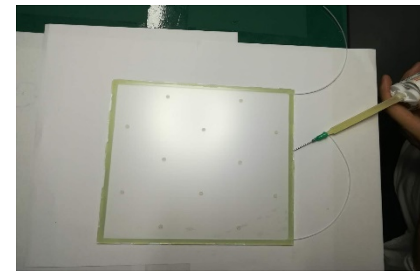
2.Glue walls and pipes.

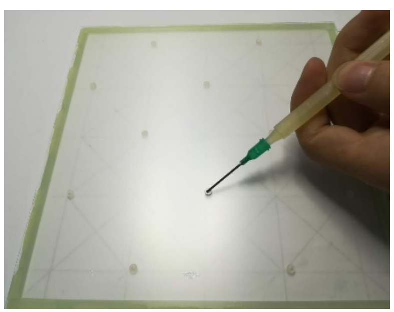


3.Draw the spacer position sketch

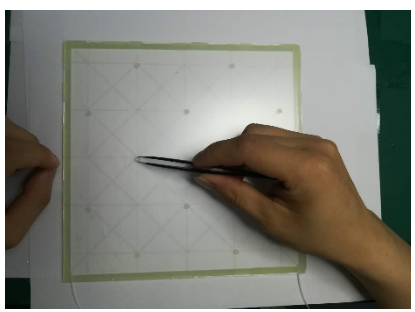


4.Put the spacers on the glass

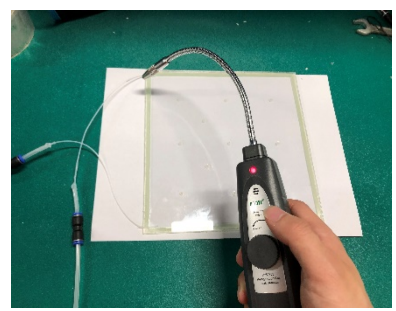




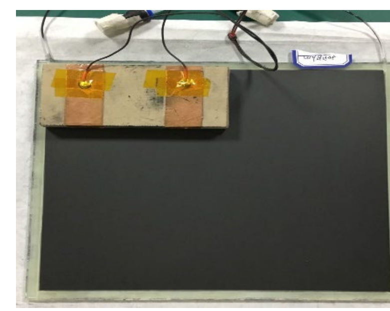
5.Glue the spacers



6. Glue the second glass to the walls

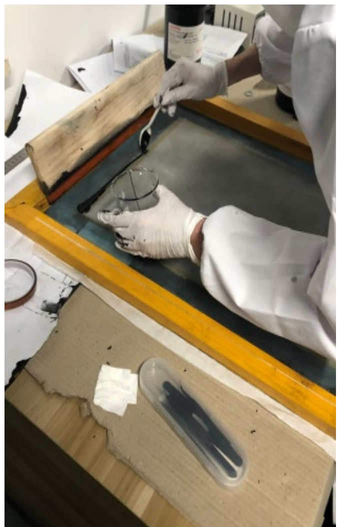


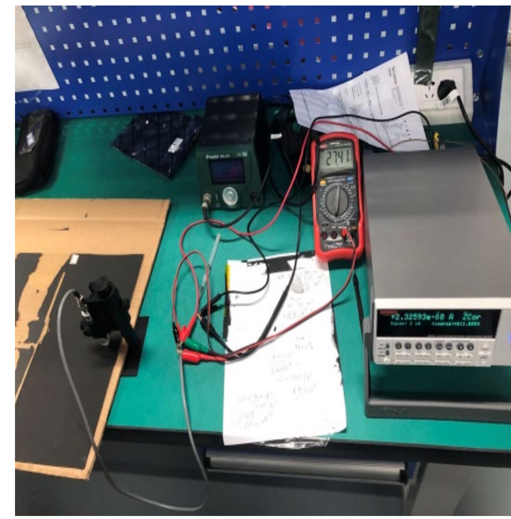
7. Gas tight with silicon and test leaks

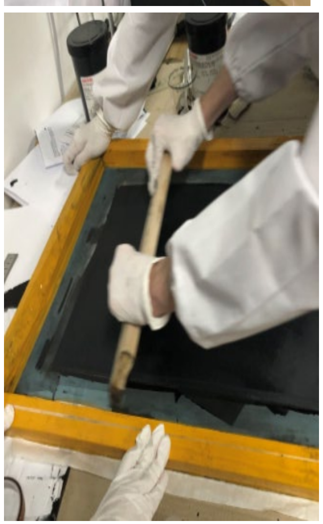


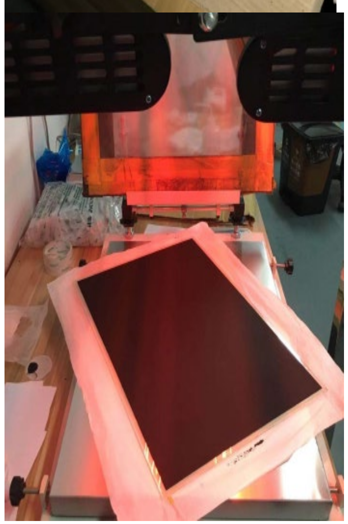
8. Graphite coating and mylar fixing

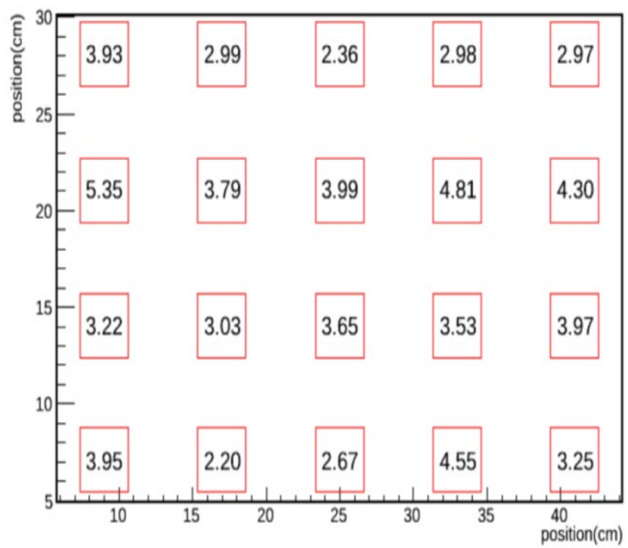
SDHCAL: RPC Construction

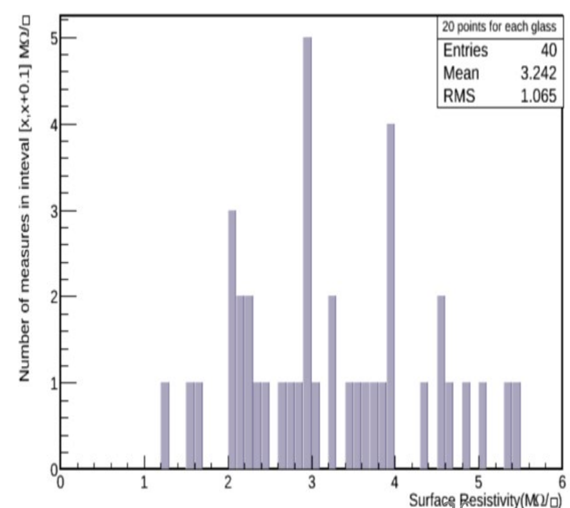










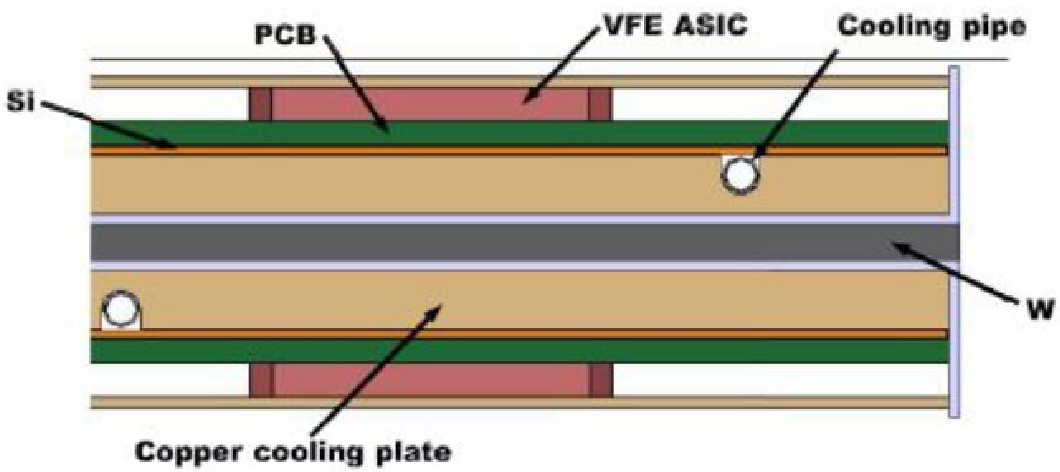


Active Cooling

- CEPC is designed to operate at continuous mode with beam crossing rate: 2.8×10^5 Hz. Power pulsing will not work at CEPC.
- Compare to ILD, the power consumption of VFE readout electronics at CEPC is about two orders of magnitude higher, hence it requires an active cooling
  - Evaporative CO_2 cooling in thin pipes embedded in Copper exchange plate.
  - For CMS-HGCAL design: heat extraction of 33 mW/cm^2, allows operation with 6×6 mm^2 pixels with a safety margin of 2
- To be modelled for Mokka simulation

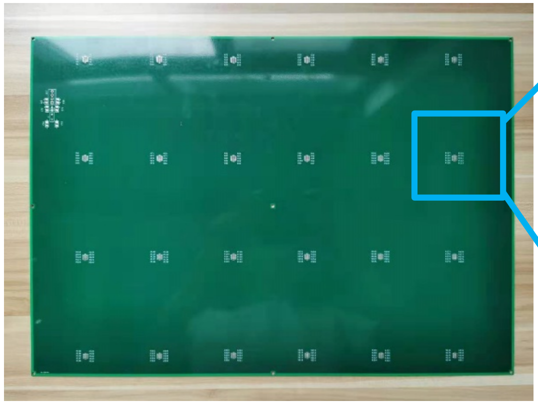
➔ **Transverse view of the slab with one absorber and two active layers.**

➔ **The silicon sensors are glued to PCB with VFE chips, cooled by the copper plates with CO_2 cooling pipes.**



Active Cooling Simulation and Test

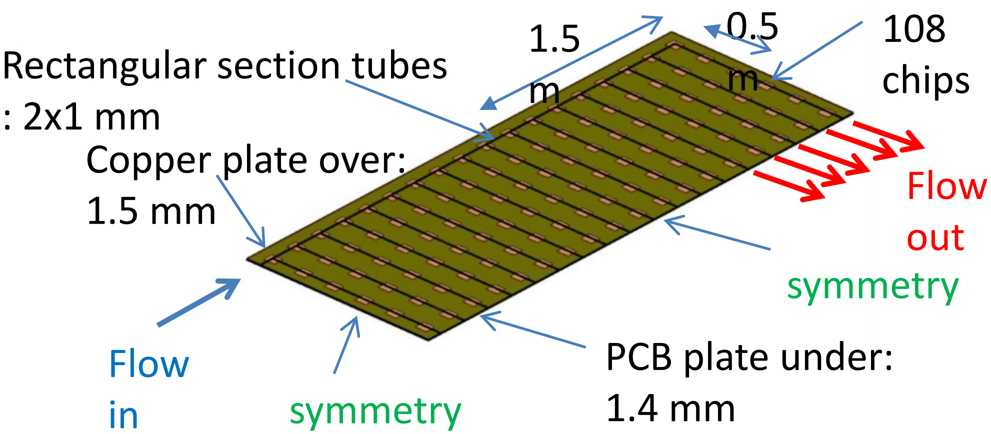
- Resistors: 4*6*10 per PCB
- Total resistance of a group of 10 parallel-connected resistors: 470Ω
- ASICs in SDHCAL: ~0.064W/chip
  ➔ ~5.5V on resistors
- Requirements for the power supply:
  - Voltage range: >0~5.5V
  - Output power: >1.536W/PCB
  - Adjustable/programmble



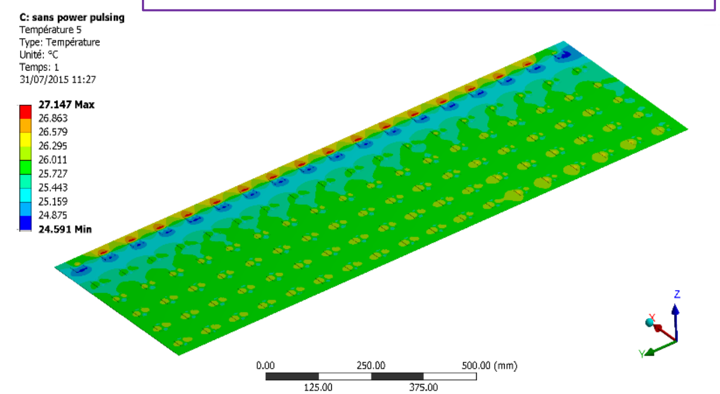
Resistance(Ω)	4.7k
Power rating(W)	0.0625(~17V)
Max operating voltage(V)	50
Max overload voltage(V)	100
Max operating T(℃)	155
Min operating T(℃)	-55
Temperature coefficient	±100ppm/℃

Active Cooling Simulation

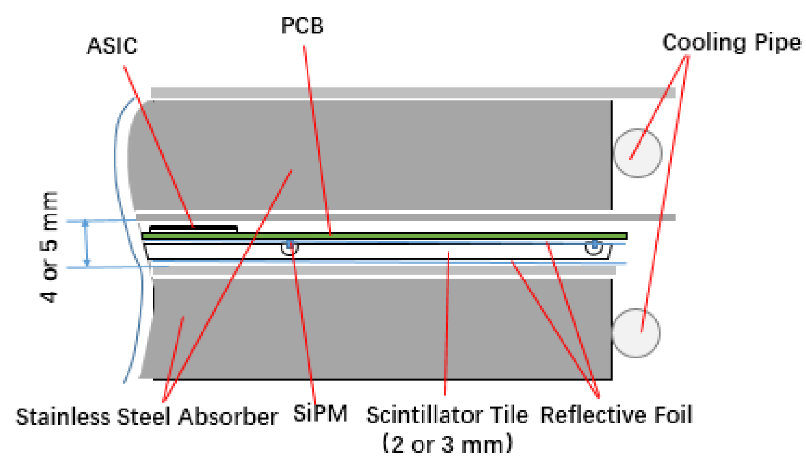
Cooling maybe necessary if operating at continuous mode (CEPC)



27.147 (max) – 24.591 (min) =2.556 °C



- A water-based cooling system inside copper tubes in contact with the ASICs to absorb excess heat.
- Temperature distribution in an active layer of the SDHCAL.

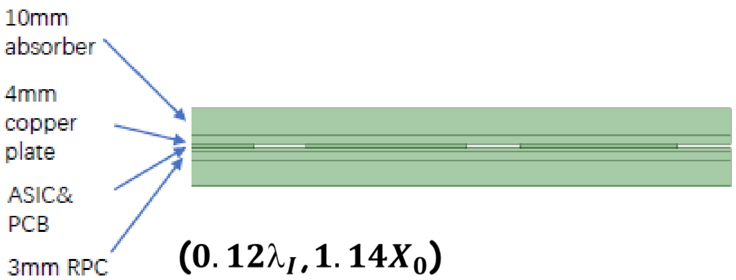


Water cooling : h = 10000 W/m²/k
Thermal load : 80 mW/chip

- For AHCAL, a water-based copper cooling system embedded in the stainless steel absorber.

Active Cooling Simulation

ANSYS Simulation of RPC+PCB With copper plate & water tubes



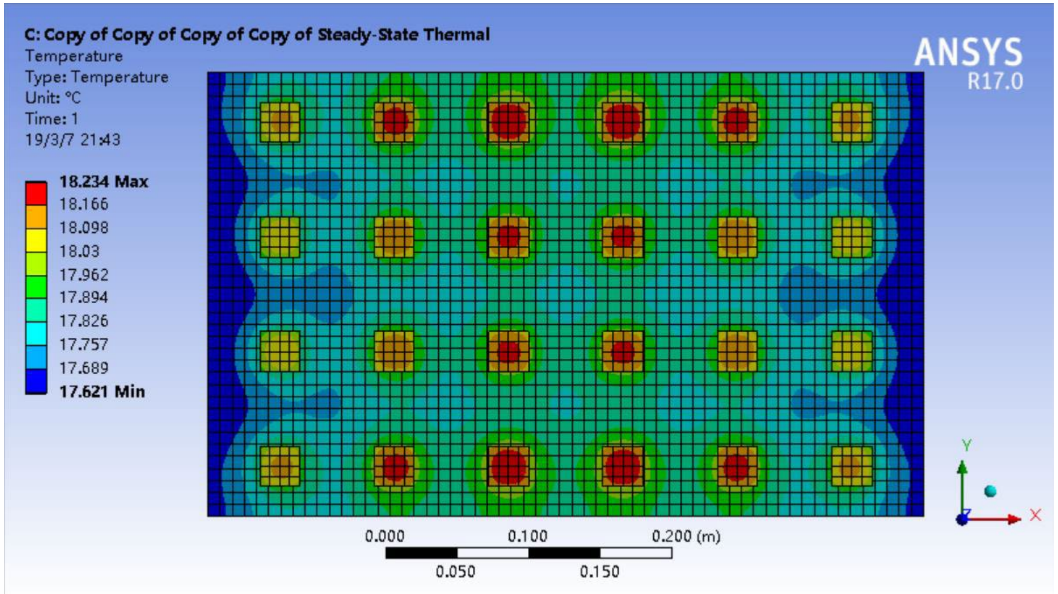
$(0.12\lambda_I, 1.14X_0)$

Stainless steel Absorber(15mm)

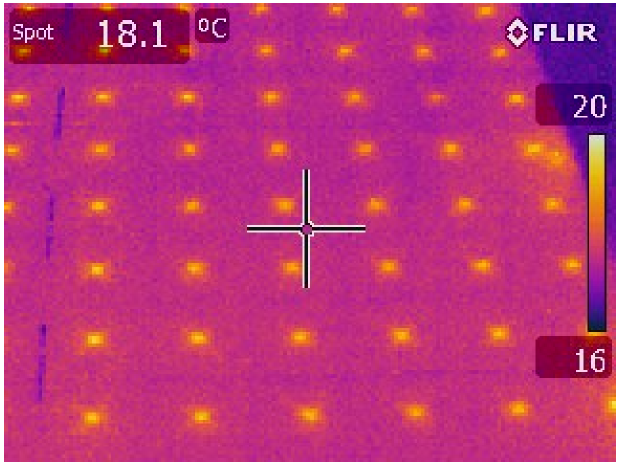
Stainless steel wall(2.5mm)

GRPC(6mm≈ $0\ \lambda_I, X_0$)

Stainless steel wall(2.5mm)



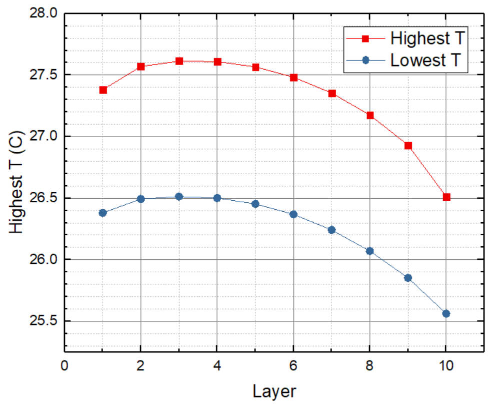
Temperature test of RPC+PCB



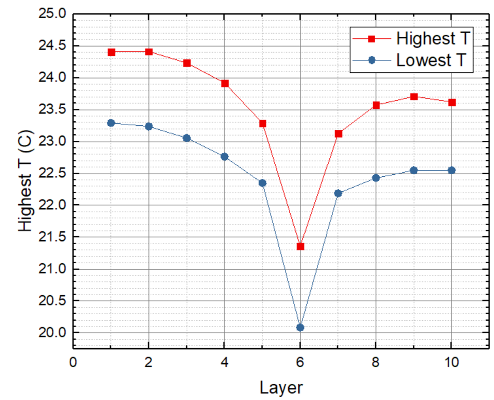
Active Cooling Simulation

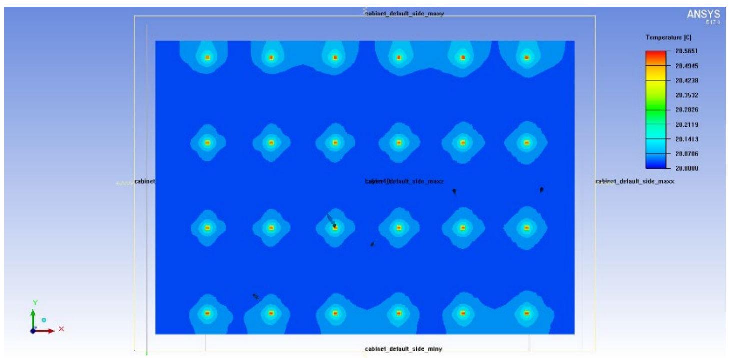
- 10 layers, flow rate: 1m/s
- With cooling at 6th layer:
- With cooling each layer:
  - uniform among layers
  - cooling power: ~1.53W/layer

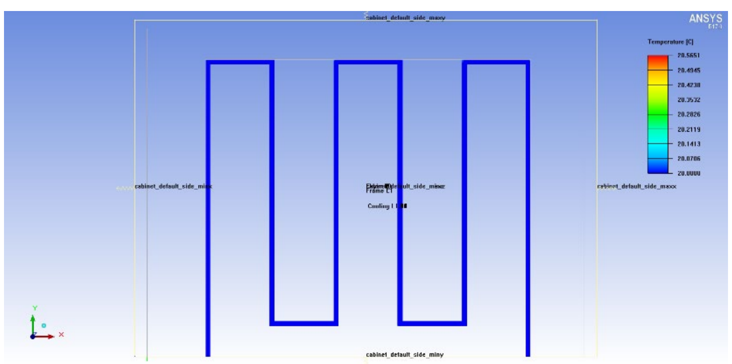
no cooling



cooling at 6th layer

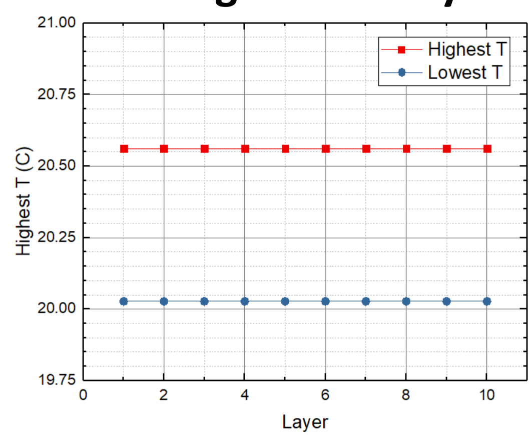


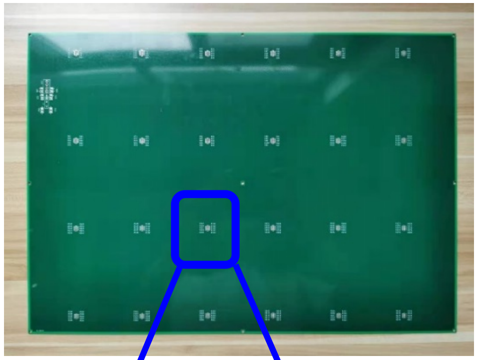




cooling pipes

cooling at each layer



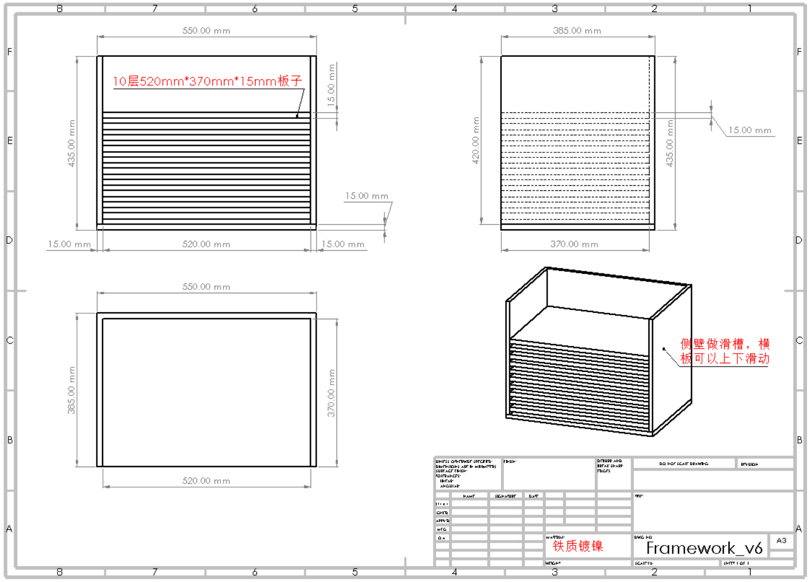


PCB with resistors to mimic HARDROC ASIC heat source for cooling design and test.

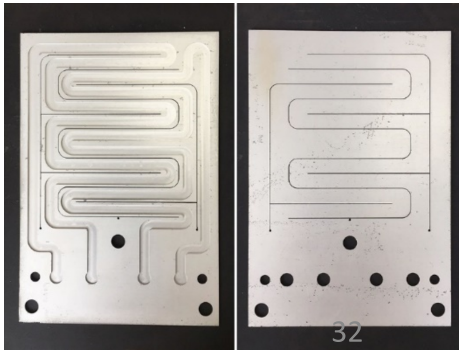
Active Cooling Module

- Cooling plates: water pipes imbedded in metal plates
  - cooling ability: ~kW/m^2
  - safety(water is not so good)
- Stainless steel
  - poor heat transmission
  - difficult to produce → high cost
  - can work as the absorber
- Aluminum
  - good heat transmission
  - easy to produce
  - 5 times the radiation length than steel

Cooling Test Module



Cooling plates



Cooling plate
PCB
RPC
Stainless steel