中国科学院高能物理研究所
Institute of High Energy Physics
Chinese Academy of Sciences

TaichuPix-1 pixel analog test results

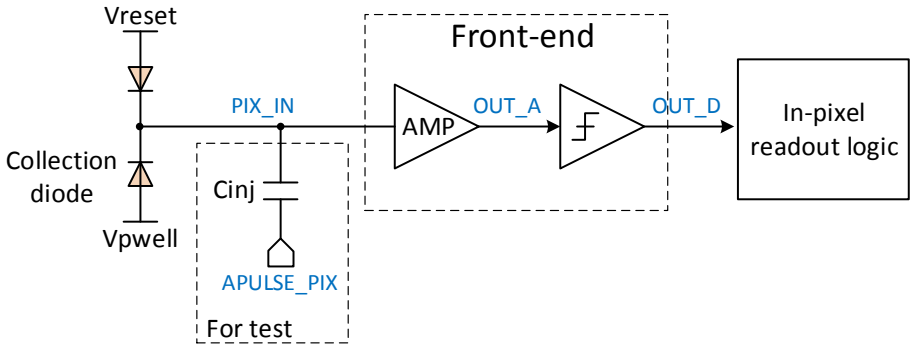
Ying ZHANG

Overview of the testing status

- **Three chips (test boards #2-#4) have been tested**

  only one chip (#4) functional to external charge injection (APULSE)

  - Using **internal Bandgap** for biasing DACs. Two of which are lower than the design value
    - VBG2= 0.45 V, VBG3= **0.68 V– 0.96 V** , VBG4=0.47 V
    - **Each chip provides different biasing values with same DAC input codes**
  - Using external APULSE to inject voltage steps (charges)
  - Analog output (**OUT_A**) performance measured through analog readout buffers for the 23 monitored pixels for chip #4



Block diagram of a pixel.

Chip #4 performance

- **VBG=0.47 V (stable, no oscillation observed)**
- **Output range of CDACs (current DACs) much lower than design**
  - ITHR can NOT reach the desired value for pixel

    max. = 0.58 nA, nominal 4.5 nA, but should be **enough for pixel work functionally**

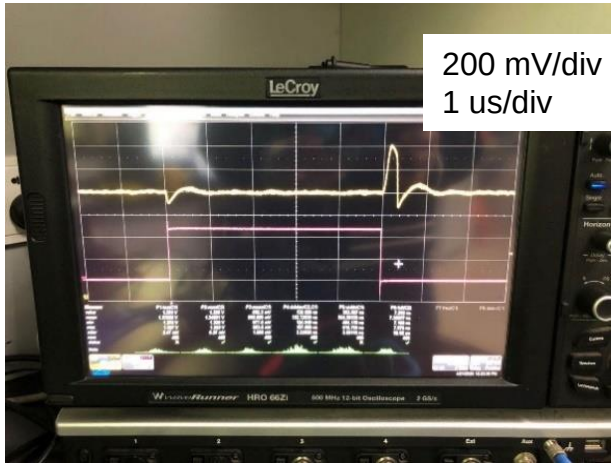
    IHTR max. is 4 times lower than Chip#2
  - IBIAS max.= 255 nA (nominal value = 440 nA, designed range 0~7.5 μA)
- **Output range of VDACs (voltage DACs) of around half of the design**
  - Satisfy the required voltage bias
- **Different output with same input code for DACs, especially CDACs**
- **Analog front-end has response to the injection APULSE**

Bias	IBIAS	ITHR	IDB	VCLIP	VCASP	VCASN	VCASN2	VRESET
Design value	440 nA	4.5 nA	1 μA	0/0.2 V	0.6 V	0.55 V	0.5 V	1.4 V
Config. value	**255nA-286 nA***	**0.58 nA-0.70 nA***	0.54-0.56 μA	0.18 V	0.55 V	0.53 V	0.53 V	1.7 V

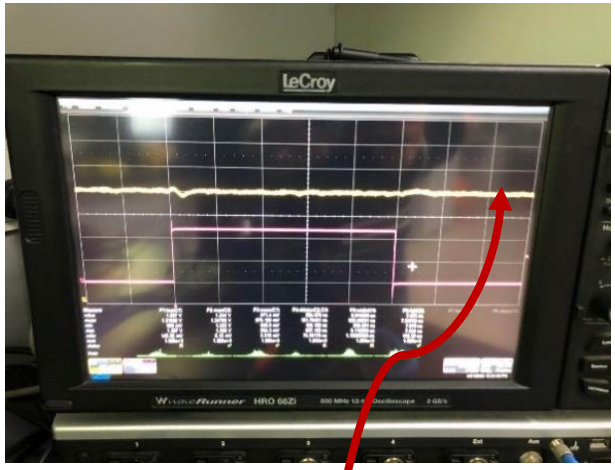
* CDAC output different values with same input codes, which will affect the threshold and noise of FE

Chip #4 performance

- **VPWELL= 0 V, pulsing with VHIGH = 1.2 V, VLOW = 0.3 V- 1.1 V**

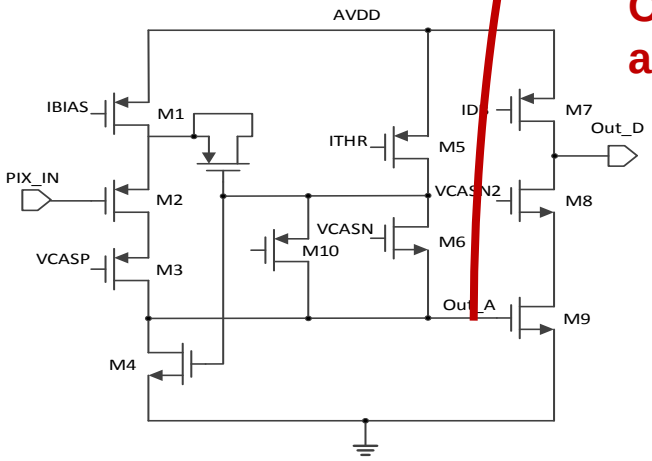


OUTA@VLOW=0.3V



OUTA@VLOW=1.09 V

OUTA with analog buffer



Chip #4 performance

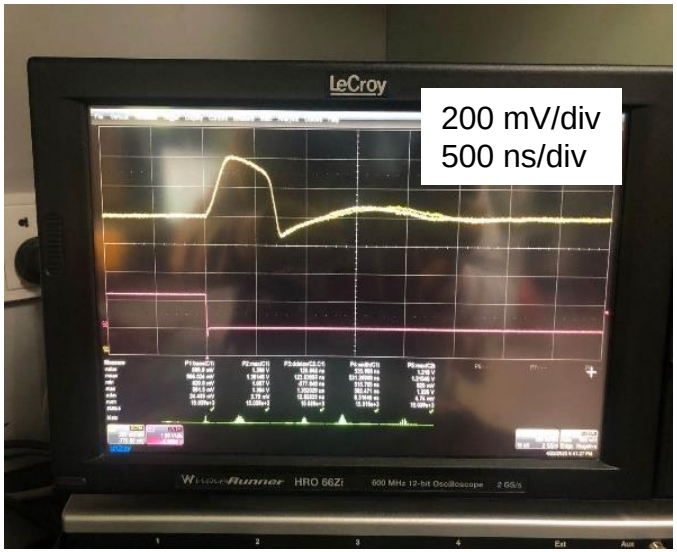
- **Measured different pixels**

Pixel selected	Min-DeltaV [mV]	ENC*	Vth [mV]	Sector
Pix0 of Col<2>	20	5 e-	130	1
Pix0 of Col<6>	20	5 e-	130	1
Pix0 of Col<10>	20	5 e-	130	1
Pix0 of Col<14>	20	5 e-	130	1
Pix0 of Col<18>	20	5 e-	130	1
Pix0 of Col<22>	20	5 e-	130	1
Pix0 of Col<2>	20	5 e-	130	2
Pix0 of Col<6>	20	5 e-	130	2
Pix0 of Col<10>	20	5 e-	130	2
Pix0 of Col<14>	20	5 e-	130	2
Pix0 of Col<18>	20	5 e-	130	2
Pix0 of Col<22>	20	5 e-	130	2
Pix127 of Col<2>	20	5 e-	130	3
Pix127 of Col<6>	20	5 e-	130	3
Pix127 of Col<10>	20	5 e-	130	3
Pix127 of Col<14>	20	5 e-	130	3
Pix127 of Col<18>	20	5 e-	130	3
Pix127 of Col<22>	20	5 e-	130	3
Pix127 of Col<2>	20	5 e-	130	4
Pix127 of Col<6>	20	5 e-	130	4
Pix127 of Col<10>	20	5 e-	130	4
Pix127 of Col<14>	20	5 e-	130	4
Pix127 of Col<18>	20	5 e-	130	4

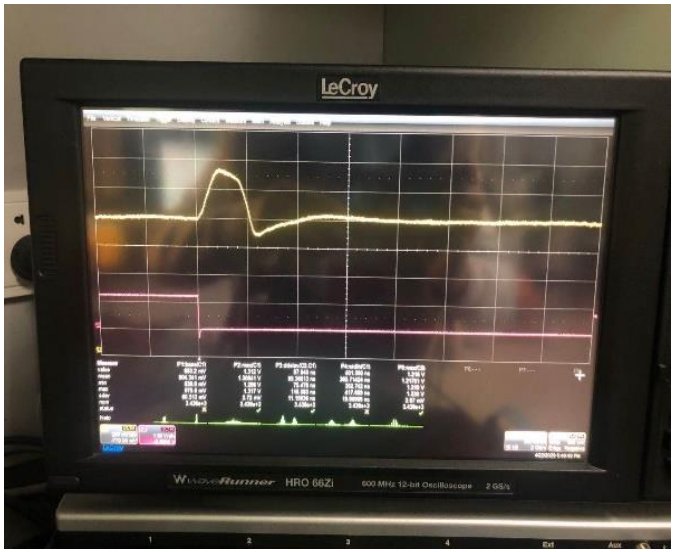
*Simulated voltage to charge factor 0.7 mV/e-

Chip #4 performance

- **Effect of VCLIP**
  - Lower VCLIP results in lower pulse duration, consistent with design



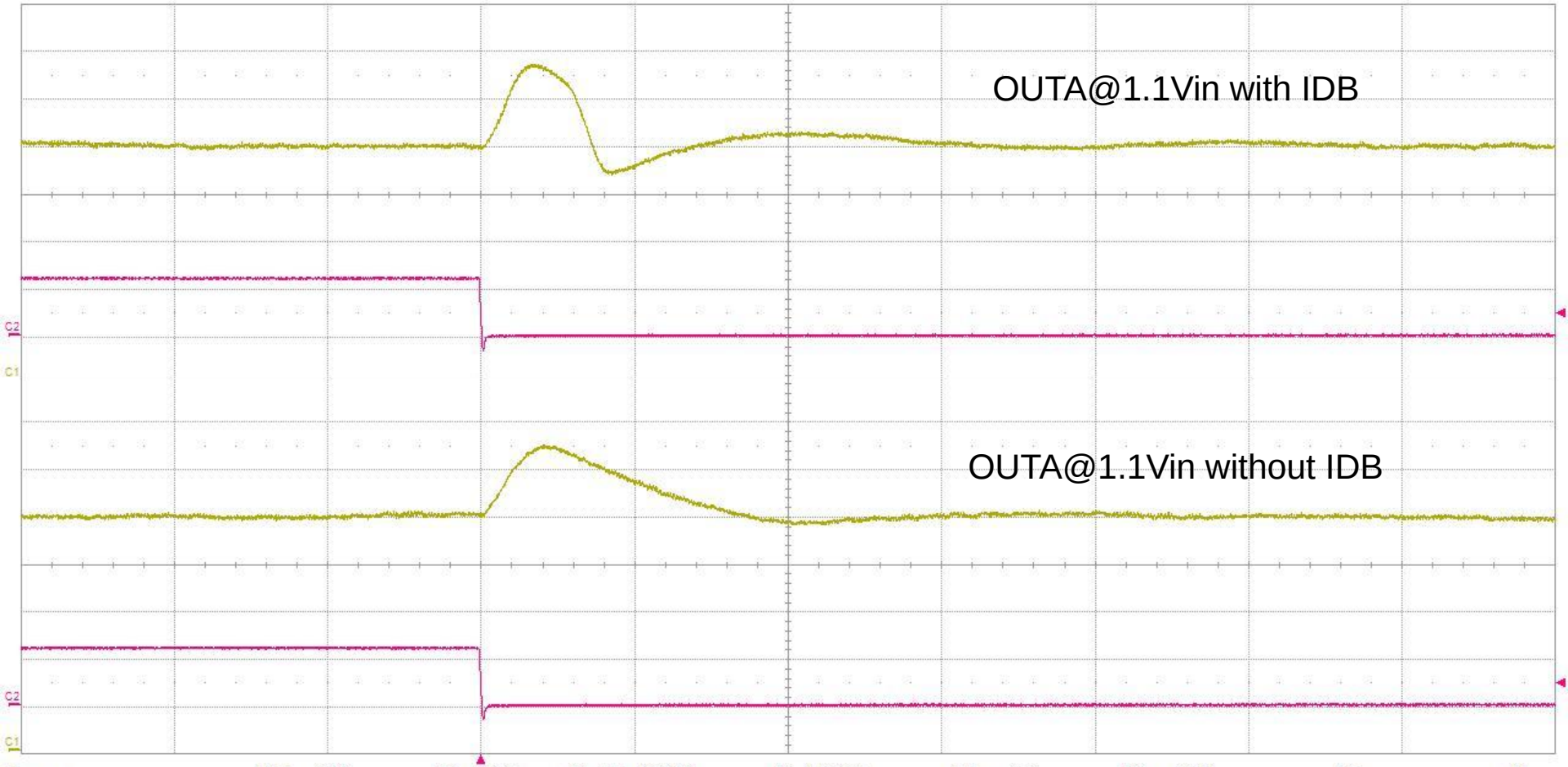
OUTA@VCLIP=0.18 V



OUTA@VCLIP=0.06 V

Chip #4 performance

- **Effect of IDB, unexpected performance**



Measure	P1:base(C1)	P2:max(C1)	P3:ddelay(C2,C1)	P4:width(C1)	P5:max(C2)	P6:ampl(C1)	P7:- - -	P8:- - -
value	946.3 mV	1.285 V	78.275 ns	467.025 ns	1.217 V	338.6 mV		
mean	877.379 mV	1.31938 V	65.14781 ns	308.56961 ns	1.21029 V	440.998 mV		
min	841.2 mV	957 mV	-1.162572 µs	225.112 ns	5 mV	32.7 mV		
max	990.3 mV	1.342 V	2.848125 µs	4.410583 µs	1.231 V	486.6 mV		
sdev	40.491 mV	20.34 mV	13.62666 ns	79.10132 ns	69.49 mV	59.130 mV		
num	77.812e+3	77.812e+3	77.545e+3	78.111e+3	77.852e+3	77.812e+3		
status		✔	✔		✔			
histo								

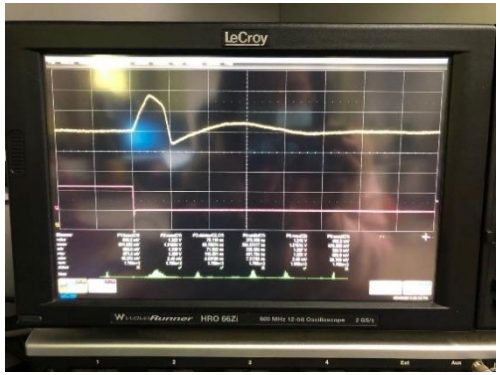
Chip #4 performance

- **Response to different injected inputs**
  - Delay of analog output increases with input signal decreasing. The trend is consistent with design, but much slower than design @IBIAS = 440 nA (IBIAS=280 nA in the measurements)

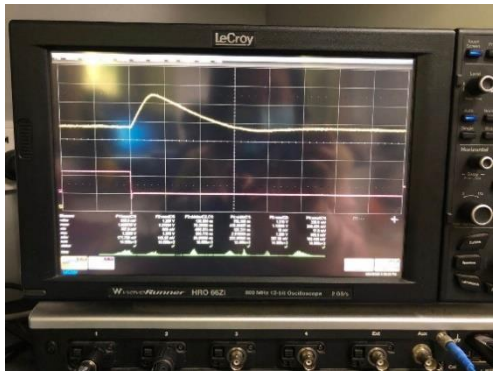
DeltaVin[V]	OUTA_dc (V)	OUTA_max (V)	Vsig (V)	Ddelay (ns)	WidthOUTA (ns)
1.3	0.836	1.337	0.501	59	234
1.1	0.836	1.332	0.496	63	233
0.9	0.842	1.327	0.485	71	232
0.7	0.865	1.319	0.454	86	228
0.5	0.872	1.313	0.441	117	222
0.3	0.884	1.308	0.424	190	215
0.25	0.884	1.306	0.422	217	214
0.2	0.859	1.302	0.443	247	214
0.15	0.859	1.300	0.441	279	212
0.13	0.855	1.300	0.445	290	213

Chip #4 performance

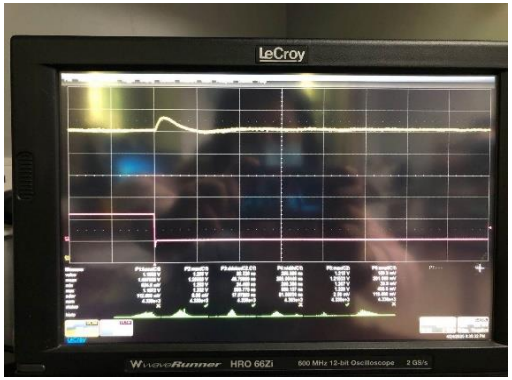
- **Response to injected input at different VPWELL with same biasing**



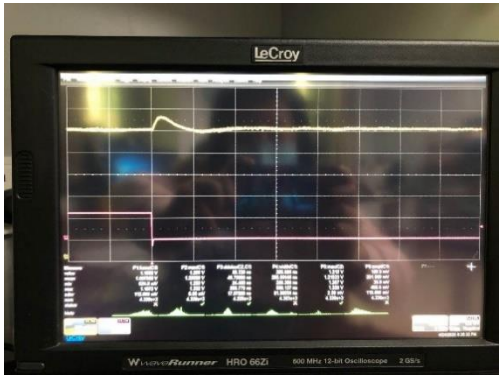
VPWELL=0.026 V



VPWELL=0.484 V



VPWELL=1.506 V



VPWELL=1.998 V

- **Front-end can work with negative VPWELL, but DACs need to be re-configured to provide right biasing**

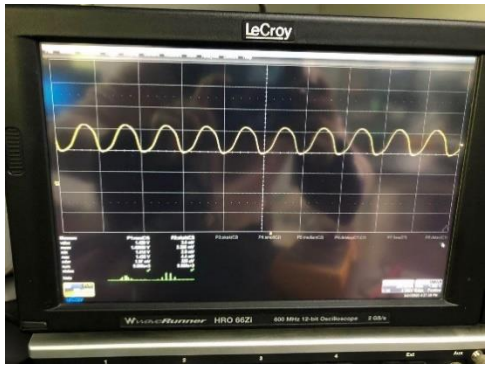
Chip #2 performance

- **VBG=0.45 V (stable, no oscillation observed)**
- **Output range of CDACs (current DACs) ~10 times lower than design**
  - ITHR can NOT reach the desired value for pixel

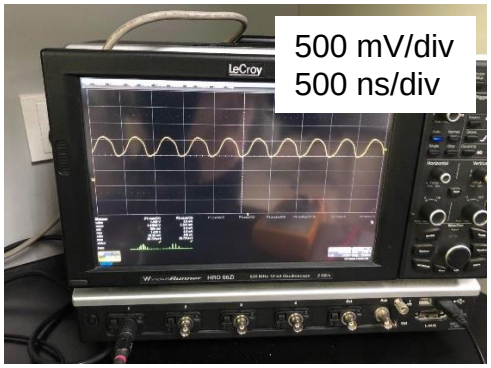
    max. = 2.4 nA, nominal 4.5 nA, but should be **enough for pixel work functionally**
  - Monitored ITHR is 400 times of the ITHR for pixel (2.4 nA = measured value/400)
- **Output range of VDACs (voltage DACs) of around half of the design**
  - Satisfy the required voltage bias
- **Different output with same input code for DACs, especially CDACs**
- **Analog front-end has NO response to the injection APULSE, with many sets of bias configurations and with covered chip**
- **Chip #2 responses to light**

Chip #2 performance

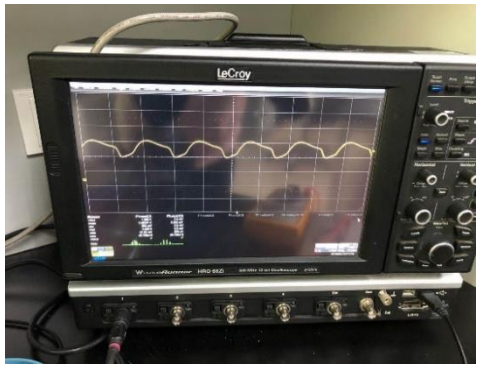
- **Chip #2 responses to light**
  - **Periodic signal observed when the chip is not fully covered**
  - **Analog responses have different frequencies depending on the sensor bias voltage (VRESET)**



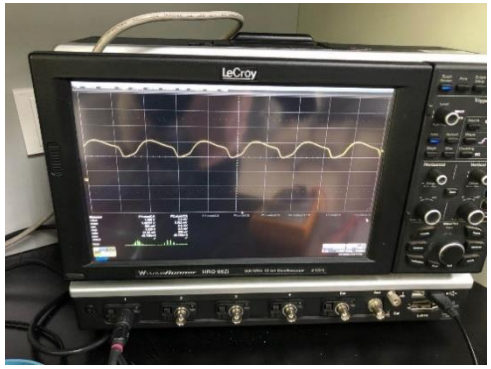
OUTA@VRESET=0.5 V



OUTA@VRESET=0.8 V



OUTA@VRESET=0.9 V



OUTA@VRESET=1.0 V

OUTA@VRESET=1.1 V

Frequency of OUTA decreases with VRESET increasing

VRESET and light-induced current affect the input voltage of front-end, and thus the working condition