Simulation of dynamic DFFs and Latches

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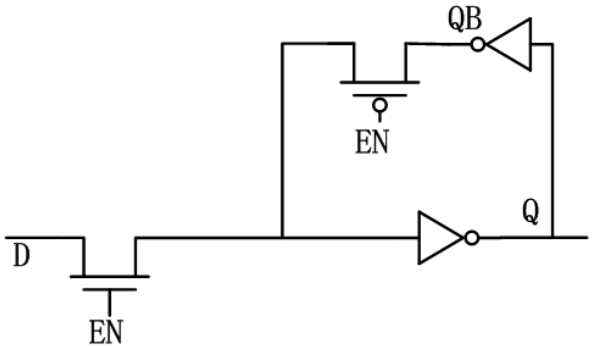
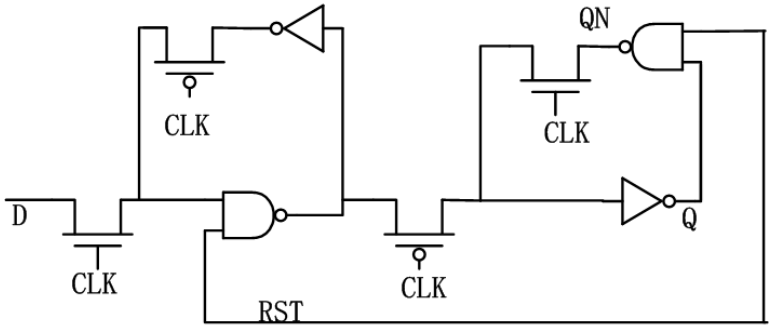
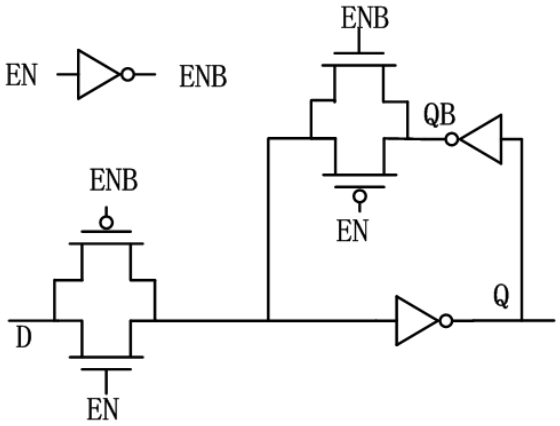
4 types dynamic DFFs in Pixel



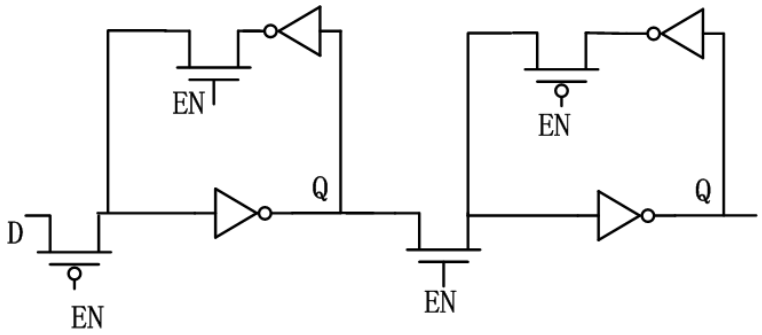
Type1: In pixel Latch for masking and calibration



Type3: ALPIDE like scheme in pixel DFF



Type2: EoC Latch for address stabilization



Type4: FE-I3 like scheme in pixel DFF and Shifting register Chain.

Setup &Hold time of Standard cell

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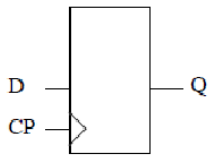
TOWERJAZZ We build more than wafers. We build trust.

Standard Cell Libraries

D Flip-Flops with Q Output Only

DFNRQ1, DFNRQ2 AND DFNRQ4

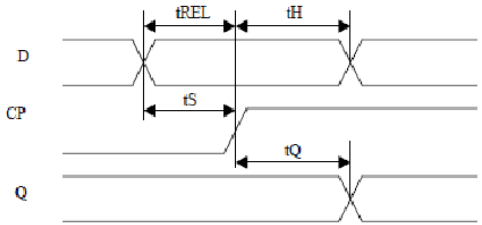
The DFNRQ1 (1x drive), DFNRQ2 (2x drive) and DFNRQ4 (4x drive) cells are positive edge triggered D flip-flops. Data present at the D input is transferred to the Q output on the positive edge of the clock, CP.



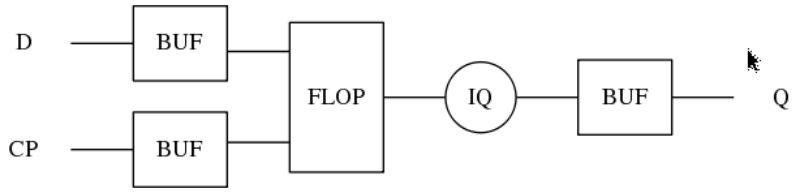
Function Table

INPUTS		OUTPUT
CP	D	Q
↑	L	L
↑	H	H
L	X	Q
H	X	Q

Waveforms



FUNCTIONAL SCHEMATIC



CONSTRAINTS

Constraint Pin	Related Pin	setup(ns)	hold(ns)
D(HL)	CP(LH)	0.1312	-0.0700
D(LH)	CP(LH)	0.1049	-0.0874

CONSTRAINTS 1.62V SS 125C

Constraint Pin	Related Pin	setup(ns)	hold(ns)
D(HL)	CP(LH)	0.2186	-0.1224
D(LH)	CP(LH)	0.1749	-0.1399

CONSTRAINTS 1.65V FF 40C

Constraint Pin	Related Pin	setup(ns)	hold(ns)
D(HL)	CP(LH)	0.0874	-0.0350
D(LH)	CP(LH)	0.0874	-0.0699

From the technical documents of TowerJazz, we can find the hold time and setup time parameters of a standard DFF in different corners.

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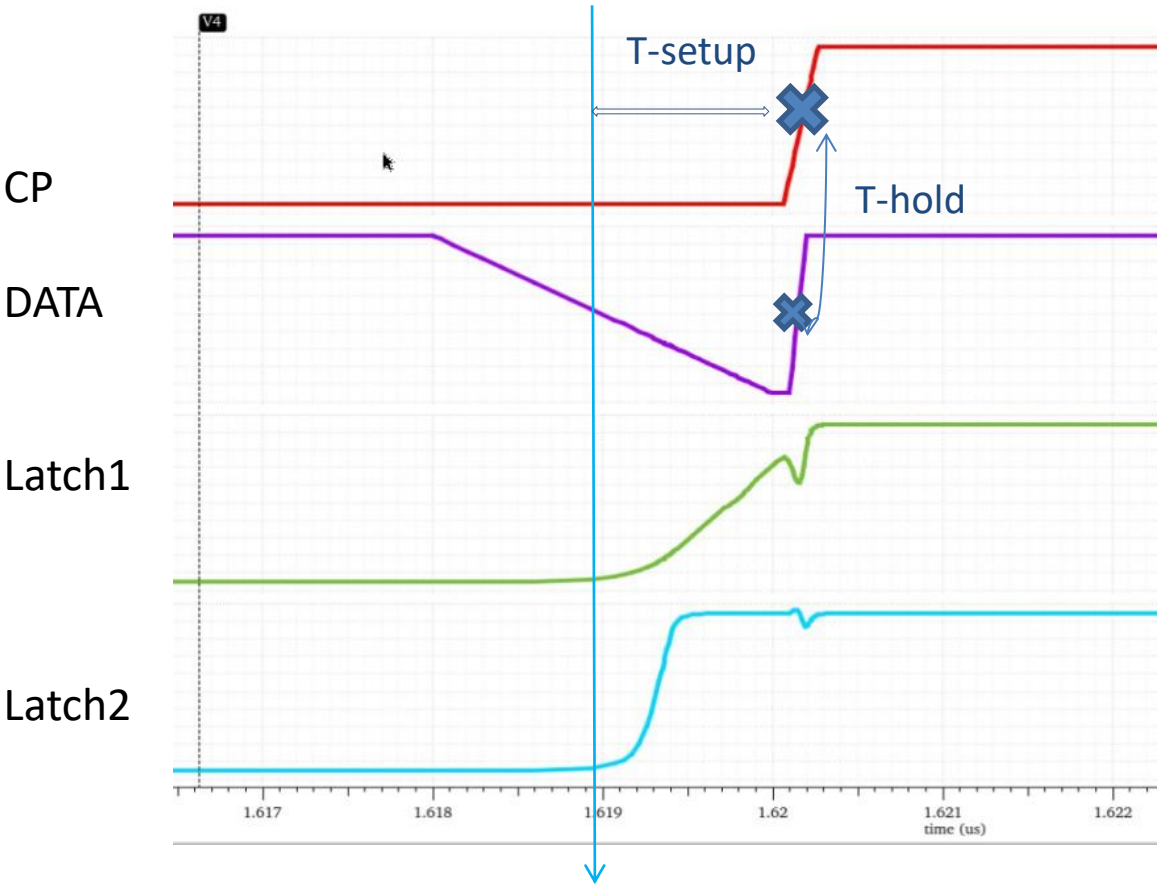
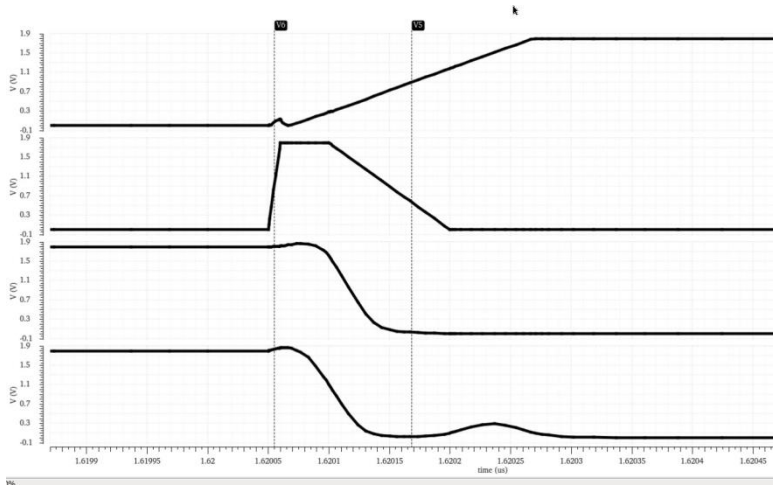
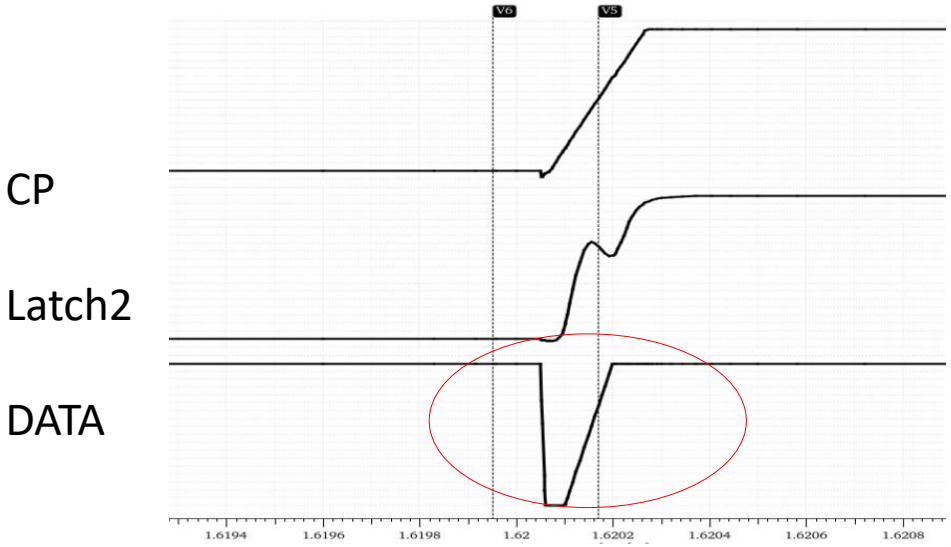
Schematic simulation result



- The minimum value of T-hold will be arriving before the rising edge of CLOCK.
- Latch1 shows the curve of half transmission gate and Latch2 is for full gate.
- The delay difference between two latches is 0.73ns here.

Schematic simulation result





- When the data is changed from LOW to HIGH, the delay difference between two latches is almost 0.
- The approach I used to measure the setup &hold time as you can see the figure below. I tuned the small window of the DATA to be the input and check the output of the Latch.

Schematic level simulation

	Setup time (ns)			Hold time(ns)		
Types	TT 1.8V 27℃	FF 1.6V 50℃	SS 1.6V 50℃	TT 1.8V 27℃	FF 1.6V 50℃	SS 1.6V 50℃
Type1(half)	1.07	0.97	3.17	0.08	-0.01	-0.013
Type2(full)	0.12	0.10	0.67	-0.01	-0.01	-0.02
Type3(with RST)	1.17	0.37	1.17	-0.02	-0.01	-0.12
Type4 (DFF)	1.7	1.17	3.67	-0.02	-0.02	-0.18

- The delay of half transmission gate setup time is obviously bigger than full one.
- There is no much difference of the minimum hold time of different Latches
- The Type3 DFF is active by the falling edge of CLK, is better than rising edge DFF.
- The worst setup time of DFF is 3.67ns.

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Thanks for your attention.

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