Progress of Vertex Detector Design

Zhijun Liang

VERTEX DETECTOR FOR CEPC

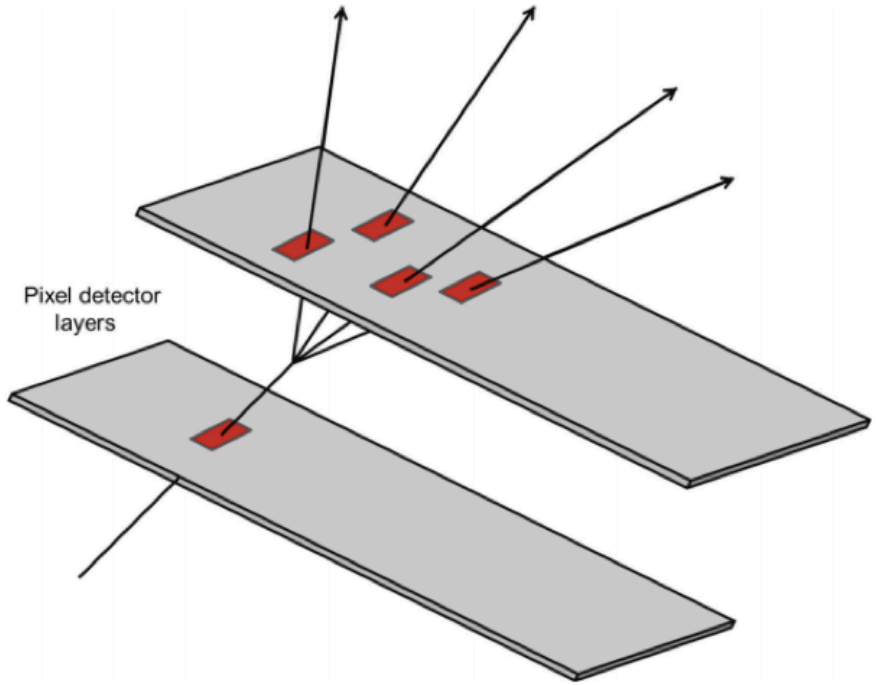
- High precision vertex detector essential for H→bb/cc/gg and H→ττ

- Single point resolution < 3 μm → Vibration need to be control to μm level
- Radiation tolerance **(per year):** 1 MRad &2×10^{12} 1 MeV n_{eq}/cm^2
- Material budget： <0.15%X_0 per layer
- Power consumption: < 50 mW/cm^2 layer ， temperature <30 ℃
- B layer radius : As close to the beam pipe as possible

MDI related

- Fast readout time: <500ns @40MHz at Z pole

$$\sigma_{r\varphi} = 3\ \mu m \oplus \frac{10\ \mu m}{p(\mathrm{GeV}) \cdot \sin^{3/2}\theta}$$

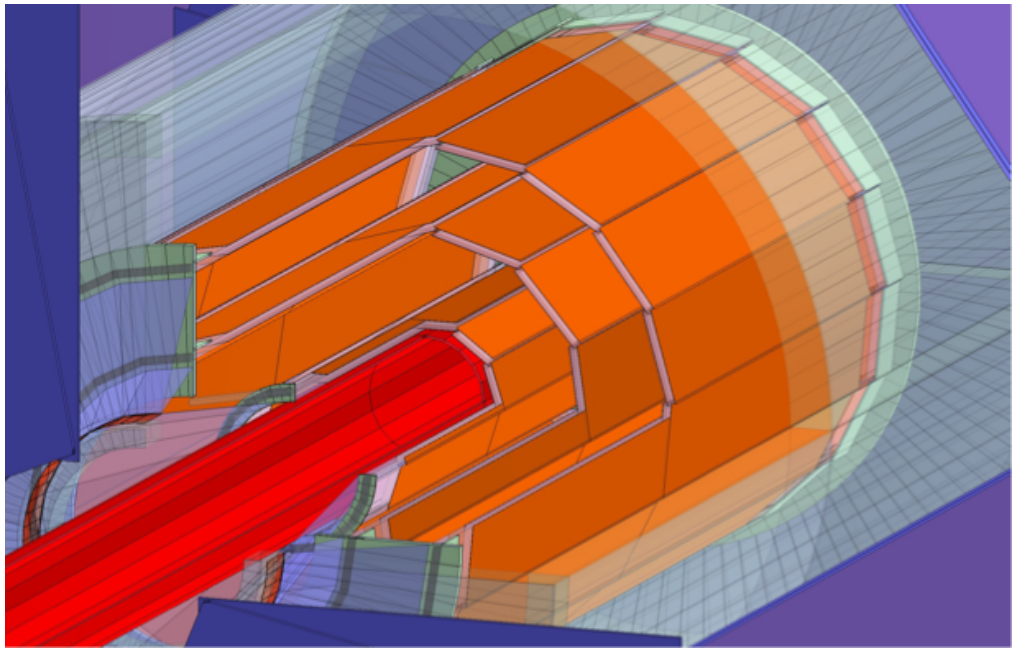


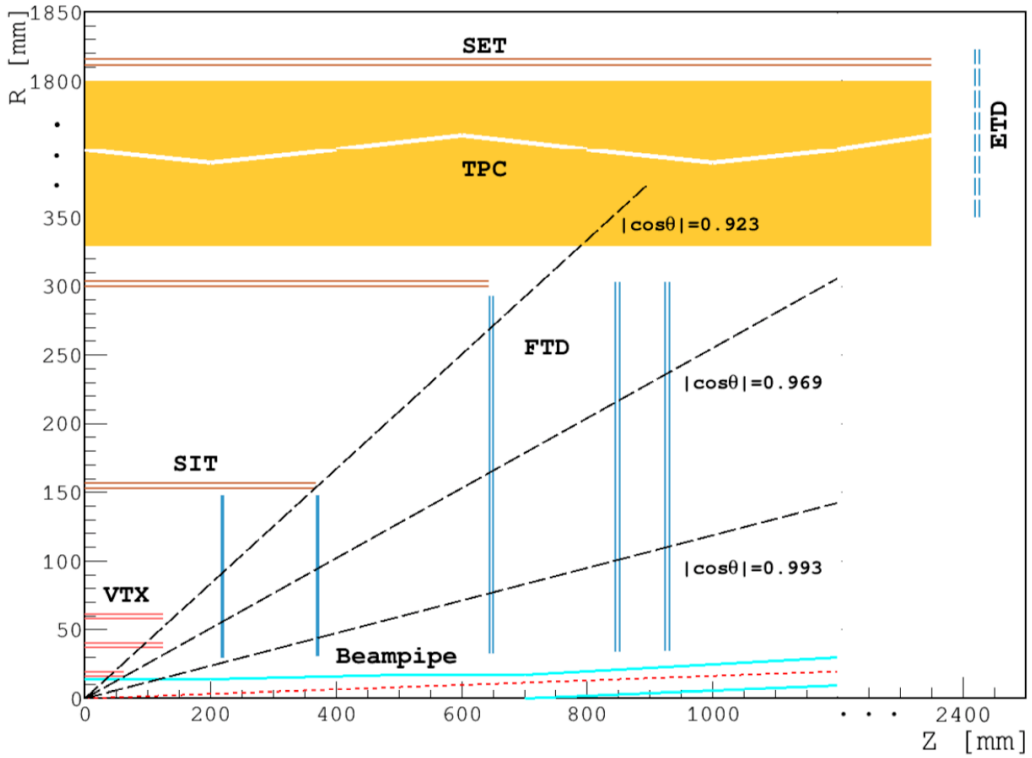
Vertex Detector Concept in CEPC CDR

- Vertex detector in CDR
  - Three double layer Barrel + Endcap disk
- Towards TDR (need engineering design)
  - Need support structure
  - Need to consider cooling
  - Need to handle cabling and other service

Main focus in this workshop

	R (mm)	$\|z\|$ (mm)	$\|\cos\theta\|$	$\sigma(\mu m)$
Layer 1	16	62.5	0.97	2.8
Layer 2	18	62.5	0.96	6
Layer 3	37	125.0	0.96	4
Layer 4	39	125.0	0.95	4
Layer 5	58	125.0	0.91	4
Layer 6	60	125.0	0.90	4

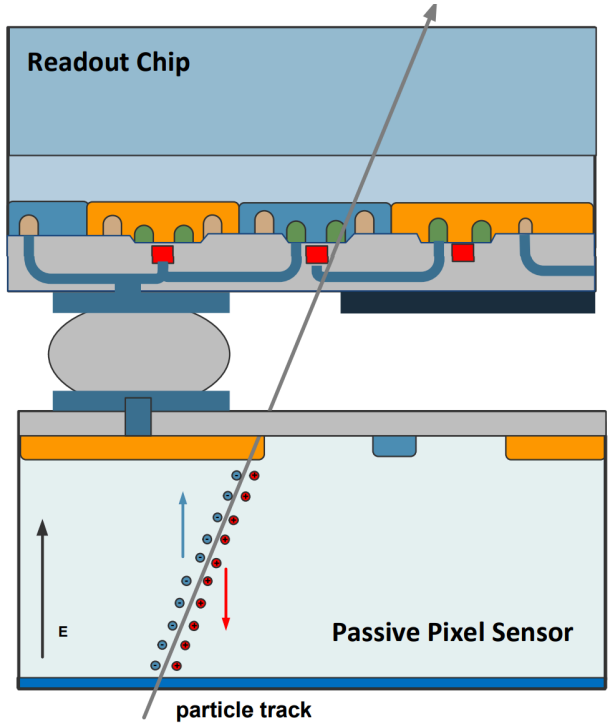




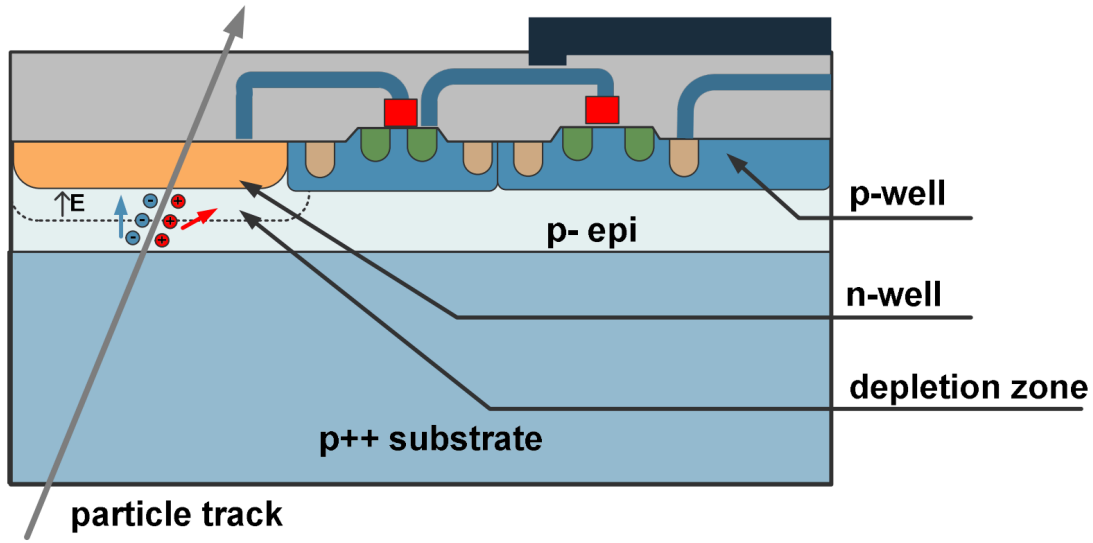
CMOS PIXEL SENSOR

- Monolithic pixel (CMOS imaging CIS process or SOI process) is ideal for CEPC application
  - low material budget (can be thin down to 50μm)
  - Material budget is about 5-10 times smaller than Hybrid pixel technology
  - Lots of development on going: Jadepix and Taichu chip…

Hybrid pixel



Monolithic Pixels



Barrel Vertex detector machanism design

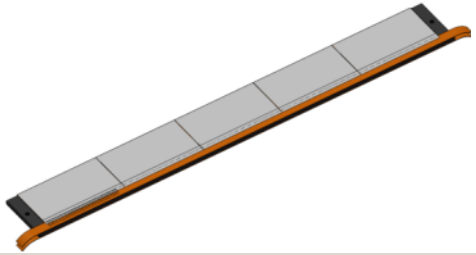
Engineering design on the ladder (module) of vertex detector and support structure.

Monolithic Sensor chip : 14.8 x 25.6 x 0.05 mm (not consider stitching yet)

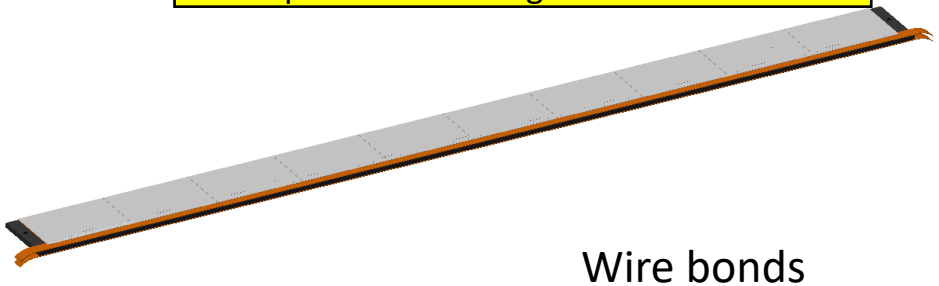
Ladder: support structure + chips + flexible PCB

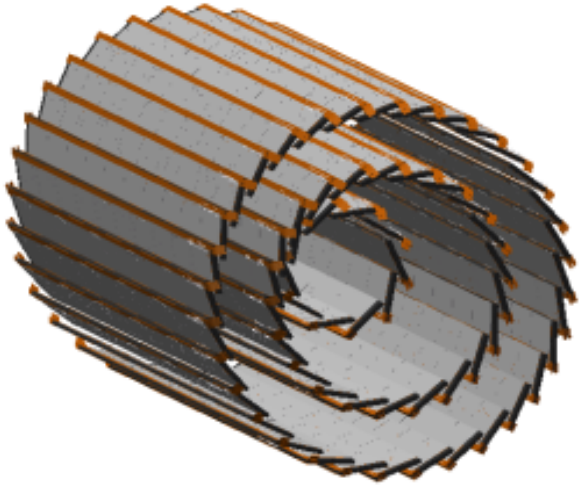
By Jinyu Fu

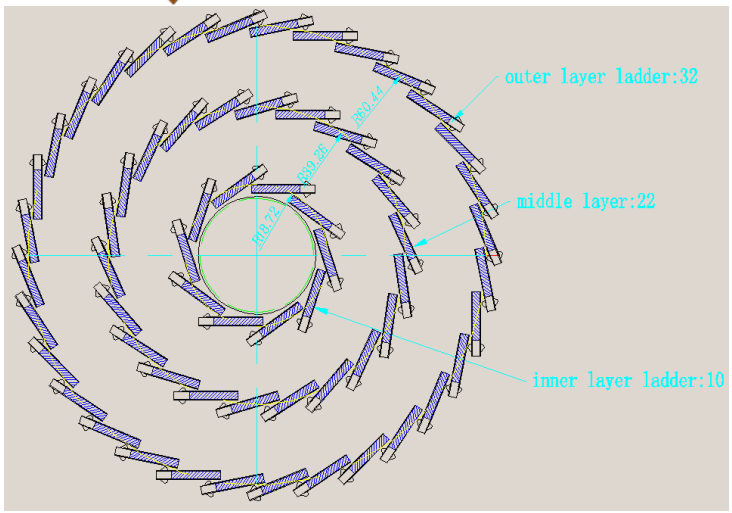
Ladder of inner layer(16.8 x 131 mm):
10 chips total including both sides



Ladder of outer two layers(16.8 x 264 mm):
20 chips total including both sides



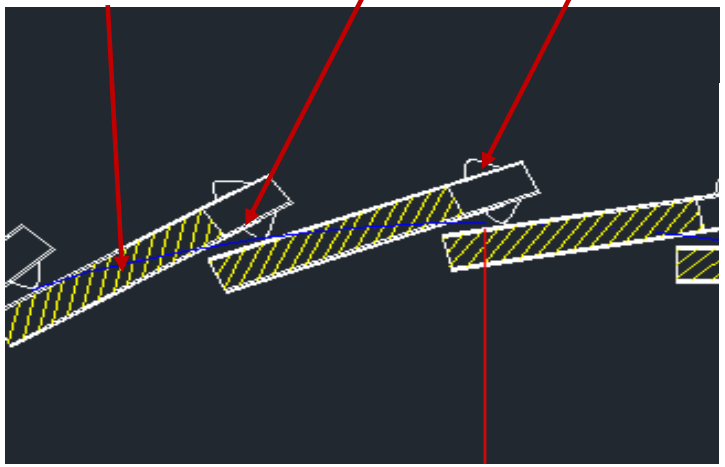


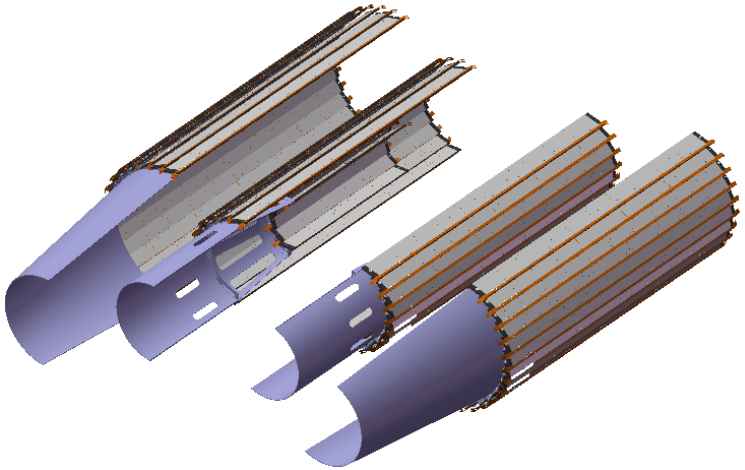


Active area

Dead area

Wire bonds

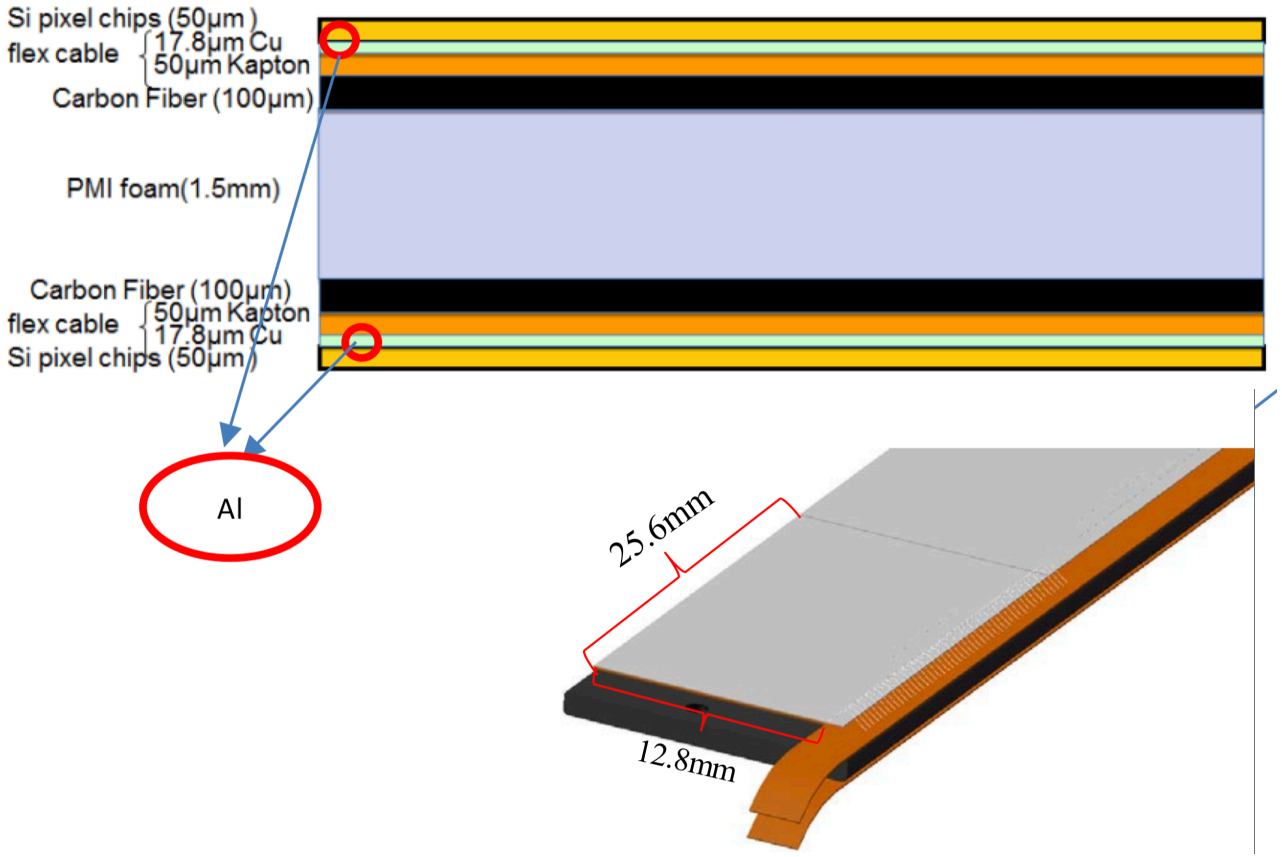


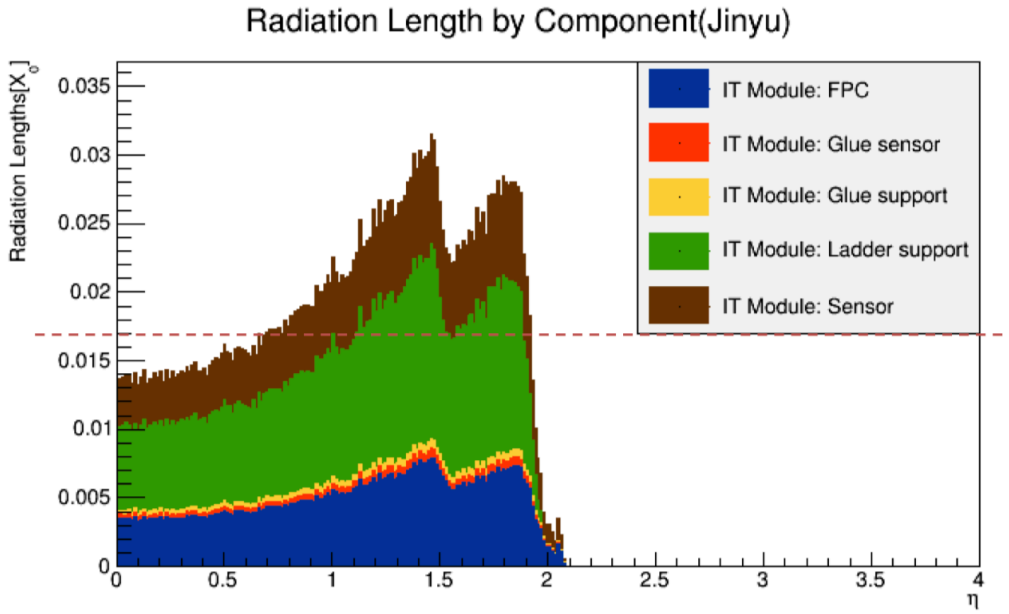


Vertex detector module

By Jinyu Fu & Mingyi Dong

- Requirement : Material budget 0.15%X_0 per layer
- First draft of CEPC vertex module design: double layer module
  - Monolithic silicon sensor(50μm)+ flex cable(18μm Aluminum trace) + Carbon fiber Support (100μm)
  - Material budget barely within 0.15 %X_0 per layer at small incident angle
  - Need to be rigid in air cooling. Need further optimization

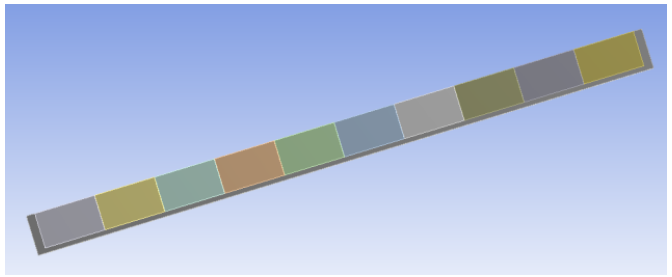


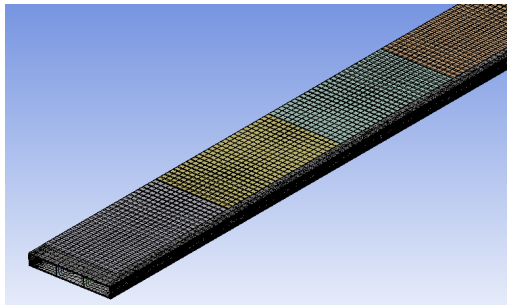


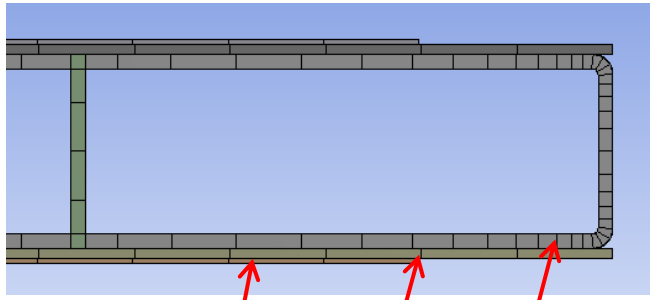
Rigidity of the ladder support structure

- Finite element simulation of the ladder model with the support with sensors and flexible PCB
  - Maximum deformation:4 μm (with 100 μm thin carbon fiber support)
- Need to simulate the dynamic vibration in air cooling in next step
- Need to find a balance between rigidity and low material budget
- Prototype of ladder support structure will be fabricated in a carbon fiber foundry.

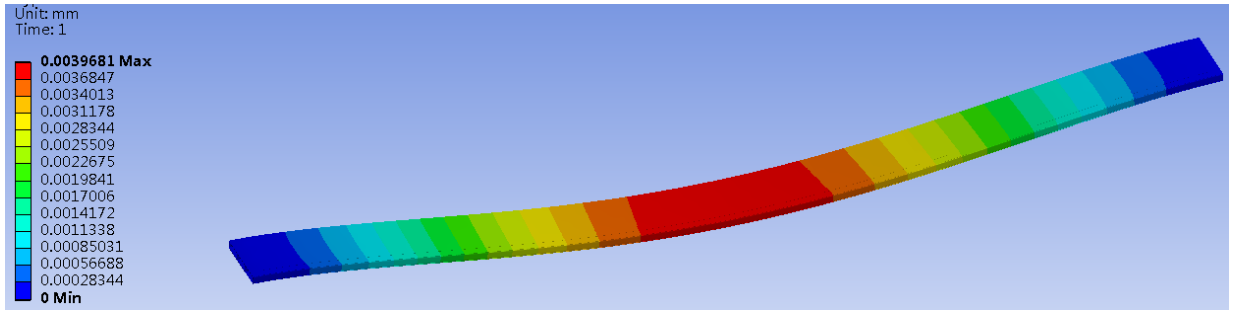
By Jinyu Fu







Max deformation: 4 μm



Material ： <0.15%X_0 per layer

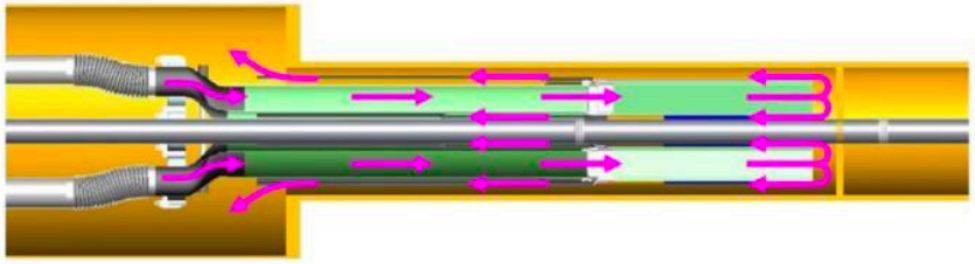
resolution < 3 μm

(vibration μm level)

After the flexible PCB with sensors glued on, the rigidity of the full ladder is increased by 24% compare to that of the support itself.

POWER CONSUMPTION AND COOLING

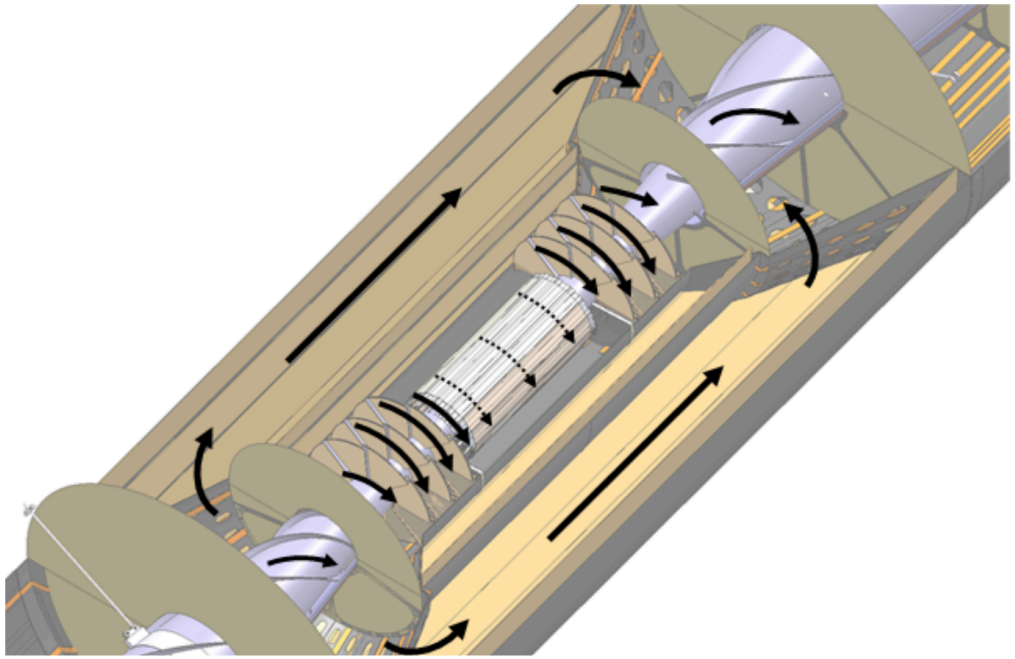
- To reduce material budget, air cooling is prefer in lepton collider
  - However CDR do not provide a path for the air to flow through the detector
  - Need engineering design
- How much power consumption can air cooling handle ?
  - Most of us consider the upper limit is about 10 mW/cm^2
  - Estimated power dissipation of vertex detector is ~50 mW/cm^2
  - Star HFT detector managed to cool 150 mW/cm^2
    - One of the key is without endcap disk in Star detector
    - Air flow can be much larger (10m/s) without endcap

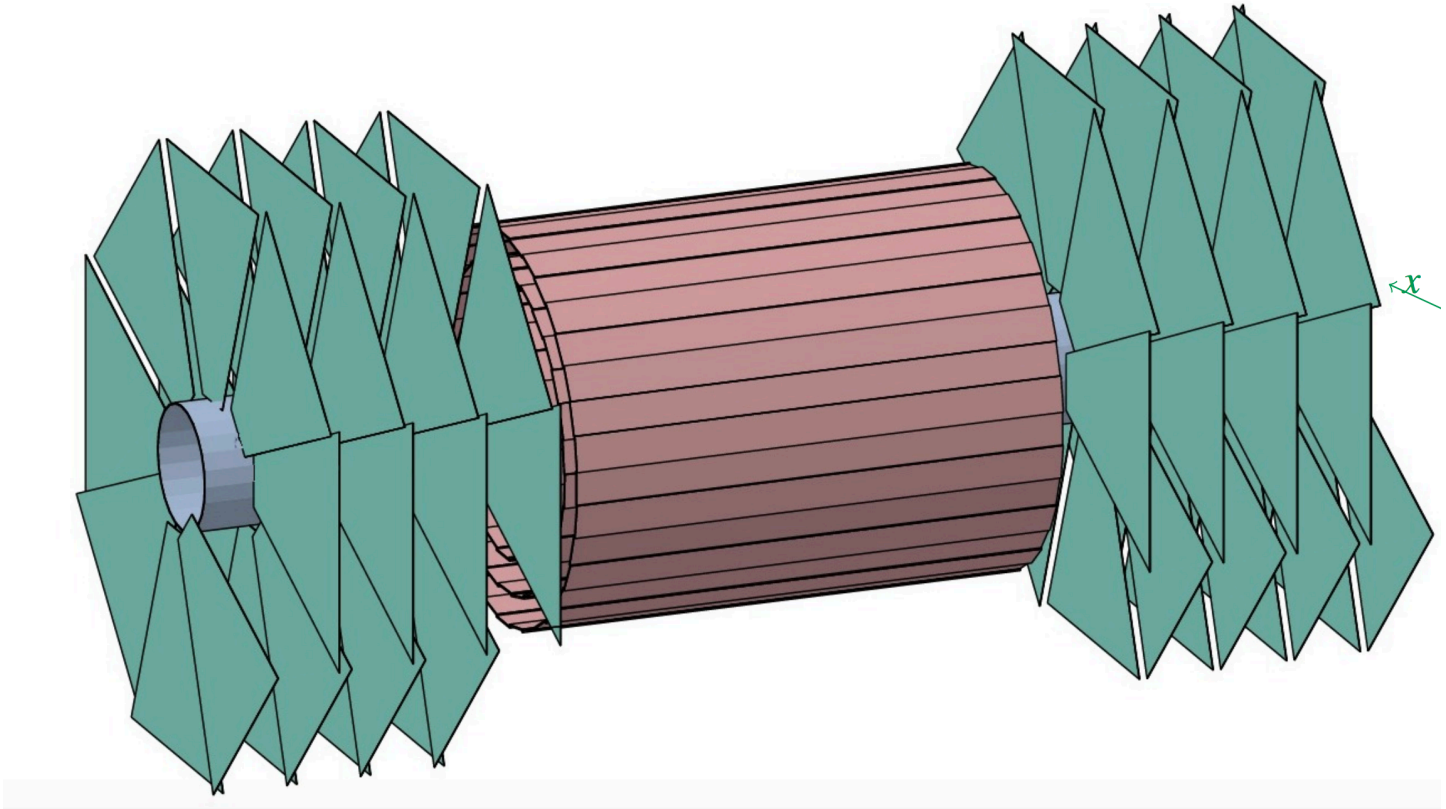


The STAR MAPS-based PiXeL Detector NIM, A 907 (2018) 60-80

POWER CONSUMPTION AND COOLING (2)

- CLIP proposed an concept of air cooling vertex detector with endcap (Spirals geometry)
  - Air cooling + power pulsing (20ms gap between bunch trains)

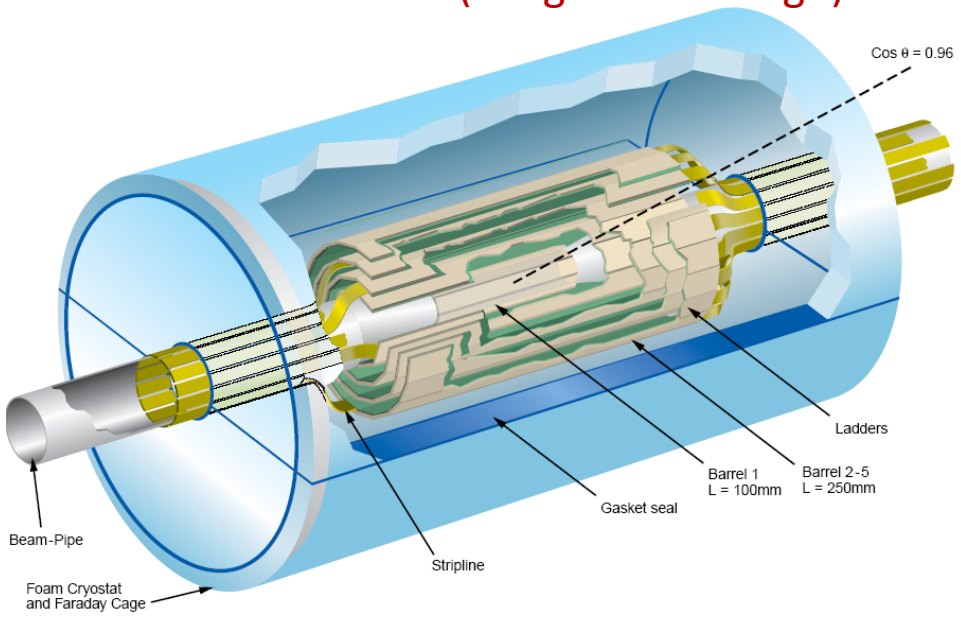




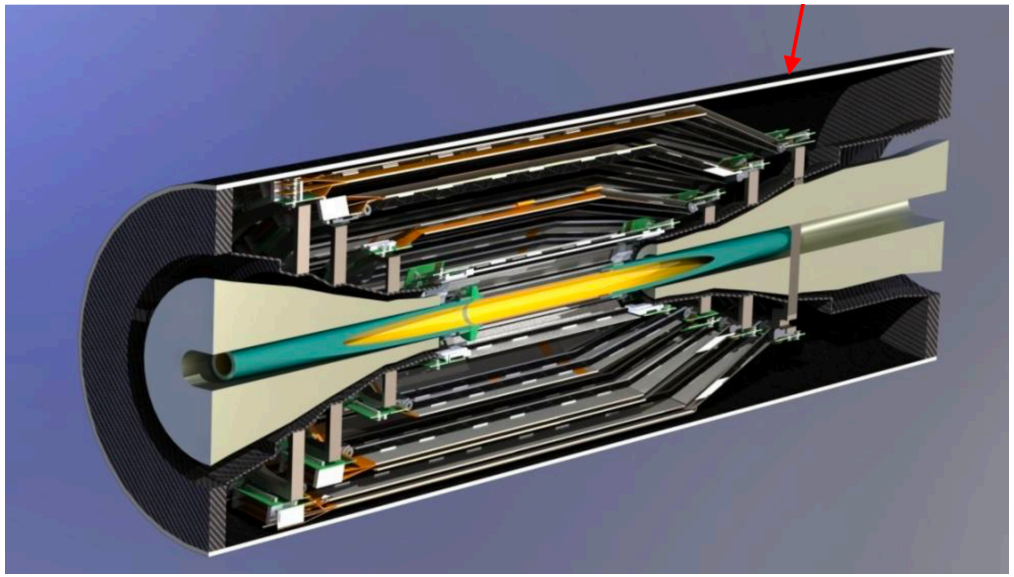
Interface between vertex detector and beam pipe

- Short barrel + endcap disk (air cooling)
  - CLIP Spirals concept
- Long barrel design
  - Star HFT detector (Barrel only , air cooling)
  - BELLE2 vertex detector (no endcap disk, air cooling)
  - SLD vertex detector (Long barrel, More details in Chris Damerell's talk yesterday)
- CEPC Vertex detector- beampipe interface :
  - Start engineering work with Long barrel design (Quan Ji)
  - Re-visit Short barrel + endcap disk after we gain enough experience

Star HFT vertex detector(Long barrel design)



BELLE2 vertex (no endcap disk)



VERTEX DETECTOR WITHOUT ENDCAP ? (LONG BARREL)

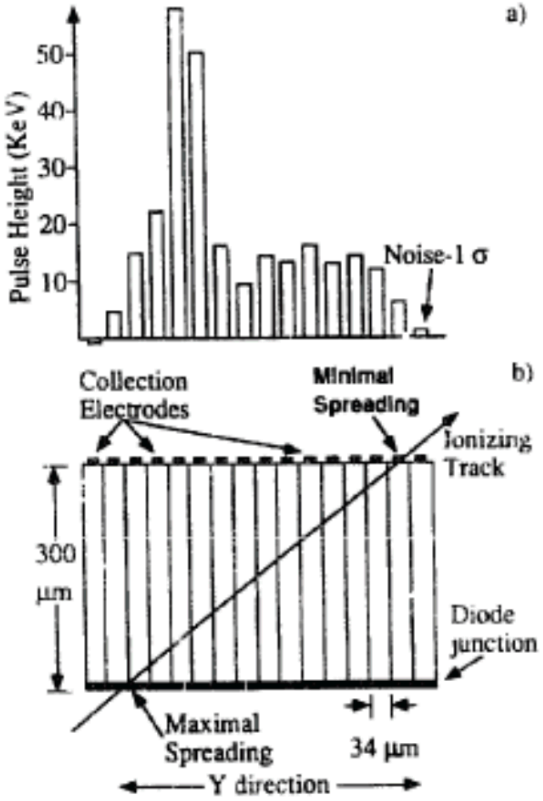
- CEPC Vertex detector- beampipe interface :
  - Start engineering work with Long barrel design (more in Quan Ji's talk)
  - Re-visit Short barrel + endcap disk after we gain enough experience

- Three double layer of long barrel silicon detector
  - ✓ Support by beampipe
  - ✓ More details in Quan's talk

By Quan Ji

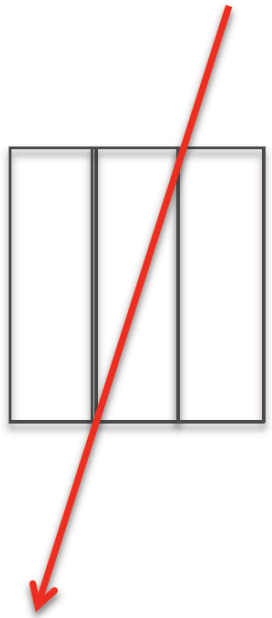
VERTEX DETECTOR WITHOUT ENDCAP ?

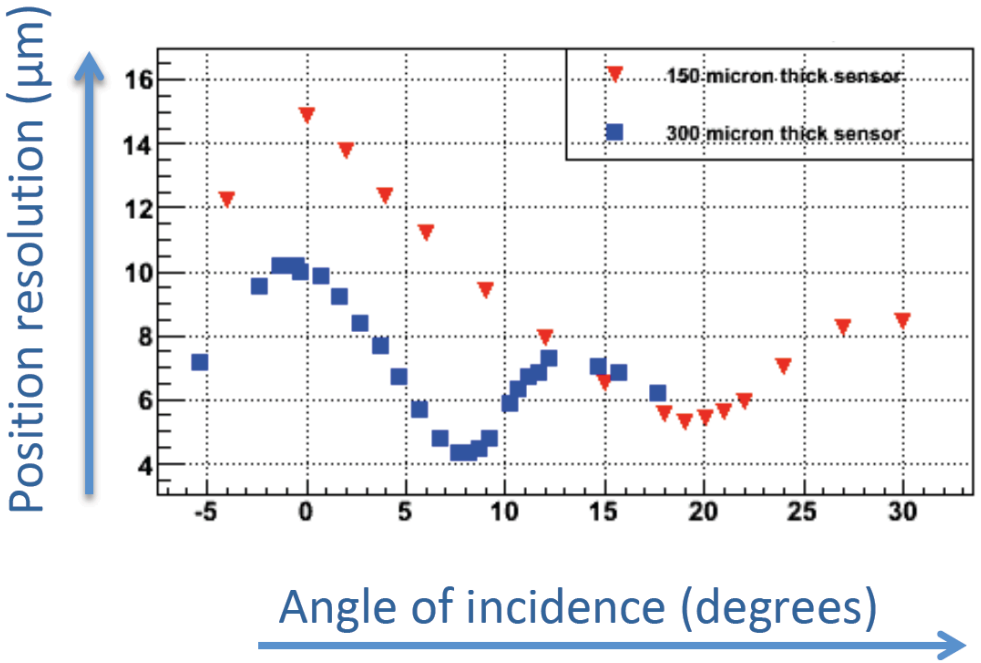
- Long barrel was not ideal in the past, with hybrid thick pixel sensor (300µm)
  - Charge sharing in small incident angle track help to improve resolution
  - Large incident angle track cause large charge sharing → low S/N



C. Kenney et al. NIM A 654 (2011) 258-265

Average of extreme pixels in the cluster gives better results
In this case the signal (and the S/N) for a single channel reduces with track inclination



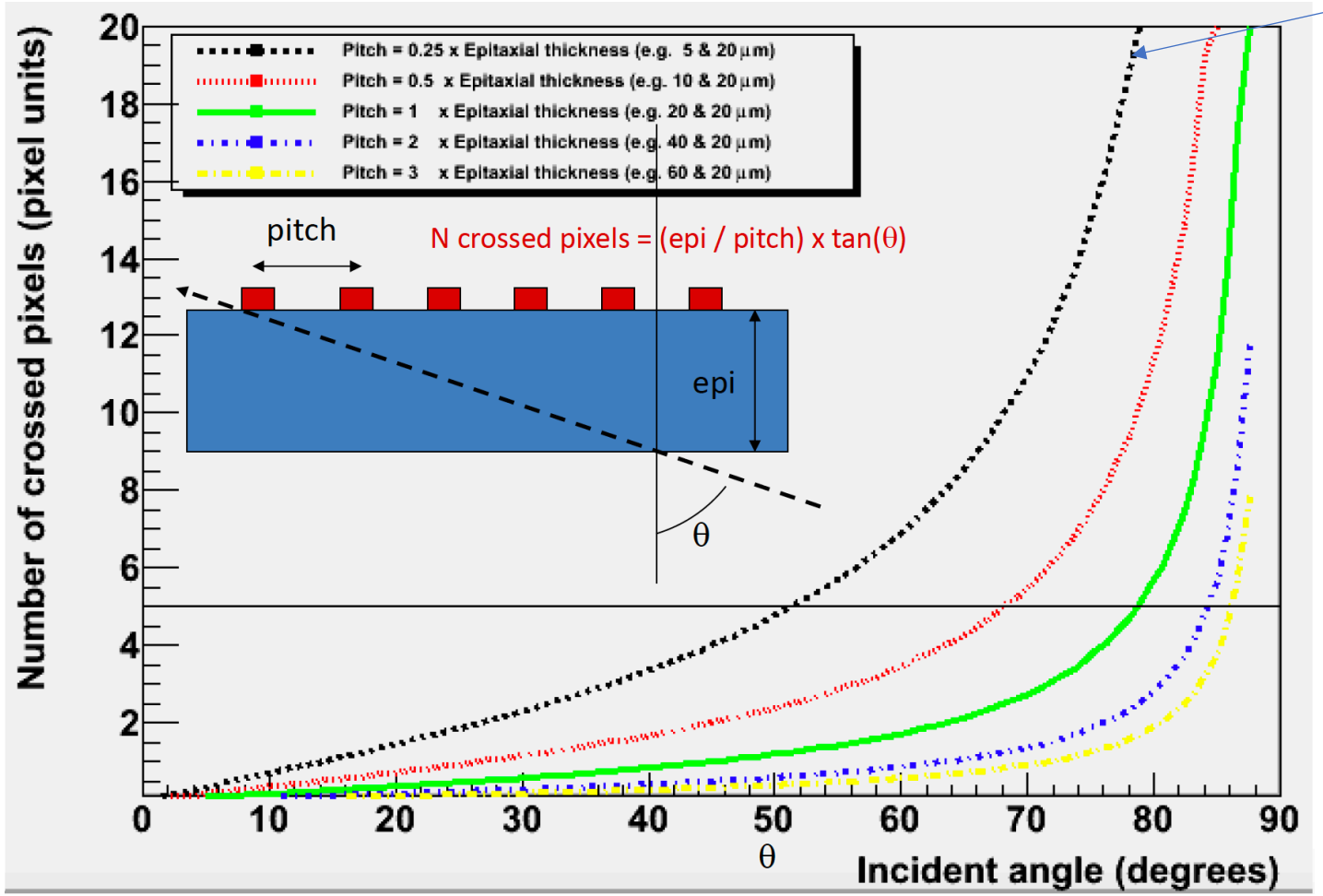


Timepix3: X. Llopart, J. Buytaert, M. Campbell, P. Collins et al.

Can optimize resolution using track inclination to enhance charge sharing, can also be done using a magnetic field

VERTEX DETECTOR WITHOUT ENDCAP ? (LONG BARREL)

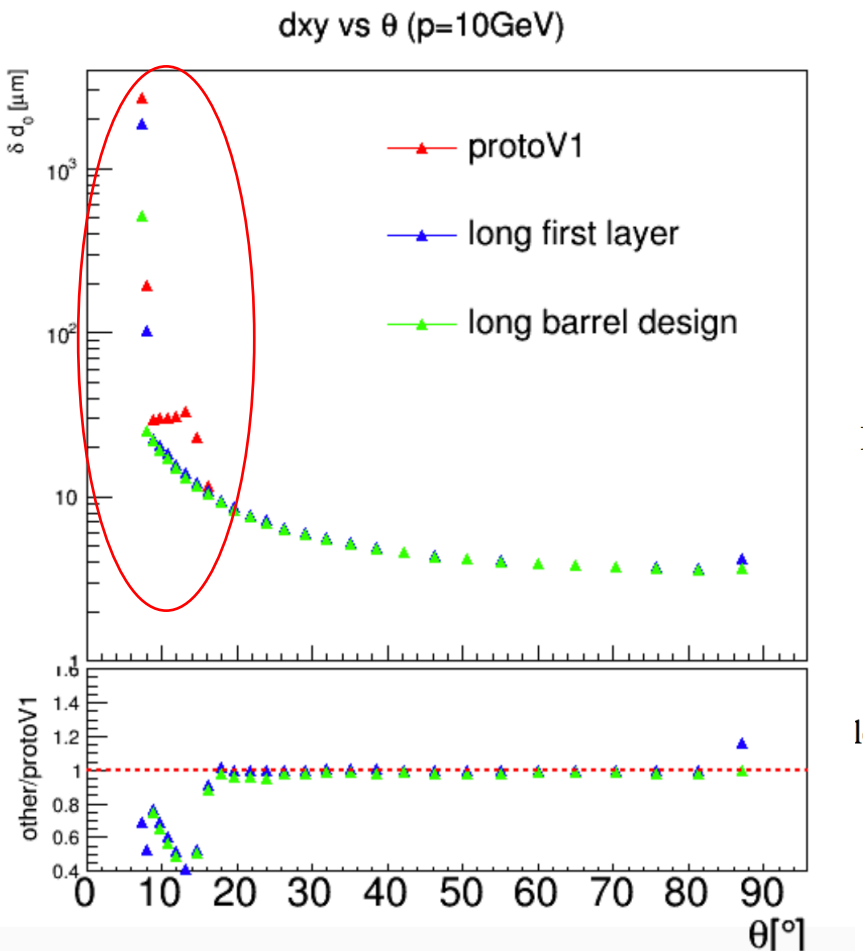
- Using thin CMOS pixel sensor, charge sharing effect is small
  - Cluster size and charge sharing can be control using thin active layer silicon
  - In-pixel amplifier in electronics improved S/N
  - No major technical issue of long barrel design



Preliminary study on long barrel performance

- Impact parameter resolution for few GeV track
  - Long barrel design (Green) compared to “short Barrel + endcap” (Red)
  - Slightly better in long barrel design , No visible shower stopper of long barrel design
  - More study and optimization to be done …

By Hao Zeng



Prototype V1

Layer	1	2	3	4	5	6
r	17.116	19.041	37.667	39.577	58.914	60.842
z_max	64.200	64.200	128.450	128.450	128.450	128.450

Disk	1	2
z	221.000	368.000

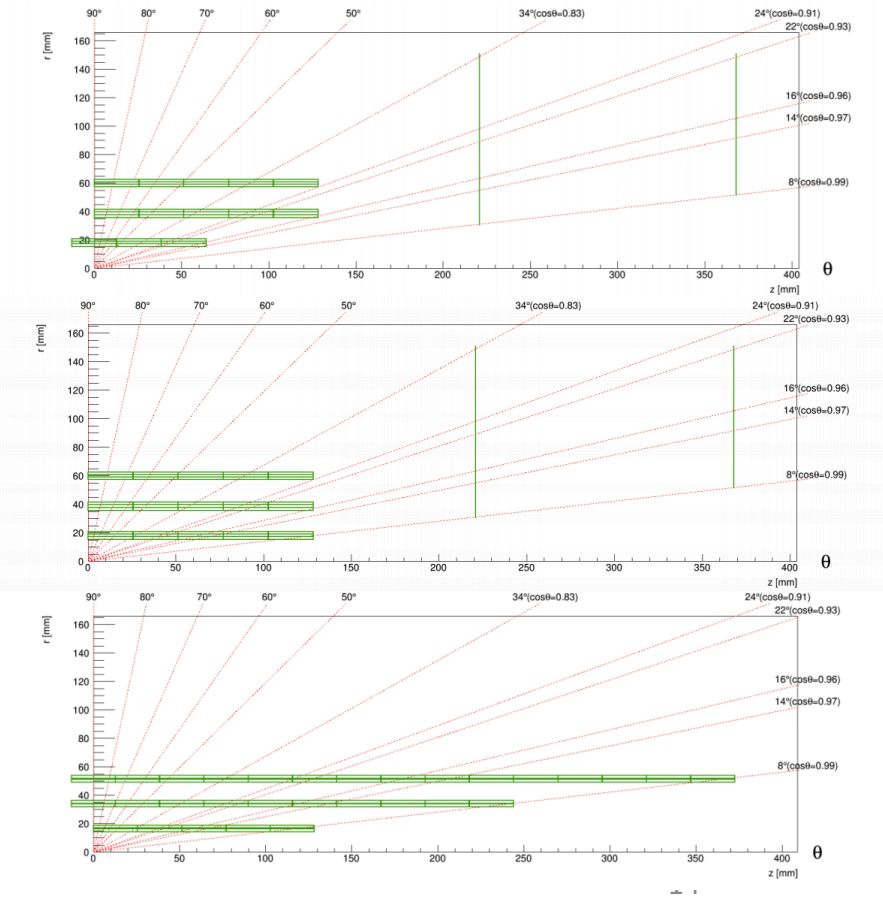
Longer first layer

Layer	1	2	3	4	5	6
r	17.116	19.041	37.667	39.577	58.914	60.842
z_max	128.450	128.450	128.450	128.450	128.450	128.450

Disk	1	2
z	221.000	368.000

long barrel design

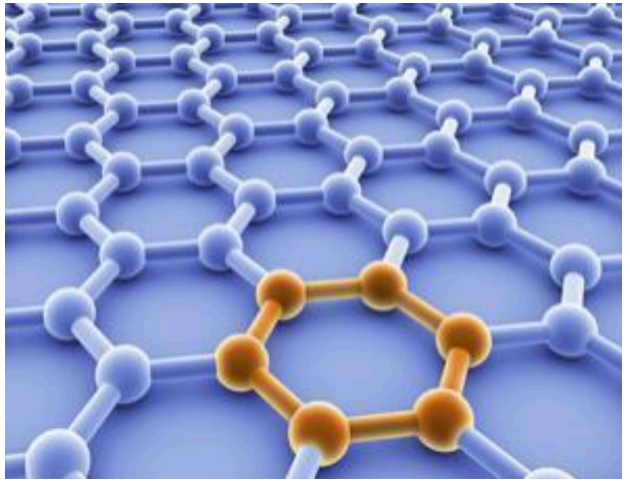
Layer	1	2	3	4	5	6
r	15.523	17.479	33.019	34.982	50.522	52.479
z_max	128.450	128.450	244.100	244.100	372.600	372.600



Thermal simulation

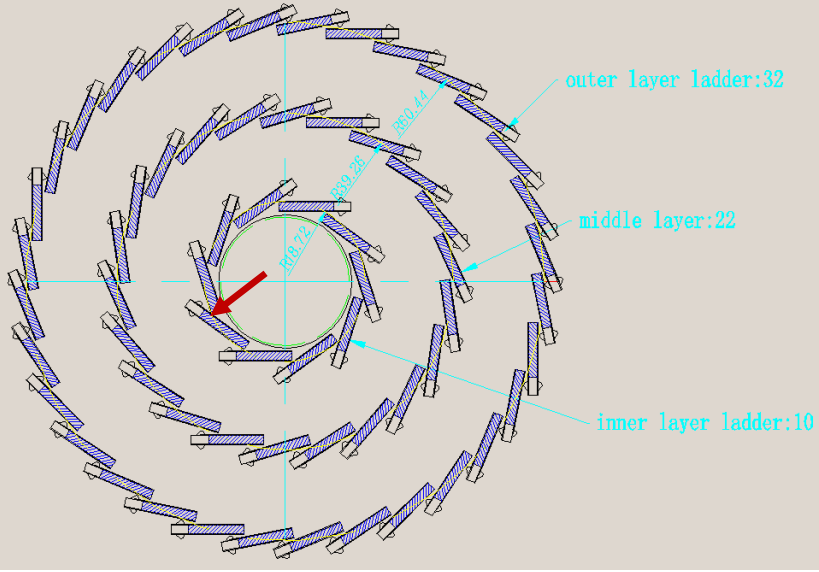
- Even using long barrel design with large Air flow
  - However, the temperature b layer of vertex detector is still high (>50 ℃)
  - Too close to beampipe (limited air flow)
  - New idea about new material (Graphene) (Quan's talk)
    - Much High heat conductivity compared to Carbon fiber
  - What is Limitation in air velocity ?
    - Star HFT detector manage to provide 10m/s air flow)

Graphene



Thermal simulation (By Jinyu Fu)

Power dissipation (mW/cm2)	Temperature of beam pipe's surface (℃)	Inlet air temperature (℃)	Inlet air velocity (m/s)	Max temperature of inner barrel (℃)	Max temperature of middle barrel (℃)	Max temperature of outer barrel (℃)
50	*30*	*0*	*2*	57.1	29.1	26.9
50	*30*	*0*	*3*	54.5	24.3	22.9
50	*30*	*0*	*4*	52.3	21.3	19.9

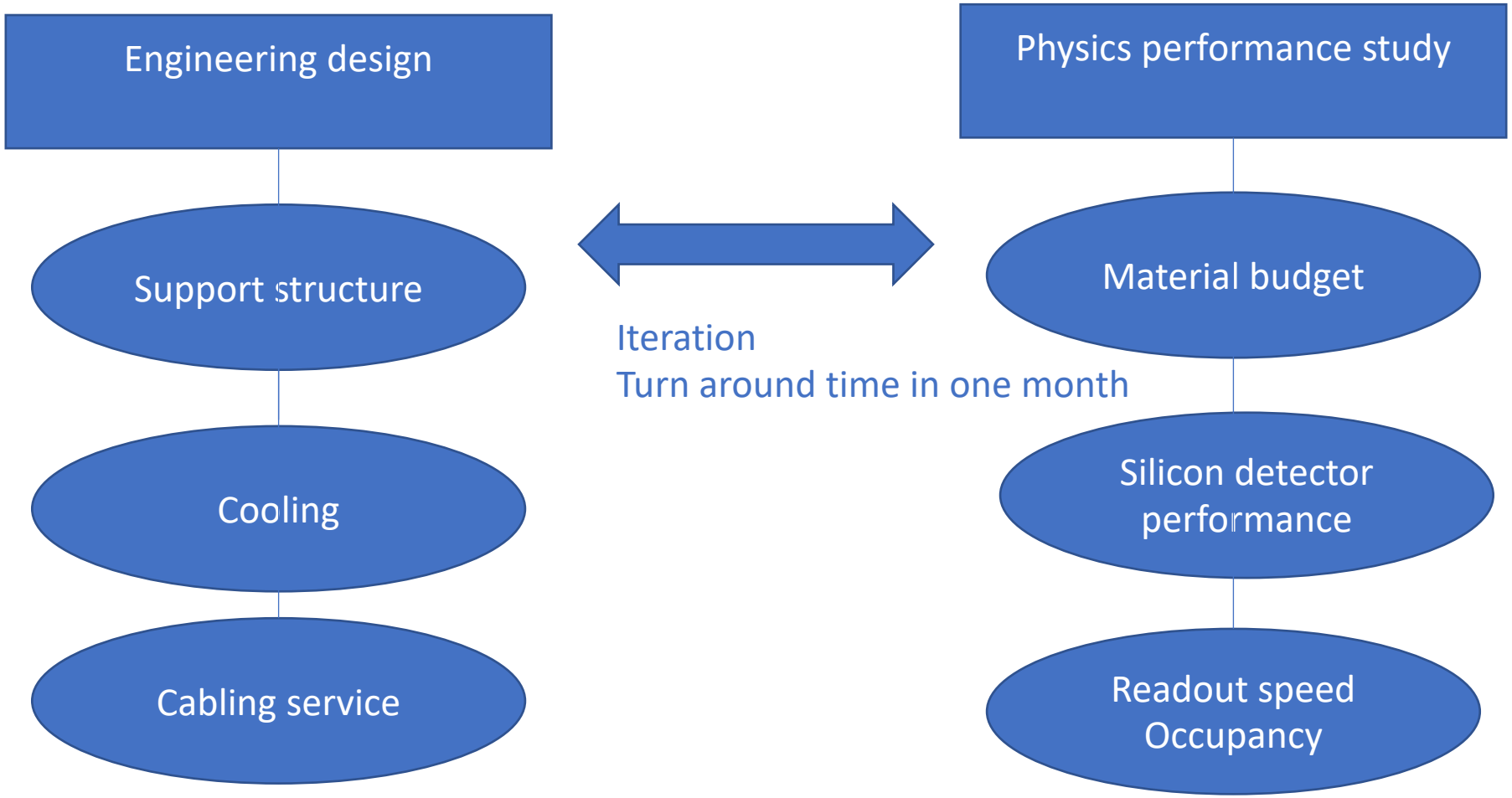


Power consumption: < 50 mW/cm^2 layer ,

temperature <30 ℃

Plan

- Start Iteration on Engineering optimization and physics performance optimization
  - A vertex-beampipe Layout version presented in Quan's talk today
  - Physics simulation and performance study to this layout in about one month
  - Invite more colleague to provide feedback to layout (tracker, Calo , physics impact)



Manpower, Funding

- Existing funding
  - CEPC MOST2 project (12M RMB)
    - ~0.5M for vertex detector support structure prototype
- Existing Manpower
  - Faculty: Jinyu Fu, Mingyi Dong, Gang Li , Zhijun Liang, Joao Costa
  - Student: Hao Zeng , Kewei Wu

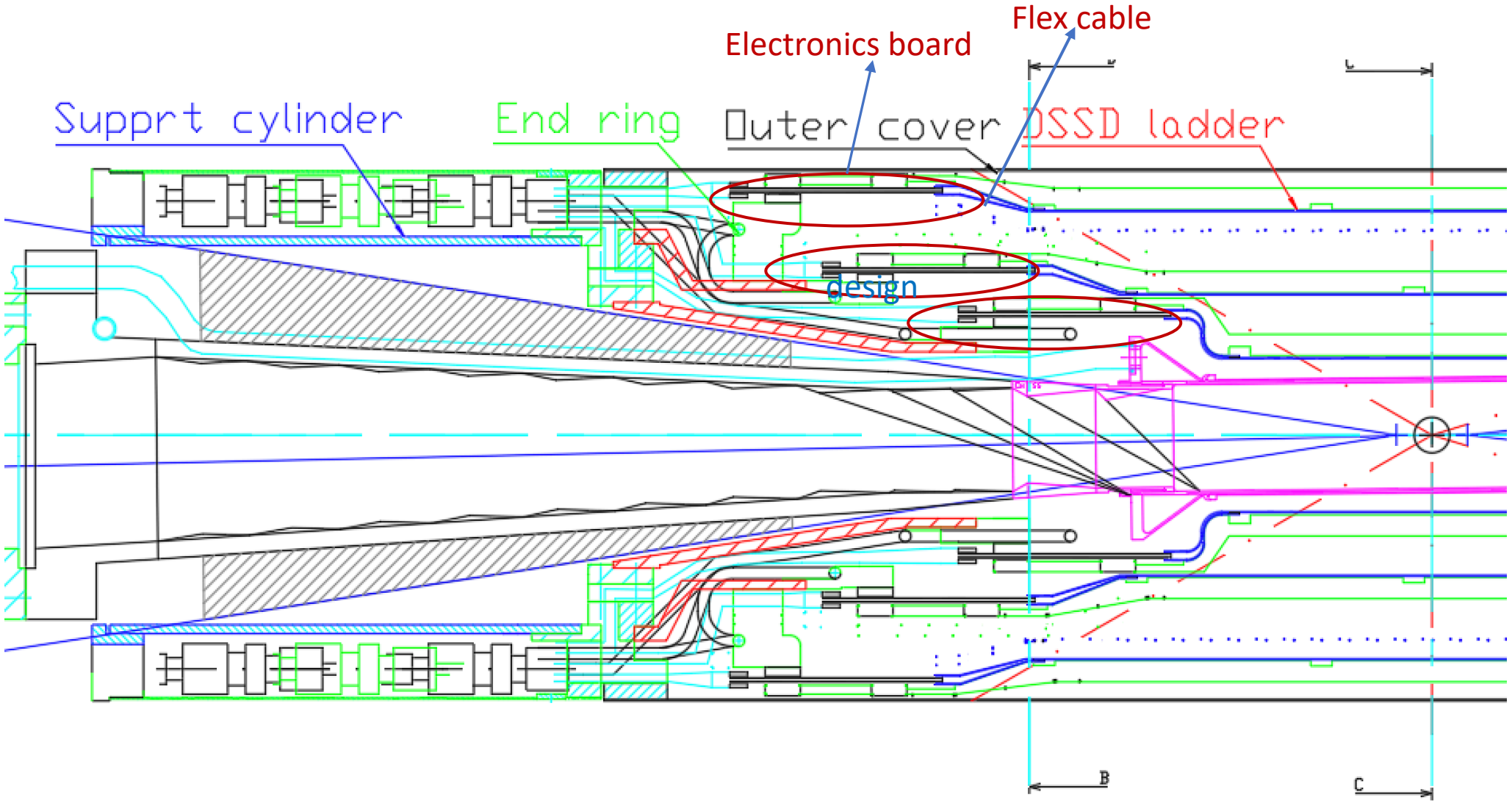
Summary

- Engineering design for the vertex detector module and vertex-beam pipe interface

Parameters	Requirement	Status
Cooling	Silicon temperature <30 ℃	2nd and 3rd layer can be handled. Air Cooling of B layer still an issue
Material budget	<0.15%X_0 per layer	OK at barrel region 50% -100% higher at forward regions
Resolution	< 3 µm Vibration with µm levels	Statics finite element simulation Next step: Dynamic simulation with air cooling Vibration test using carbon fiber support

Cabling design in BELLE2

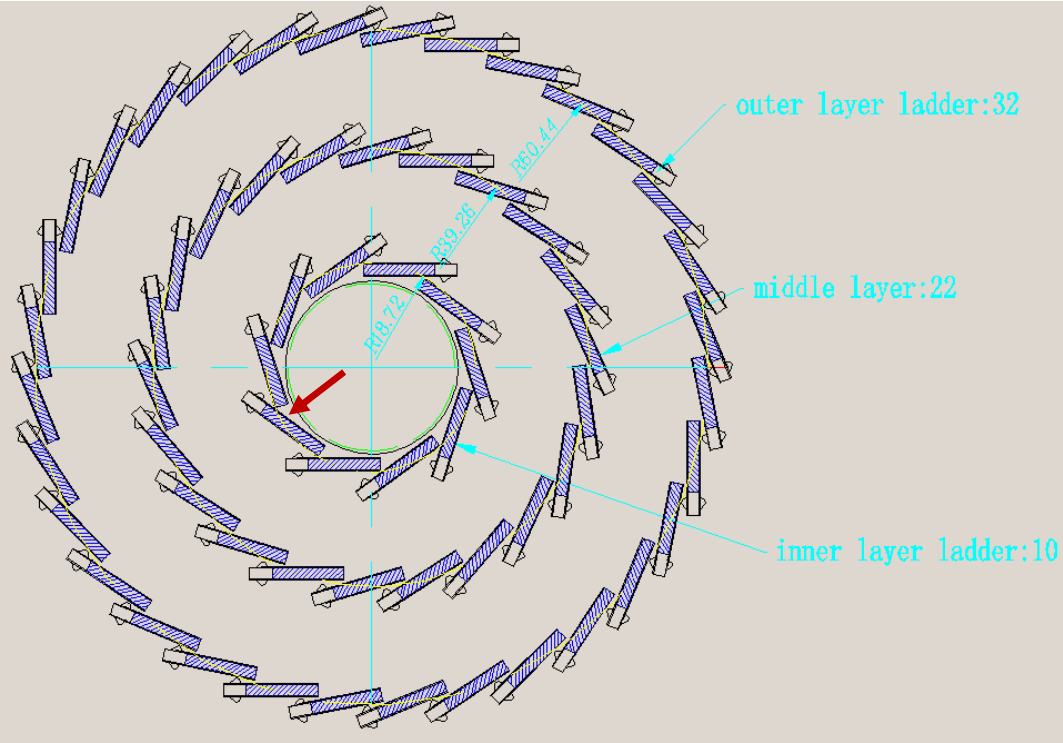
- Work on optimization of cabling in next step
  - With electronics colleague on electronics boards (radiation hardness)
  - Space optimization in Beampipe area (with Quan)

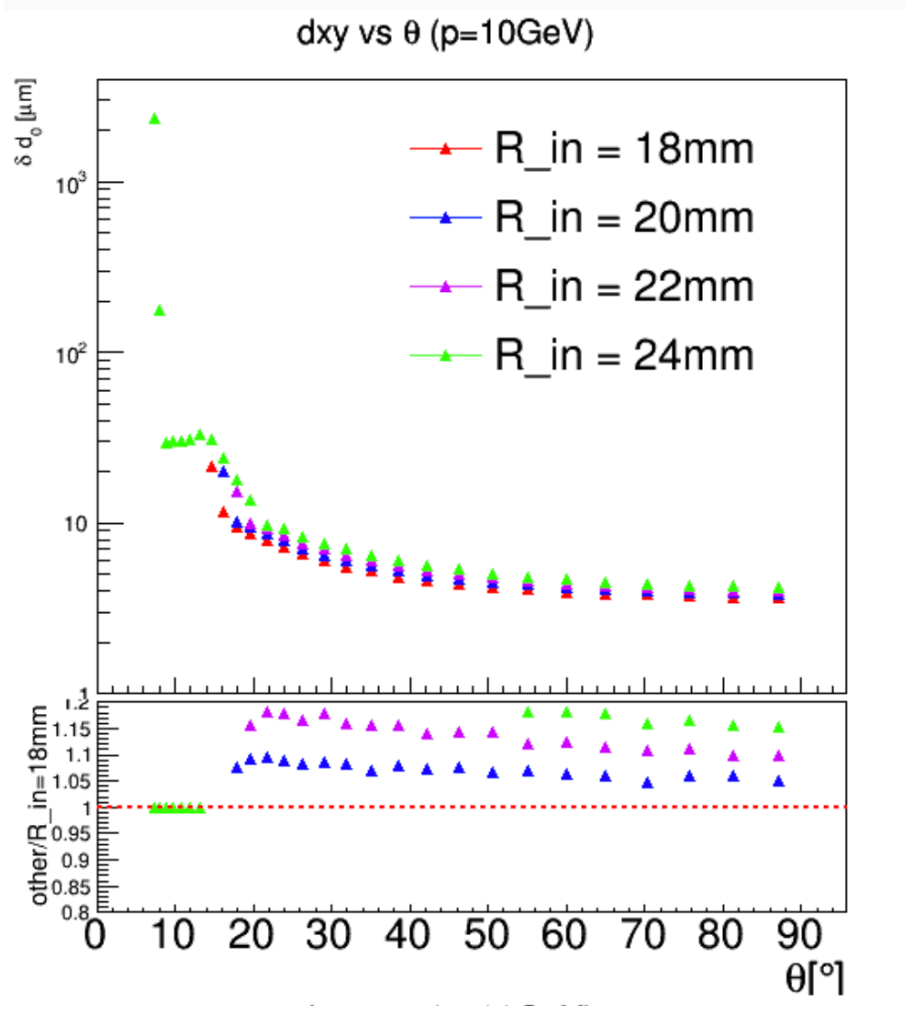


Backup: The radius of B layer of pixel detector

- the temperature b layer of vertex detector is still high
  - B layer is too close to beampipe (limited air flow)
  - Move the B layer a bit away ?
  - Impact parameter decreased 5-10% by moving 2mm

By Hao Zeng





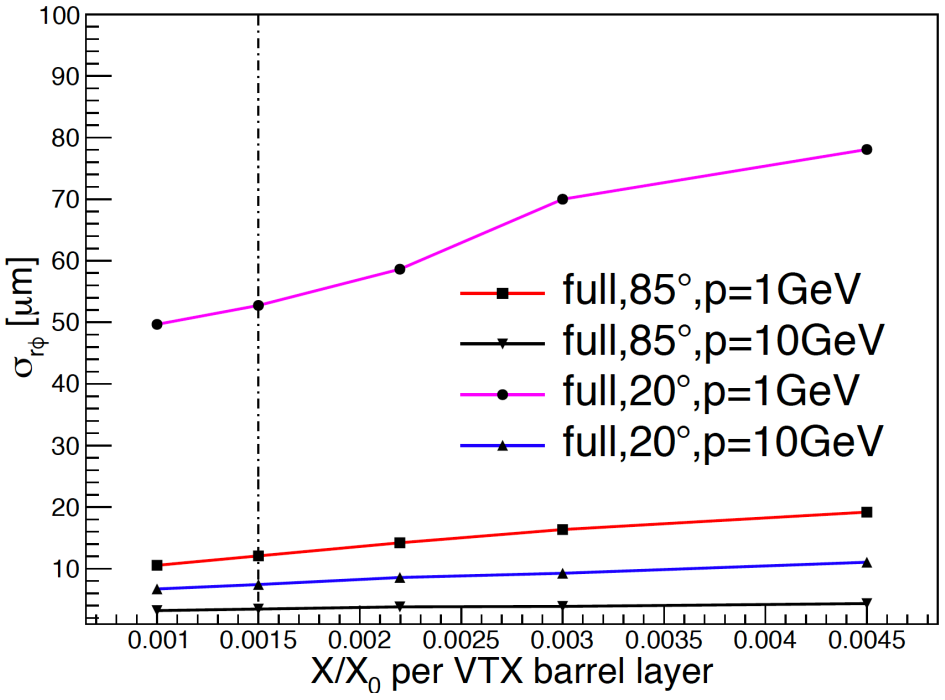
REQUIREMENT ON MATERIAL (2)

- CEPC study on material of vertex detector ：

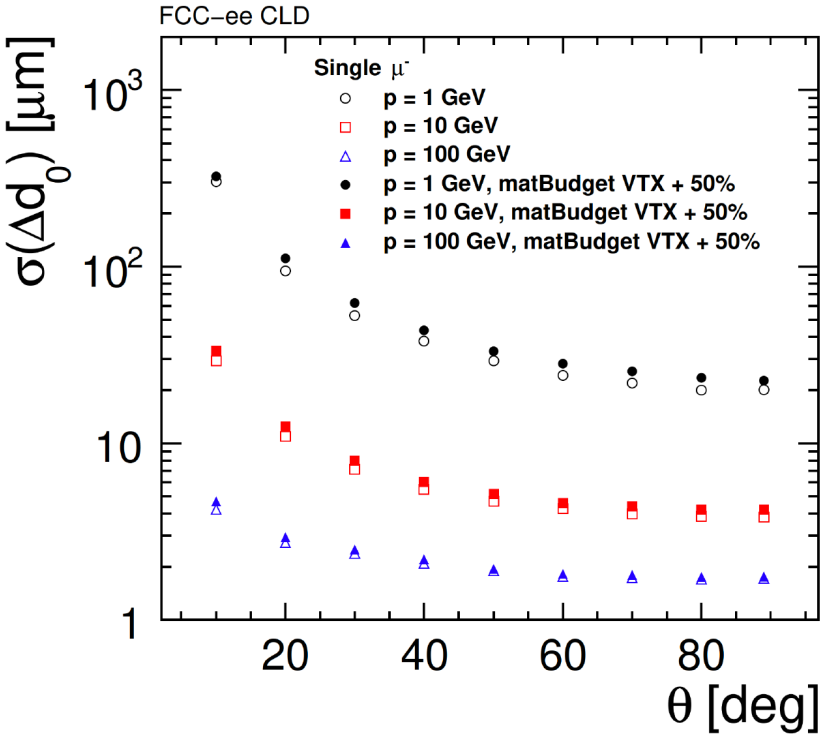
  Material requirement can be relaxed!

  - Increase material budget by 300%
  - 20~30% impact worse on 1GeV track very small impact on 10GeV track (<10%)
- Fcc-ee study on material of vertex detector ：
  - Increase material budget by 50% , small impact on impact parameter resolution

CEPC baseline detector



Fcc-ee CLD detector



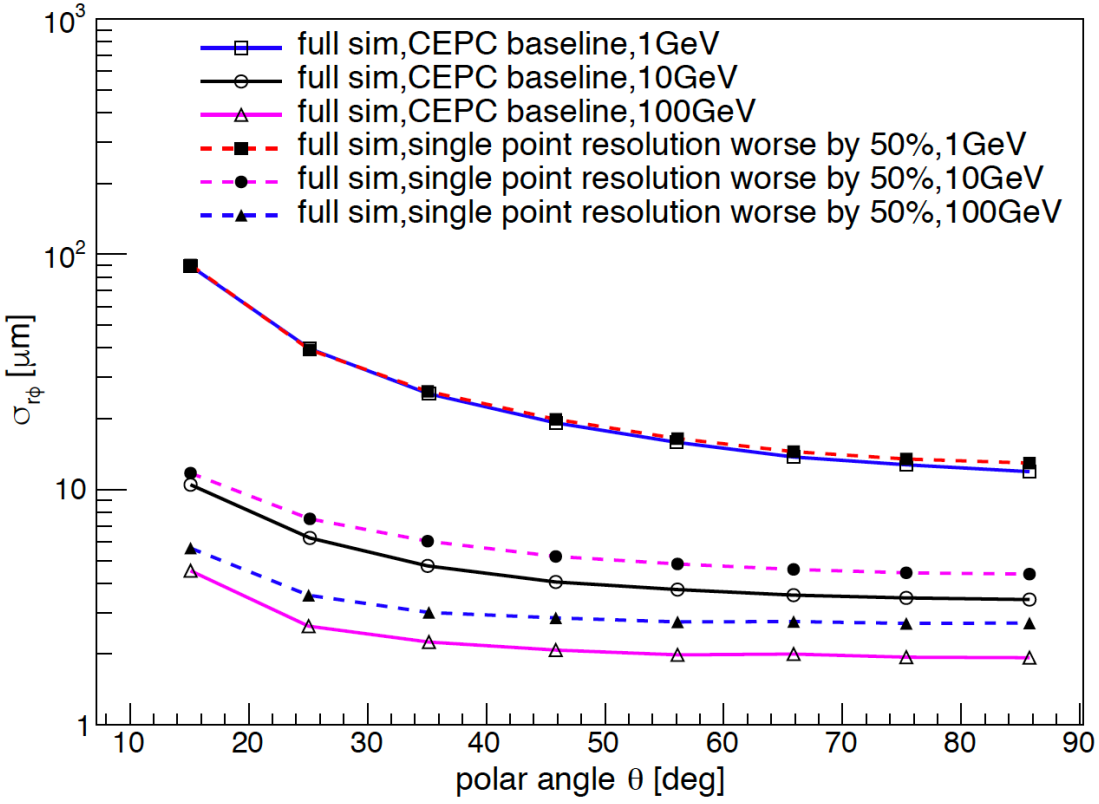
LIST OF REQUIREMENT

- Requirement on material
- Requirement on detector single point resolution
- Requirement on Power consumption and cooling
- Requirement on Timing

REQUIREMENT ON DETECTOR SINGLE POINT RESOLUTION

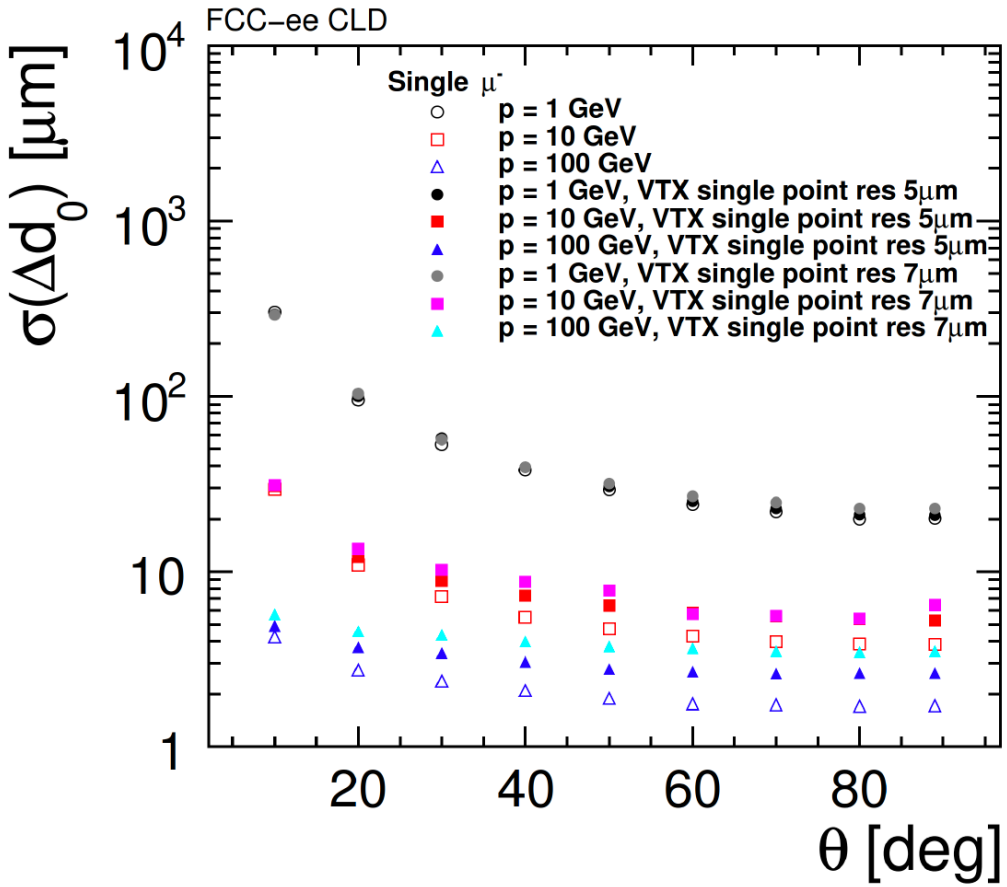
- CEPC/Fcc-ee requirement: 3μm single point resolution
- Vertex detector single point resolution gave large impact of d0 resolution
- Should try hard to improve single point resolution !

CEPC baseline detector



Fcc-ee CLD detector

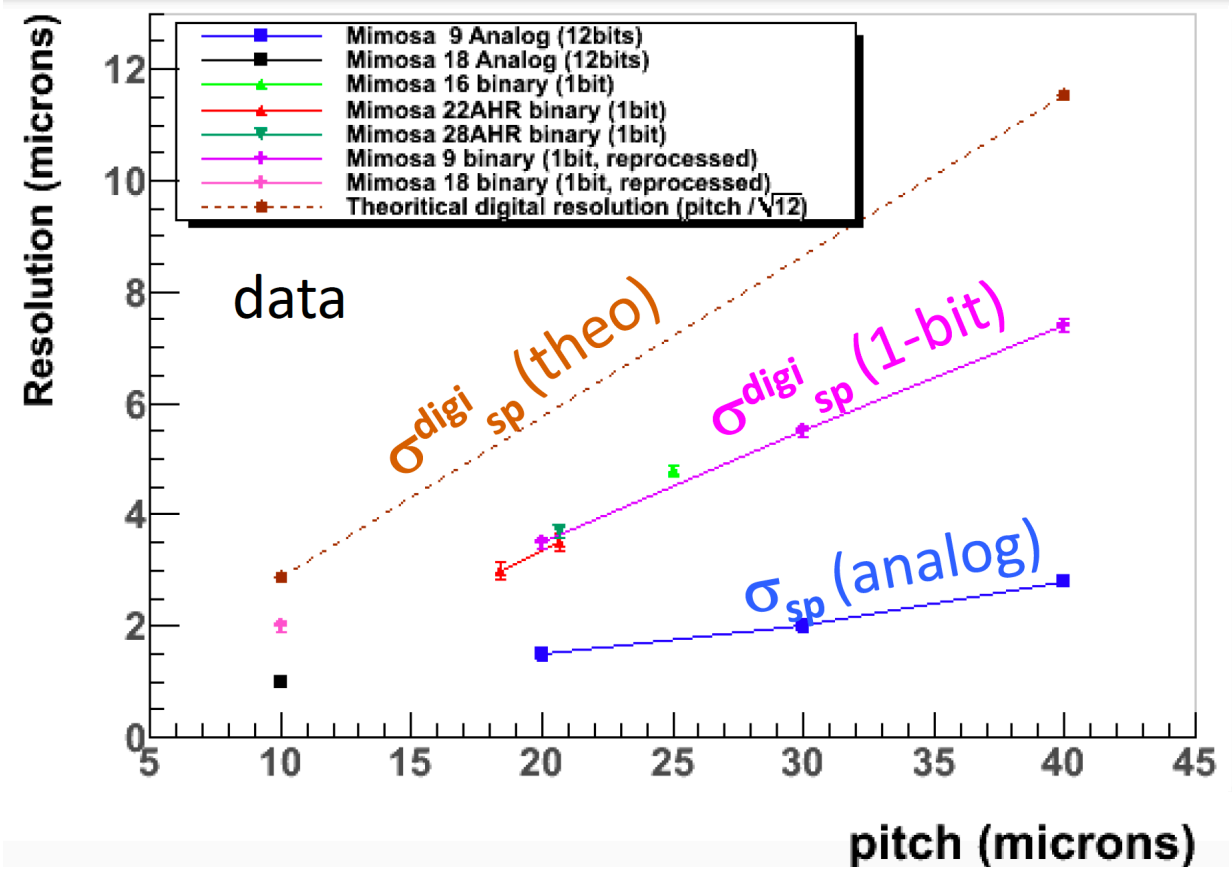
(from Philipp Roloff's talk in Fcc workshop)

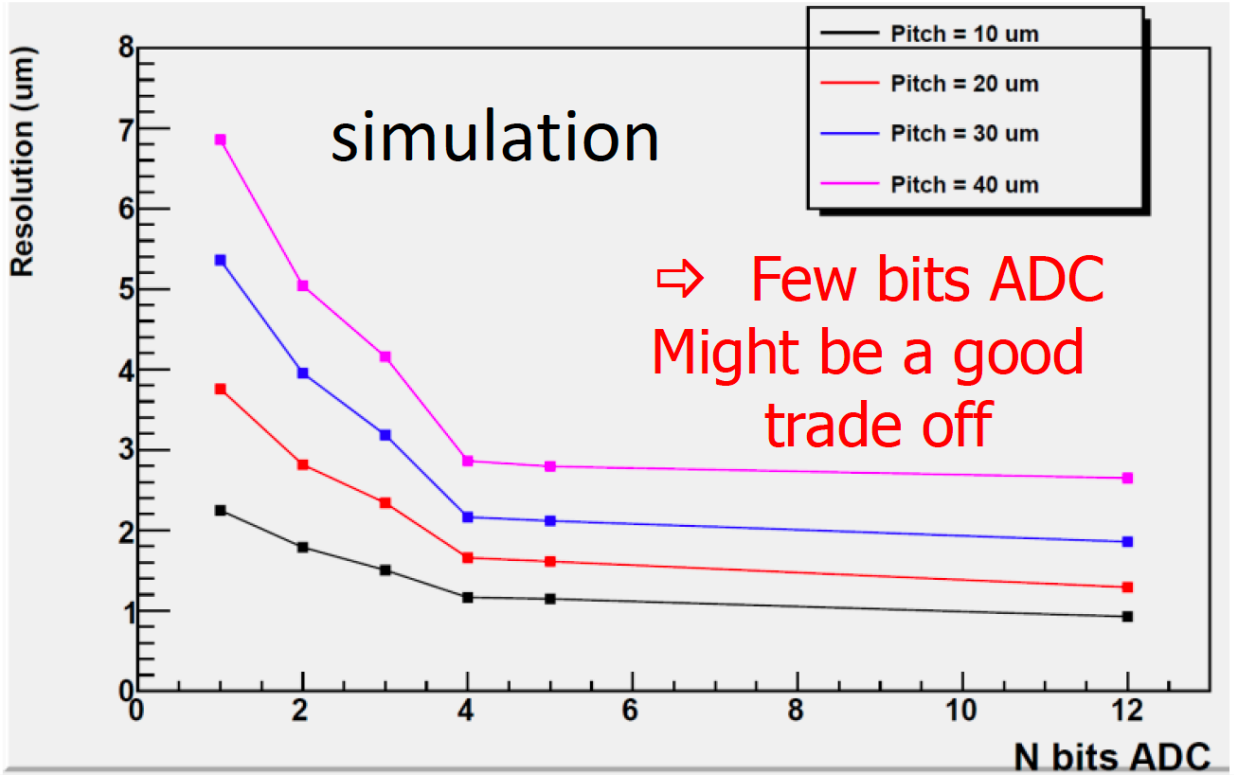


REQUIREMENT ON DETECTOR SINGLE POINT RESOLUTION

- Keeping σ_{sp}=3µm,
- Need to design a very small pixel (~17µm) with Digital readout
- Or One can design large pixel (~40µm) , with analog readout (with a few ADC)

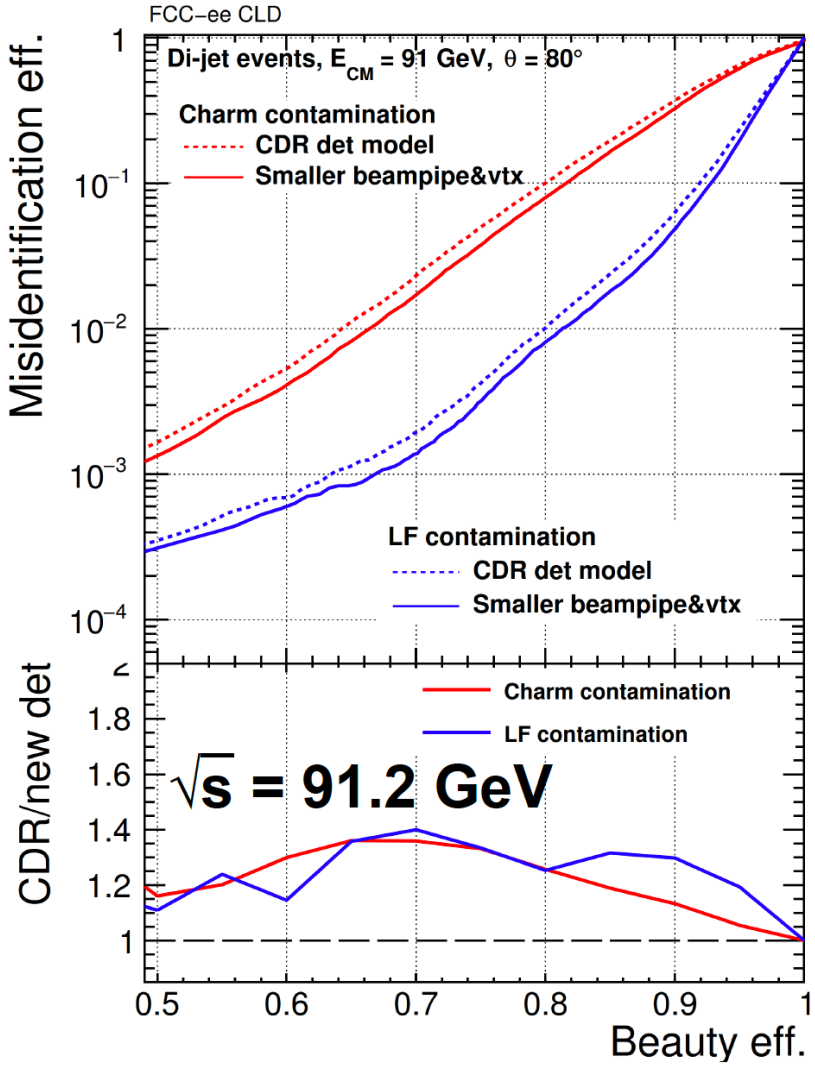
From Auguste Besson's talk in Fcc workshop





⇨ σ_{sp} ~ 3 µm ⇦⇨ pitch ~ 17 µm (not 25 µm !)

Requirement on Beampipe radius



- Keeping σ_{sp}
- The smaller beampipe, closer of first pixel layer to beam spot
- Fcc-ee Reduced the beampipe radius from 17mm to 12mm
- Improve d0 resolution by 30~40%

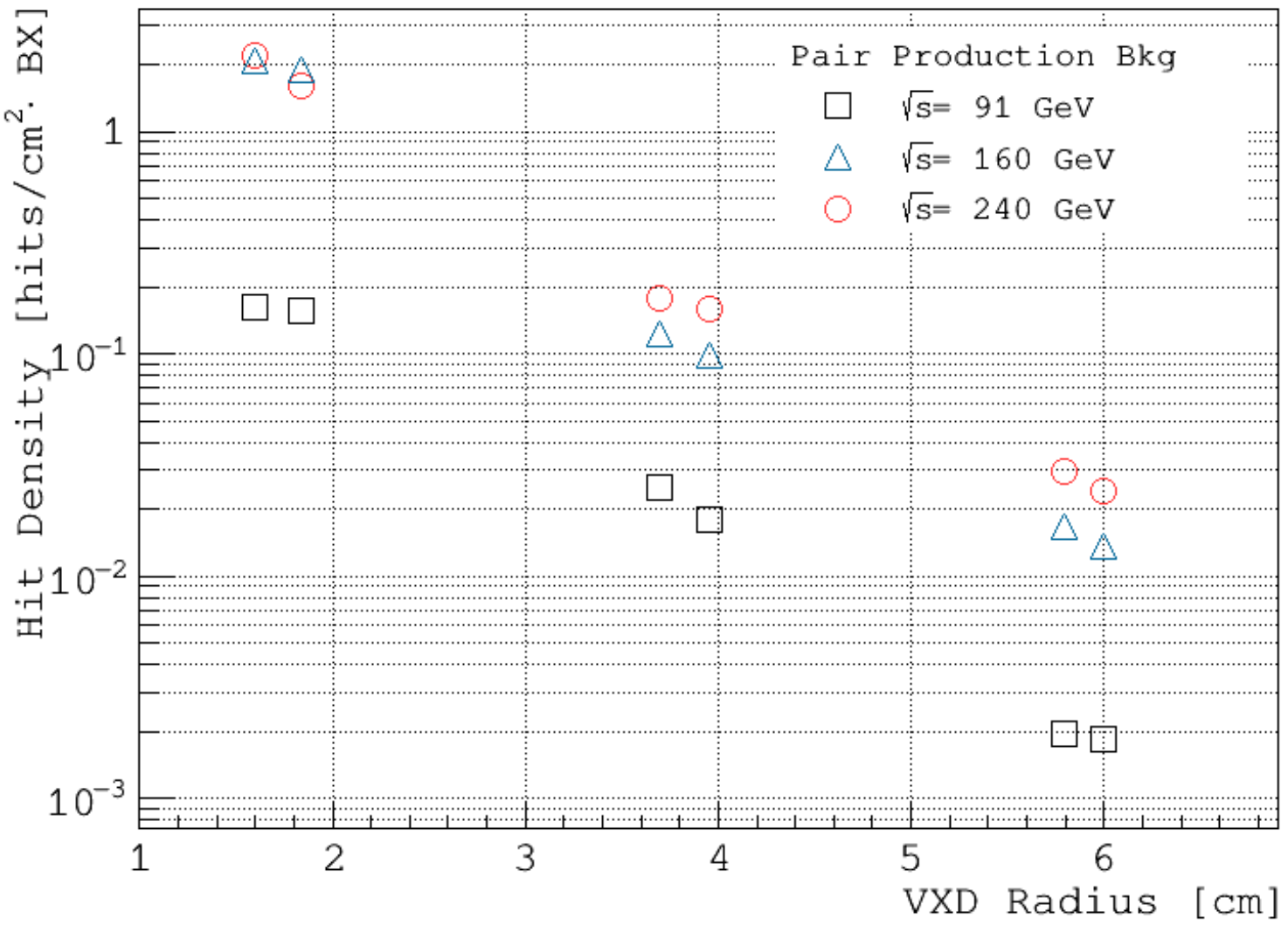
LIST OF REQUIREMENT

- Requirement on Material
- Requirement on detector single point resolution
- Requirement on Power consumption and cooling
- Requirement on radiation hardness

REQUIREMENT ON RADIATION HARDNESS

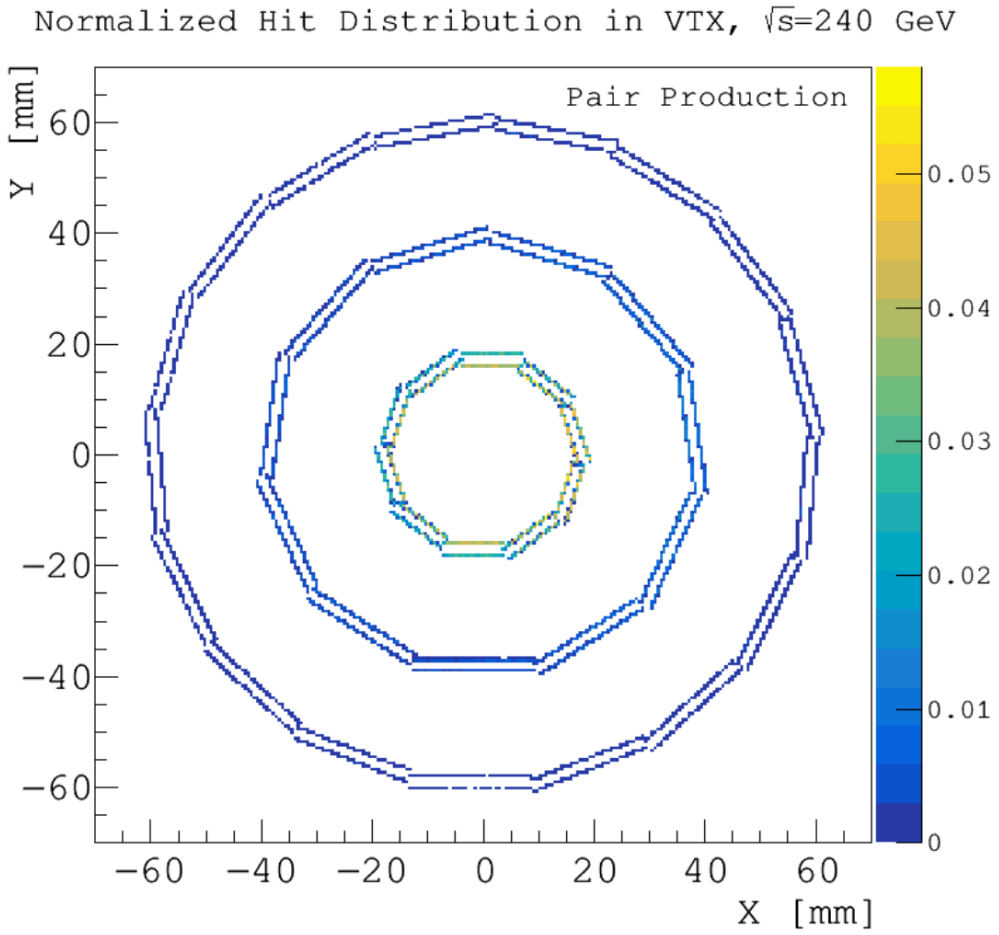
- Bunch spacing
  - Higgs: 680ns; W: 210ns; Z: 25ns
  - Meaning 40M/s bunches (same as the ATLAS Vertex)
- Hit density
  - 2.5hits/bunch/cm^2 for Higgs/W; 0.2hits/bunch/cm^2 for Z
- Cluster size: 3pixels/hit
  - Epi- layer thickness：~18μm
  - Pixel size：25μm×25μm

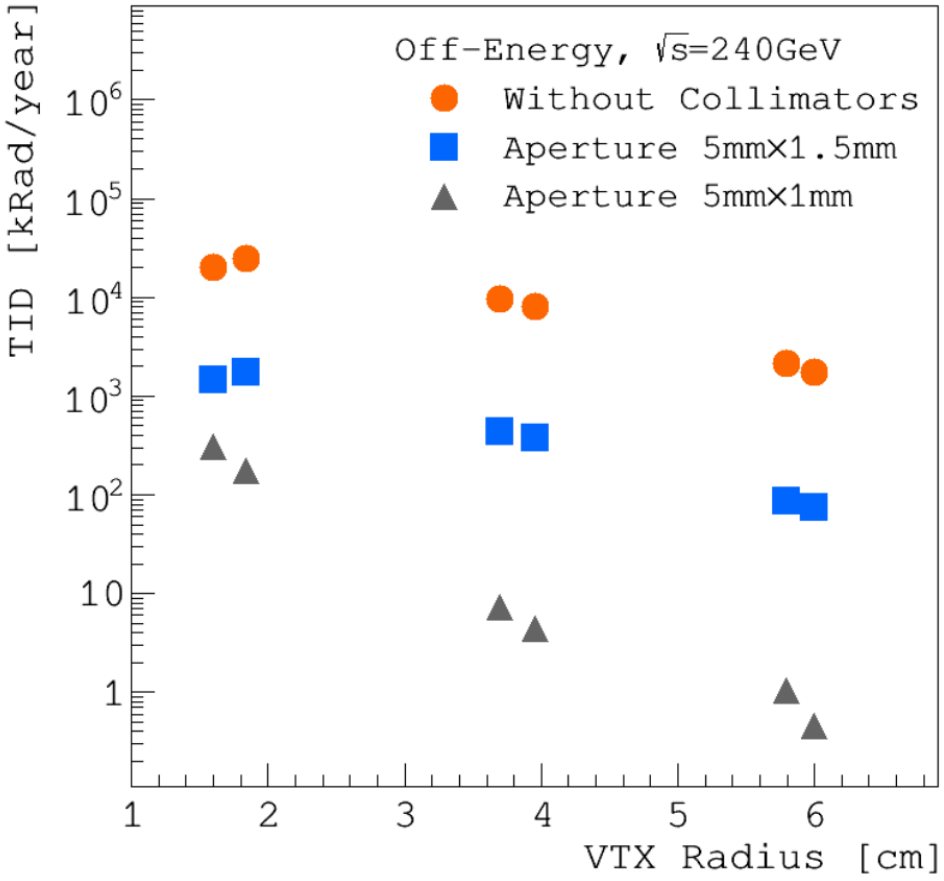
From the CDR of CEPC



REQUIREMENT ON RADIATION HARDNESS

- Radiation tolerance **(per year):** 1 MRad &2×10^{12} 1 MeV n_{eq}/cm^2

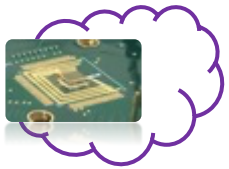




PIXEL SENSOR R&D

CEPC Pixel Sensor R&D

- **JadePix-1**：Diode optimization; design & characterization
- **JadePix-2**：Compact pixel design, in-pixel amplification, digital readout
- **JadePix-3**：bug-fix and improved design (submitted)
- **Taichu-1**： Column Drained readout (FE-I3), two-stage FIFO (submitted)



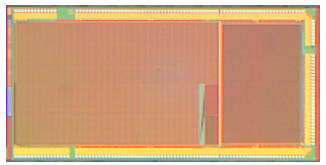
Ultimate Pixel Sensor

- **Specifications:** spatial resolution~3 μm, power consumption<50 mW/cm^2, radiation tolerance 10 MRad (TID)；

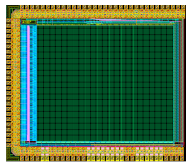
2015 2016 2017 2018 2019 2020 2021 2022 2023 2024

DEVELOPED CMOS PIXEL SENSOR PROTOTYPES FOR CEPC

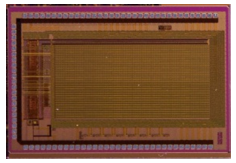
Prototype	Pixel size (μm^2)	Readout time	Power Consumption	In-pixel circuit	R/O architecture	Main goals	Status
JadePix1	33 × 33 16 × 16	~100 μs	~ 100 mW/cm^2	SF/amplifer, analog output	Rolling shutter	Sensor optimization	Lab. and beam test finished
JadePix2	22 × 22	~100 μs	< 100 mW/cm^2	amp., discriminator, binary output	Rolling shutter	Small pixel, Power < 100 mW/cm^2	Electrical functionality verified
MIC4	25 × 25	~10 μs	<26mW/cm^2	Low power front-end, address encoder	Data-driven, Asynchronous	Small pixel, fast readout for ZH run	Electrical functionality verified
JadePix3	16 × 26 16 × 23.11	~10 μs	<26mW/cm^2	Low power front-end, binary output	Rolling shutter with end of col. priority encoder	Small pixel, low power	In fabrication
Taichu-1	25×25	~50ns	100~200 mW/cm^2	binary output	Data-driven, Priority encoder	Full Functionalities Fast readout for Z pole	Fabricated, To be tested



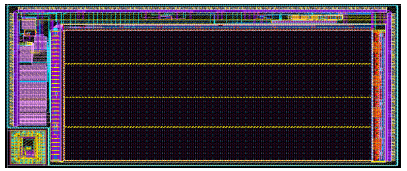
JadePix1 (IHEP)
3.9 × 7.9 mm^2



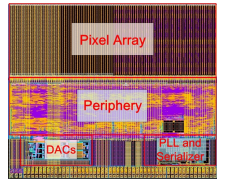
JadePix2 (IHEP)
3 × 3.3 mm^2



MIC4 (CCNU & IHEP)
3.2 × 3.7 mm^2



JadePix3
IHEP, CCNU, Dalian Minzu Unv., SDU
6.1 × 10.4 mm^2



Taichu-1
IHEP, SDU, NWPU, IFAE & CCNU
5 × 5 mm^2

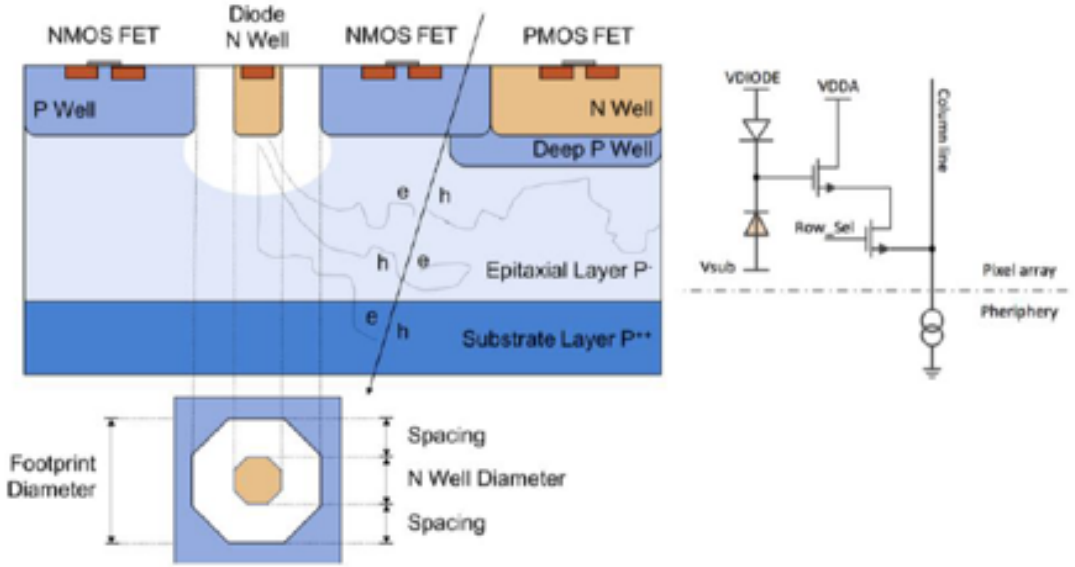
All prototypes in TowerJazz 180 nm CIS process

FUNDED BY MOST AND IHEP

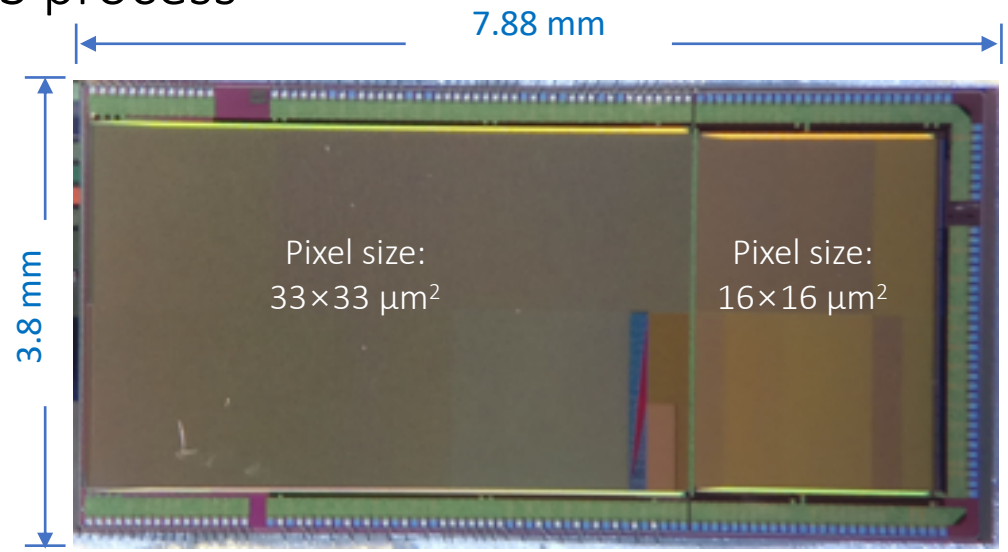
JadePix-1 Pixel

Y.Zhang, et al, NIMA 831(2016)99-104

- 1st prototype sensor developed with TJ 0.18 µm CIS process
- Primary goal: diode geometry optimization



Impacts of electrode size and footprint on charge collection performance



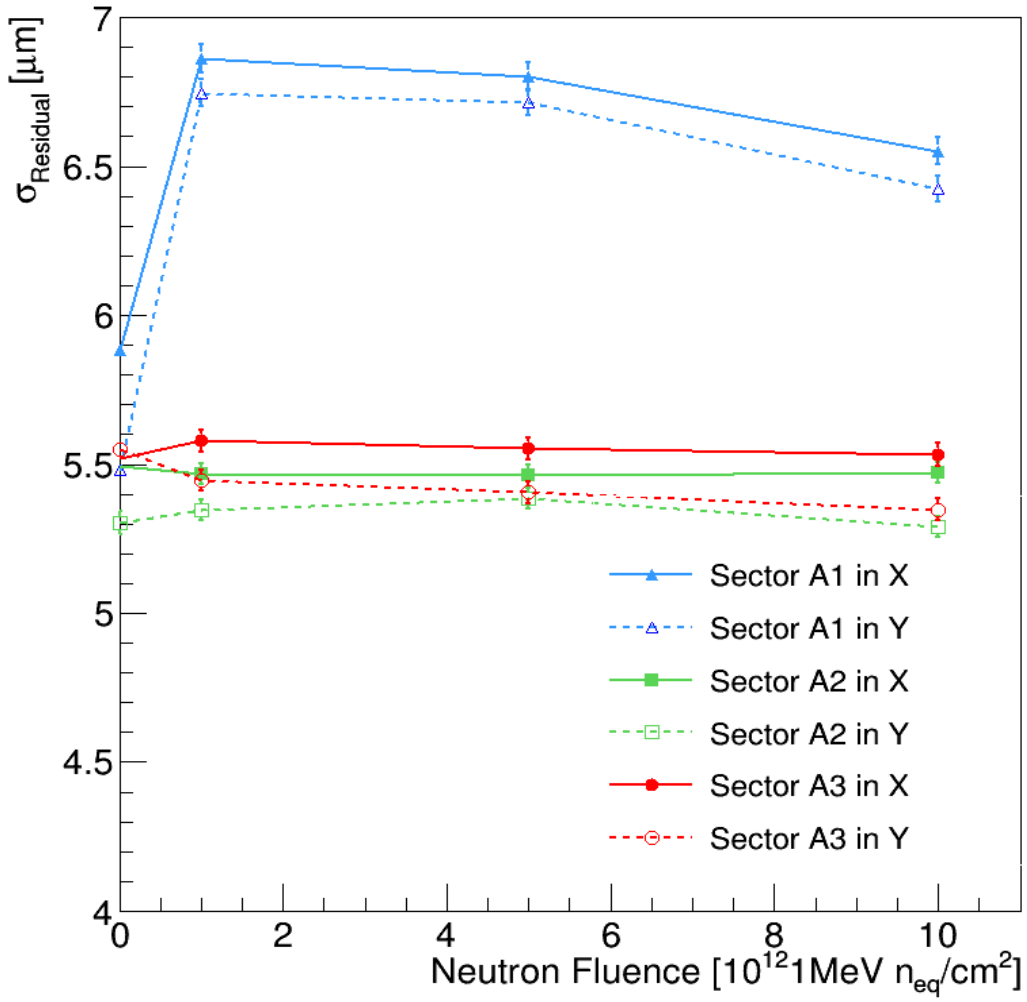
Supported by the State Key Lab of Particle Detection and Electronics & IHEP Innovation fund, **with lots of helps from IPHC**

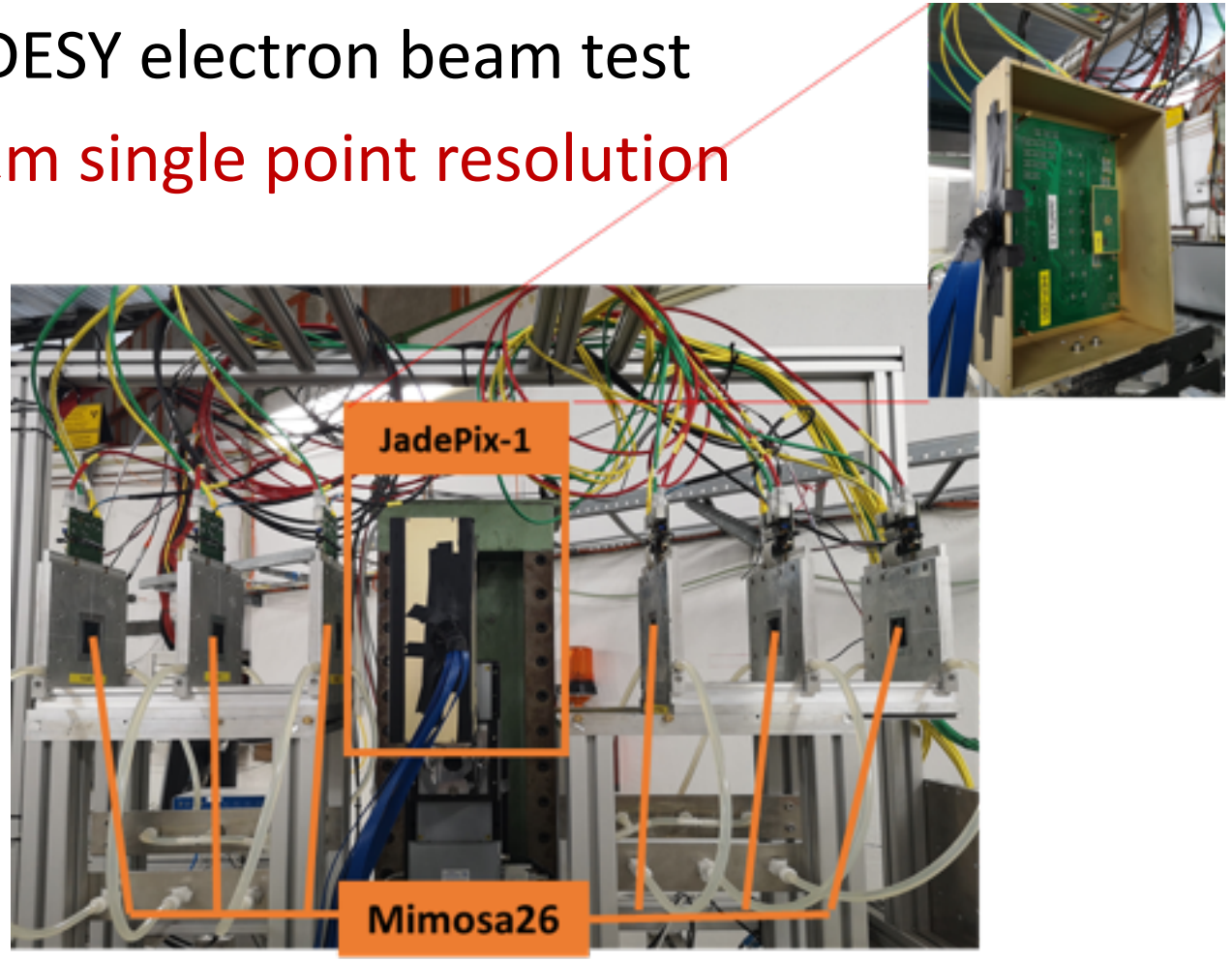
- Submission in November 2015, test system developed and verified in 2016; detailed performance characterization in 2017& 2018

	Resolution	Readout Speed	TID	Power Consumption
Jadepix-1 (TJ180nm)	3~7μm (Beam test)	~100μs integration time Analog readout test chip		~100mW/cm2

JadePix-1 Resolutions

- 5~7 μm spatial resolution achieved in DESY electron beam test
- Getting close to CEPC requirement: 3 μm single point resolution

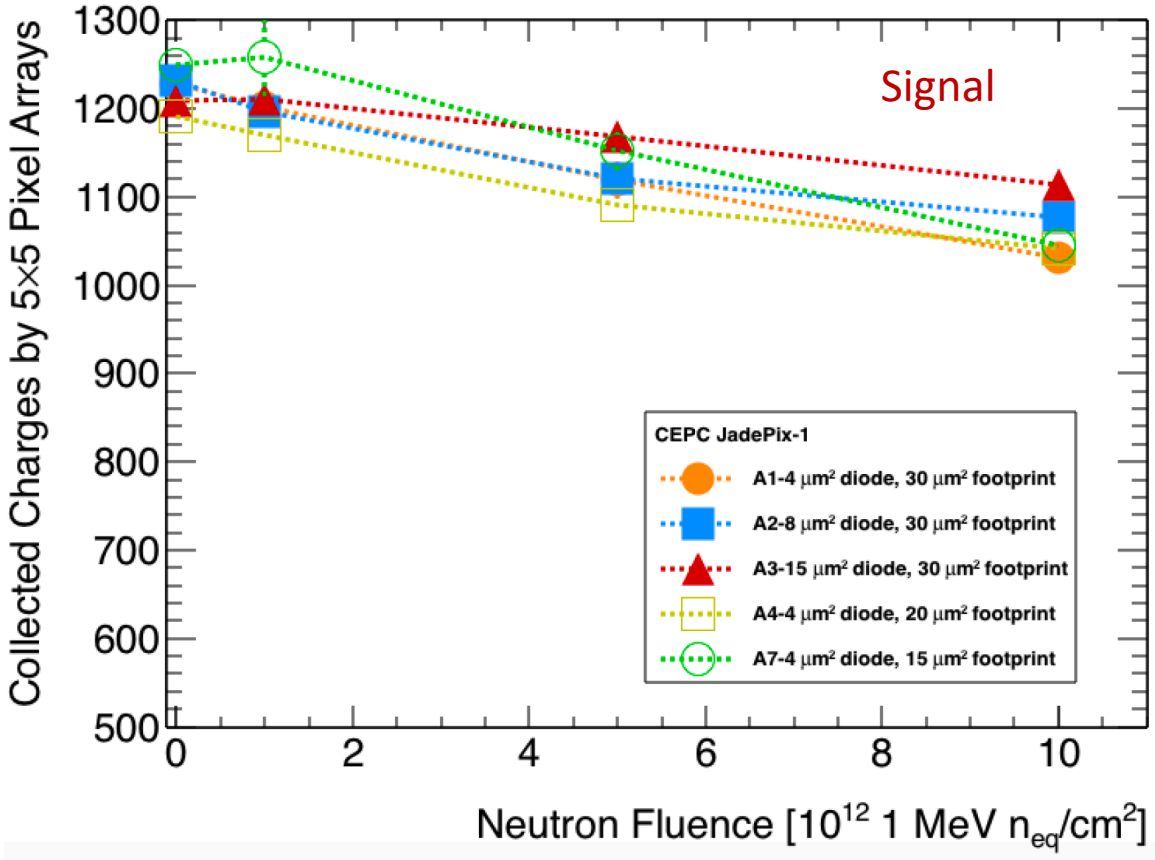


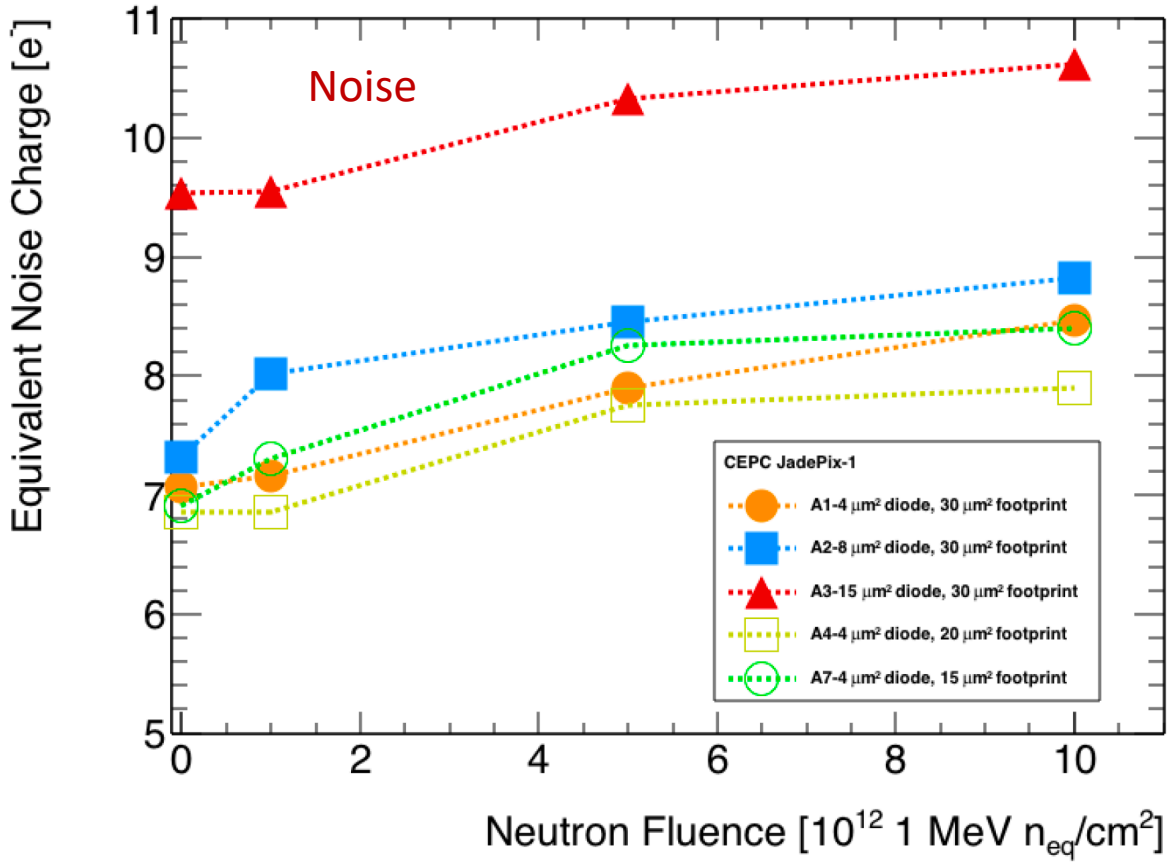


Beam telescope resolution to extracted to derive pixel resolutions

JadePix-1 radiation hardness

- CEPC requirement: have 2×10^{12} 1 MeV n_{eq}/cm^2 per year
- Neutron Irradiation up to 10^{13} Neq/cm^2
  - Signal to Noise ratio above 50 after irradiation
  - Jadepix-1 met CEPC requirement

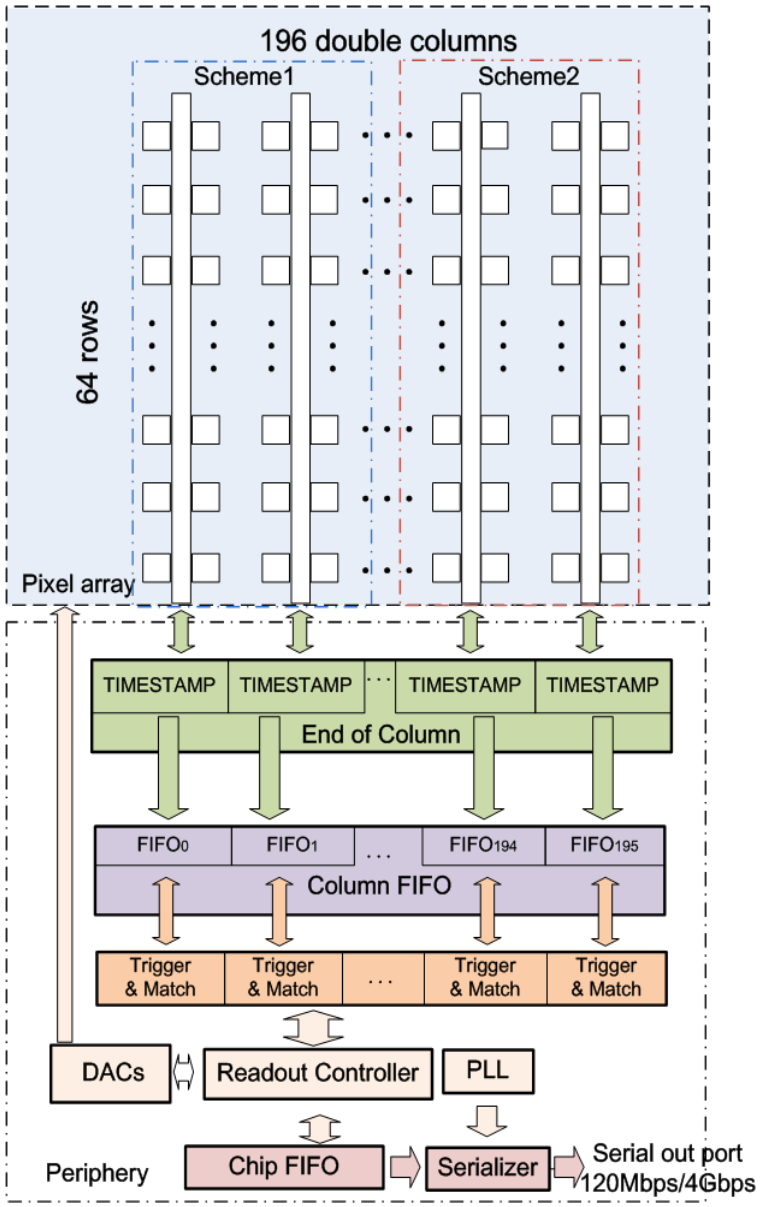




TAICHU-1: FAST READOUT + FULL FUNCTIONALITIES

By IHEP, SDU, NWPU, IFAE & CCNU team

Funded by MOST 2

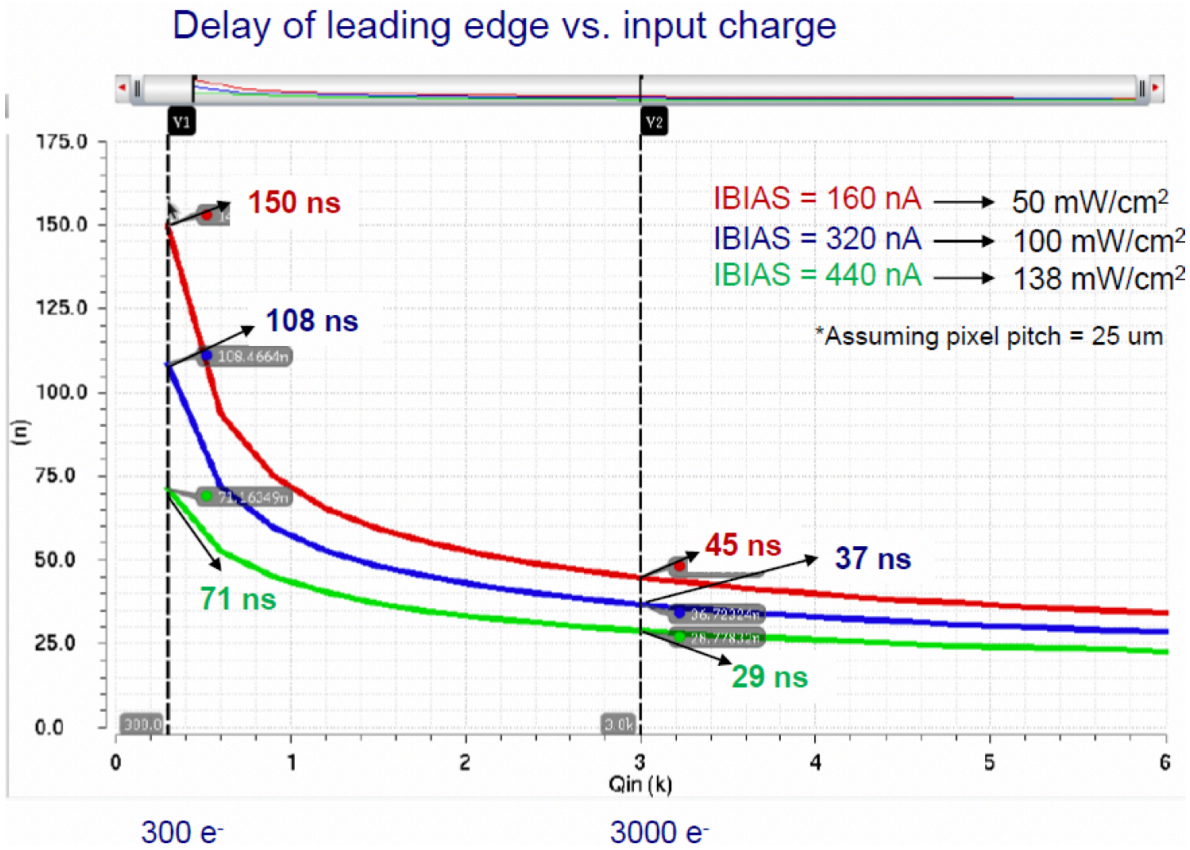


- CEPC readout time requirement:
  - 500ns deadtime @40MHZ(Z pole)
- **TAICHU-1** Column-drain readout
  - Priority based data driven readout; time stamp at EOC
  - Dead time: 2 CLK for each pixel (50ns @40MHz CLK)
  - Two digital pixel designs: FEI3-like and ALPIDE-like design
- 2-level FIFO architecture
  - L1: column level, to de-randomize injecting charge
  - L2: chip level, to match in/out data rate between core and interface
- Trigger readout:
  - Coincidence by time stamp, matched event read out

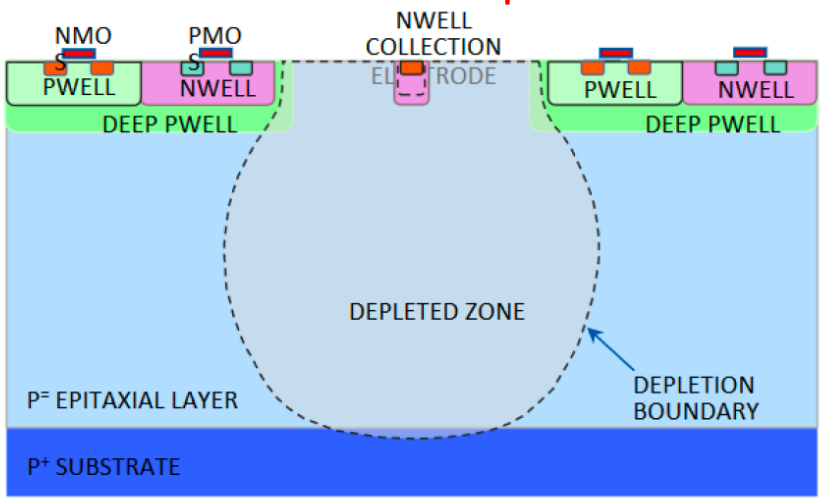
TAICHU-1: FAST READOUT + FULL FUNCTIONALITIES

By IHEP, SDU, NWPU, IFAE & CCNU team

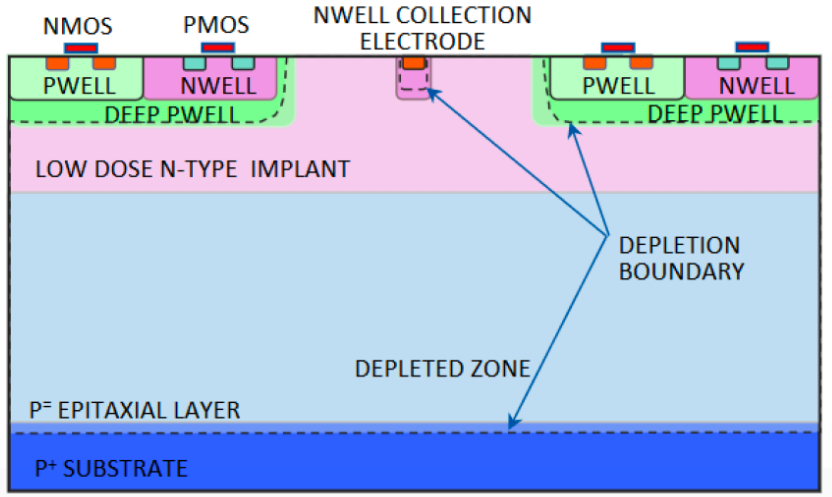
- CEPC time stamping precision requirement:
  - 25-50ns, can time stamping each collision at Z pole
- **Taichu-1 pixel analog design:**
  - 75ns~150ns (based one standard CMOS MAPS tech.)
  - Consider to use depleted CMOS MAPS



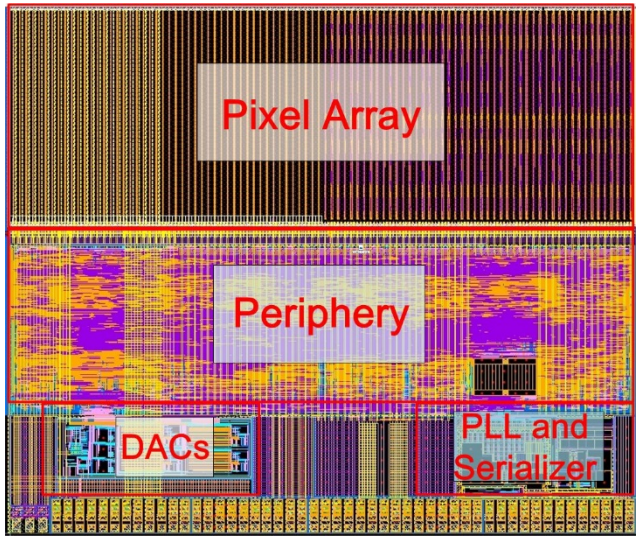
Standard : no full depletion

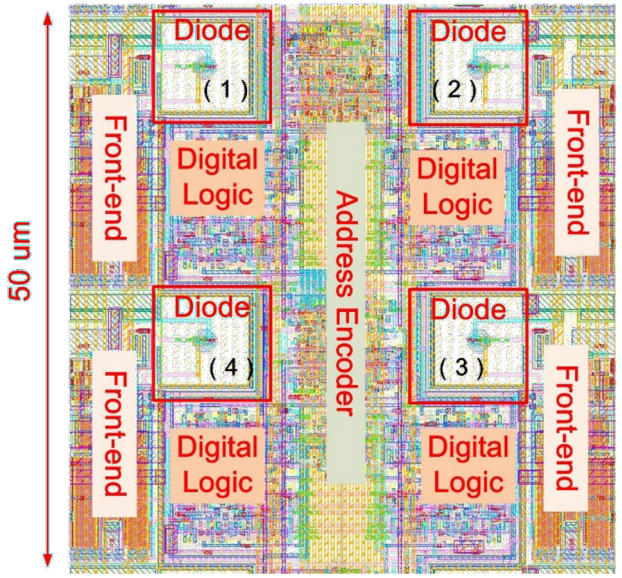


Modified : full depletion, faster charge collection

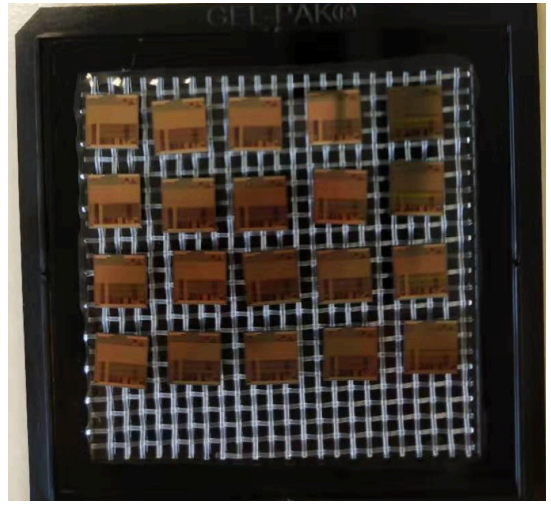


TAICHU-1: (FULL FUNCTIONALITIES + FAST READOUT)





- First MPW tapeout was submitted in June
- Chip received on Nov. 15, 2019
  - With 60 chips, now wire bonding with test PCBs
- One block area of 5mm×5mm was fully occupied
  - A full functional pixel array (small scale)
    - 85% of the block area
    - A 64×192 Pixel array + Periphery + PLL + Serializer
    - Bias generation included
    - I/O arranged in one edge, as the final chip
  - other independent test blocks (less critical)
    - LDO + PLL



Chip size: 5mm×5mm
Pixel size: 25μm×25μm

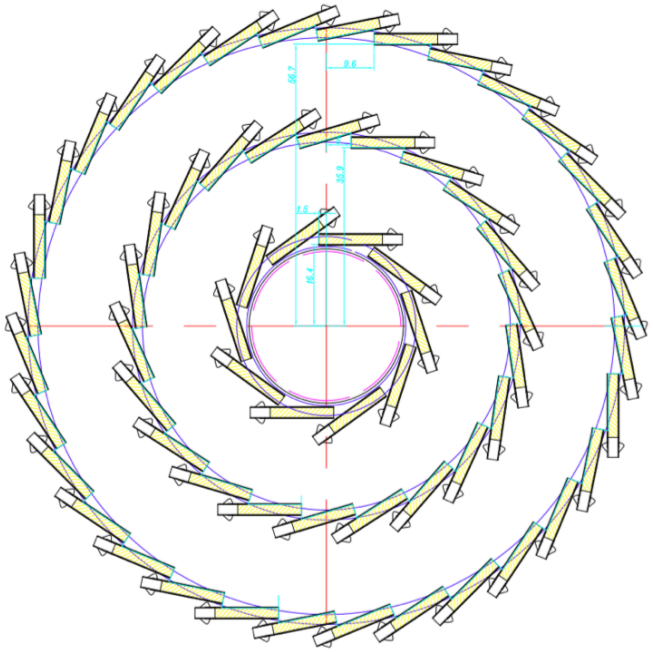
	Resolution	Readout Speed	TID	Power Consumption
Taichu-1 (TJ 180nm)	3~5μm	~50ns@40MHz Digital readout	Te be tested	100~200mW/cm2

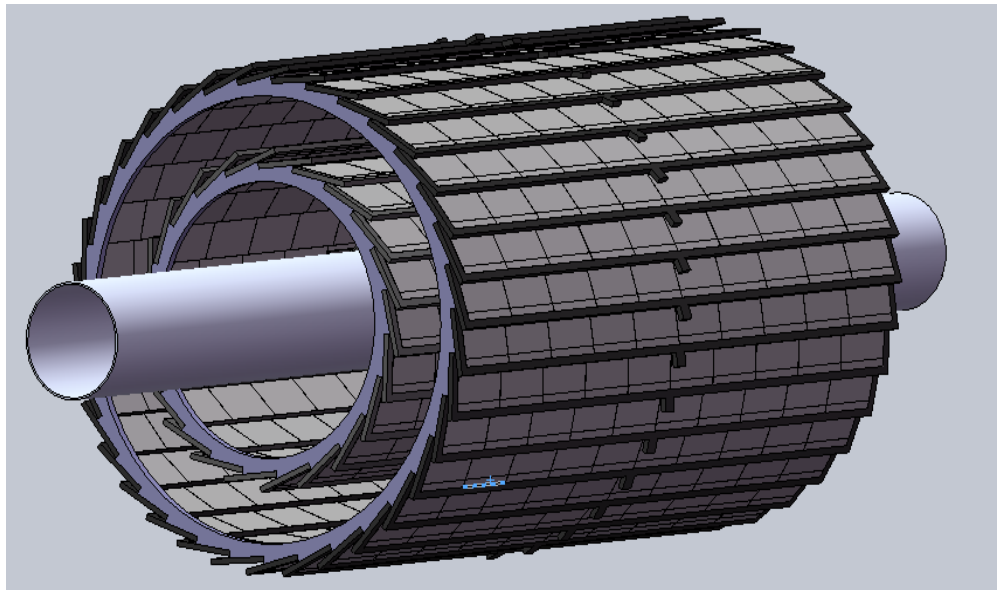
VERTEX DETECTOR PROTOTYPE

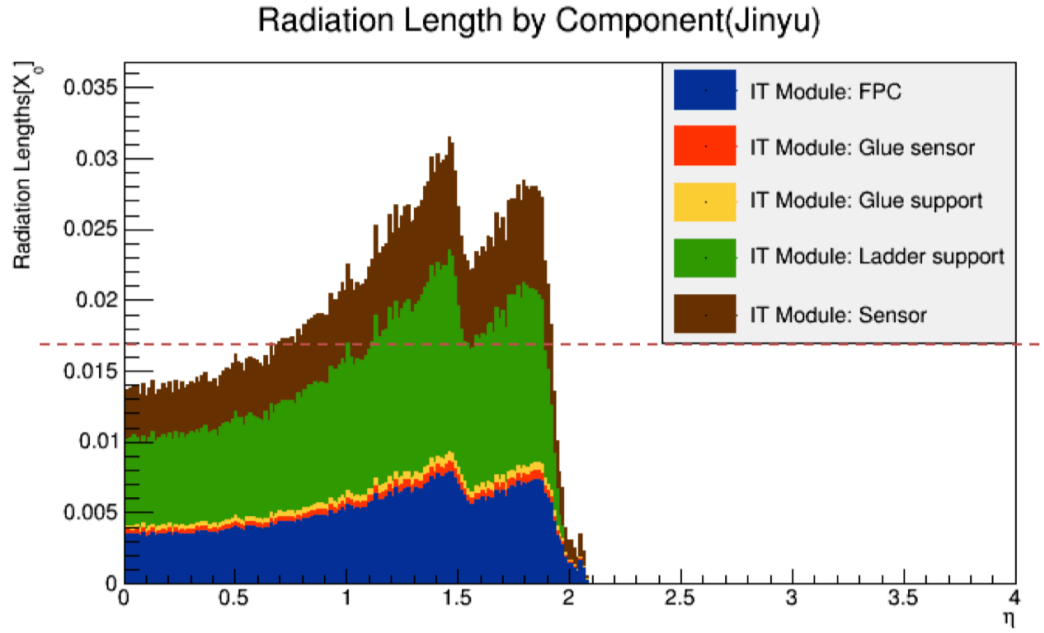
Funded by MOST 2

- Plan to build full size vertex detector prototype
  - Three double layer vertex detector
  - With Fractions of the modules will be installed
  - Supported by MOST , 12M RMB

	R (mm)	$\|z\|$ (mm)	$\|\cos\theta\|$
Layer 1	16	62.5	0.97
Layer 2	18	62.5	0.96
Layer 3	37	125.0	0.96
Layer 4	39	125.0	0.95
Layer 5	58	125.0	0.91
Layer 6	60	125.0	0.90

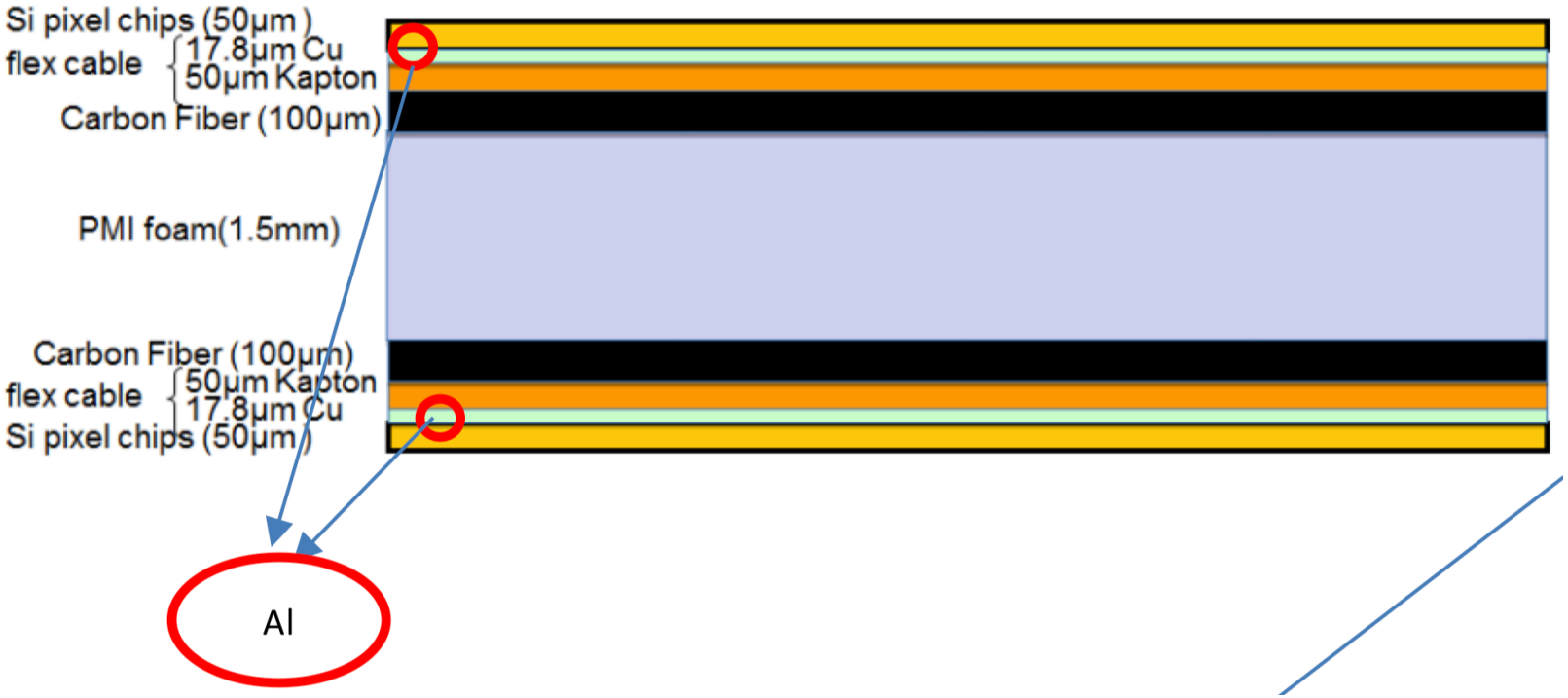


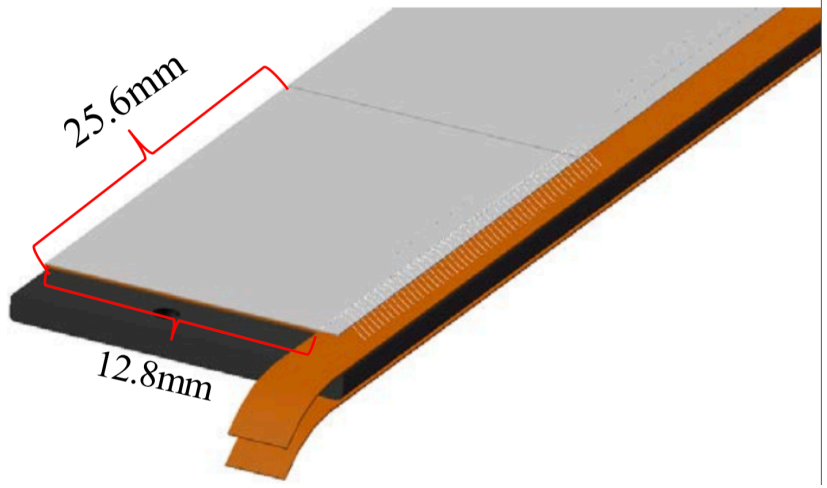




VERTEX DETECTOR PROTOTYPE: MODULE DESIGN

- Requirement : Material budget 0.15%X_0 per layer
- First draft of CEPC module design:
  - Material budget can barely 0.15 %X_0 per layer at 90 degree
  - Need to be rigid in air cooling, Difficult to reduce material budget

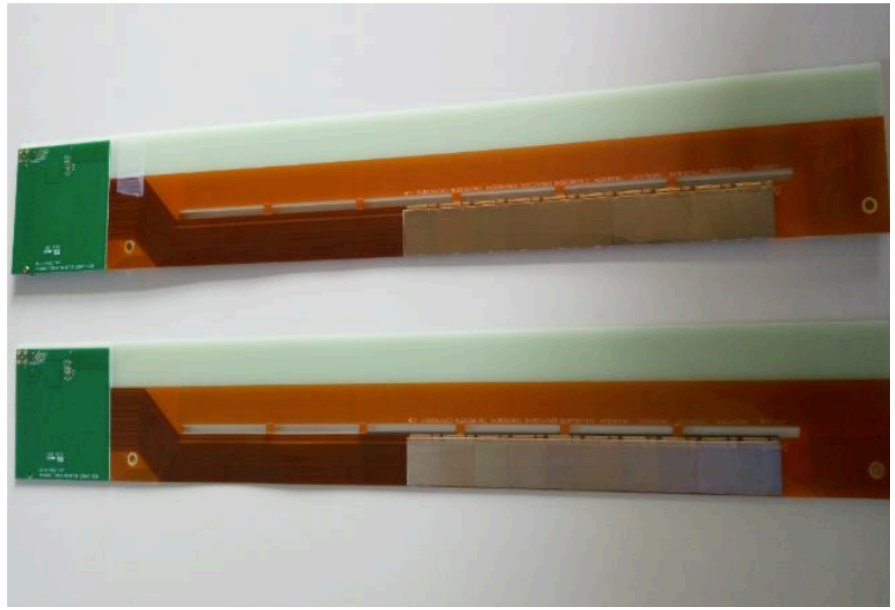




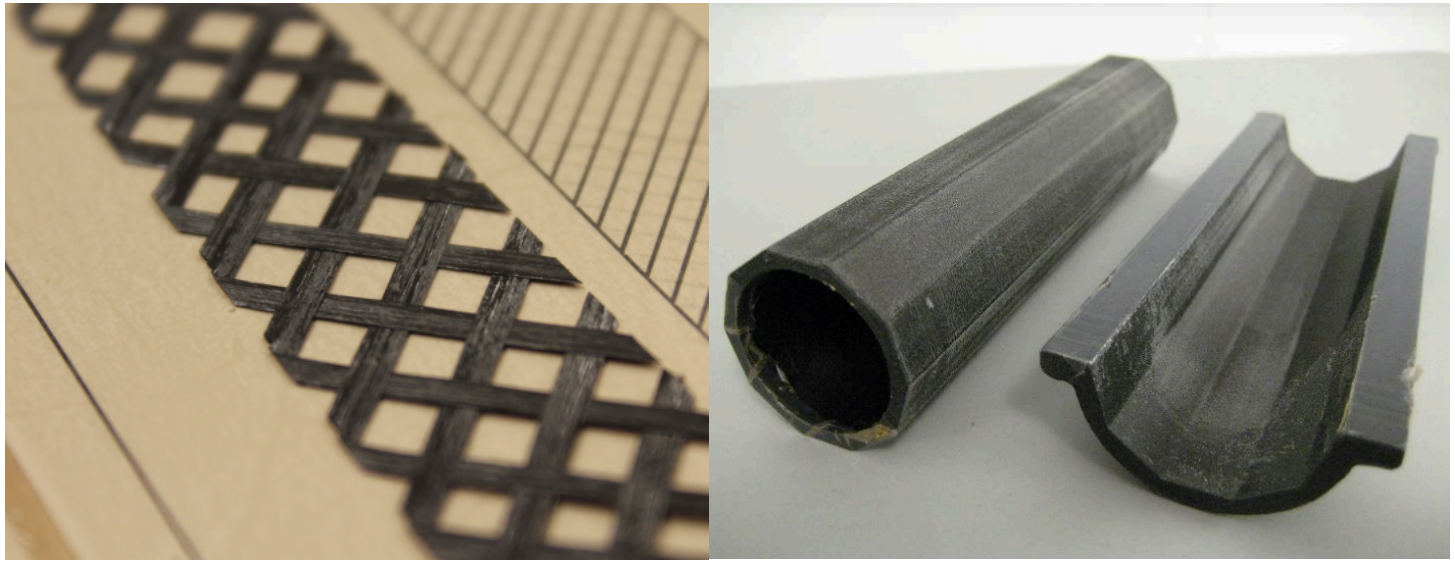
VERTEX DETECTOR PROTOTYPE

- IHEP has experience on building single-side modules
  - R & D module assembly scheme for double-side modules
- Collaboration with Livepool on detector support structure
  - New idea from Livepool of the ladder structure reinforcement.
  - Produce sample and test them in next step

Single-side HRCMOS pixel module for BESIII

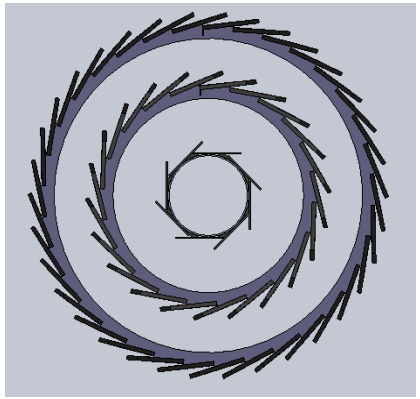


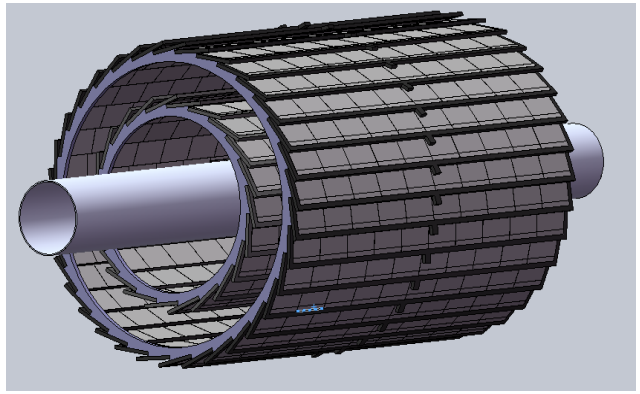
Idea about the detector support structure



Conceptual Design of VTX Support –V1

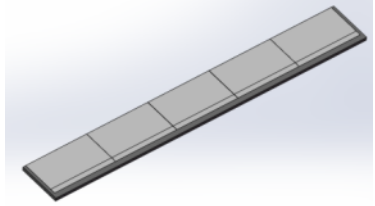
Sensor chip : 14.8 x 25.6 x 0.05 mm (2mm wide margin at one side for wire bonding)





Module: local support + chips + FPC

Module of inner layer:
10 chips on both sides of each.



Module of outer two layers:
20 chips on both sides of each.