Update on CMOS/MOST1 and SOI pixel R&D

Yunpeng Lu and Qun Ouyang

IHEP
On behalf of the study group
CEPC Day / June 15, 2020

Outline:

- Introduction
- Update on JadePix3 and CPV3
- Perspective for next 5 years

* contents will be reported: “Development of high resolution low power silicon pixel sensors for the CEPC vertex detector”, ICHEP2020, ID #394

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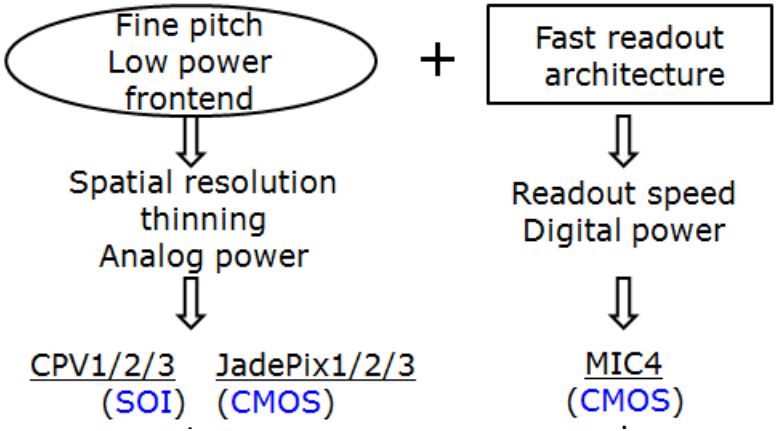
Institute of High Energy Physics
Chinese Academy of Sciences
華中師範大學
大連民族大學
Dalian Minzu University
山东大学
SHANDONG UNIVERSITY

Introduction

	Process	International collaborators	Objectives of the project	Anticipated schedule	Leading institutions
MOST1	CMOS	Strasburg IPHC	Small pixel size design with in-pixel digitization and low power frontend	2016.6-2021.5	IHEP, CCNU
NSFC	SOI	KEK/SOIPIX collaboration	Verification of SOI process with small pixel size and low noise design	2016.1-2019.12	IHEP

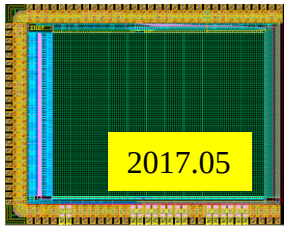
Towards Baseline Requirements: CMOS and SOI R&D in Synergy



Developed CMOS Pixel Sensor funded by MOST1

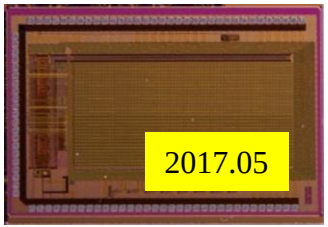
Prototype	Pixel size (μm^2)	Collection diode bias (V)	In-pixel circuit	R/O architecture	Main goals	Status
JadePix2	22 × 22	< 10 V (ac-coupled)	amp., discriminator, binary output	Rolling shutter	Small pixel, Power < 100 mW/cm^2	Electrical functionality verified
MIC4	25 × 25	reverse bias	Low power front-end, address encoder	Data-driven, Asynchronous	Small pixel, fast readout	Electrical functionality verified
JadePix3	16 × 26 16 × 23.11	reverse bias	Low power front-end, binary output	Rolling shutter with end of col. priority encoder	Small pixel, low power	Production finished

All prototypes in TowerJazz 180 nm CIS process



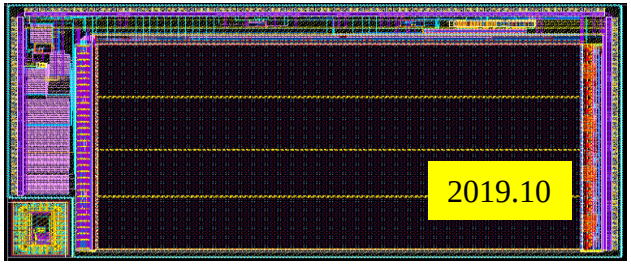
JadePix2 (IHEP) 3 × 3.3 mm^2

To be published in NIMA



MIC4 (CCNU & IHEP) 3.2 × 3.7 mm^2

NIMA 924(2019) 82-86



JadePix3 (IHEP, CCNU, Dalian Minzu Unv., SDU)

10.4 × 6.1 mm^2

Developed SOI Pixel Sensor funded by NSFC

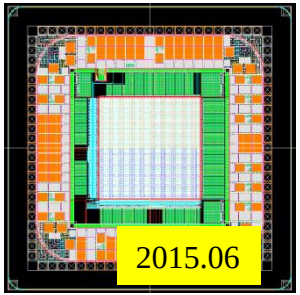
Prototypes in LAPIS 200nm Double-SOI process

- 16μm *16μm with in-pixel discrimination
- Double-SOI process for shielding and radiation enhancement

- Thinned down to 75μm thick
- Temporal noise ~6e$^-$
- Threshold dispersion (FPN) ~114e$^-$
- Single point resolution ~2.3μm measurement under infrared laser beam

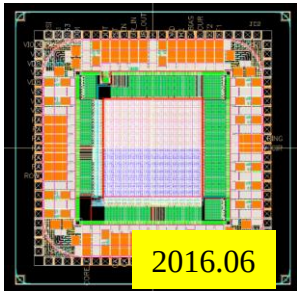
LAPIS 200nm Pinned Depleted Diode process

- Dedicated bias scheme to minimize capacitance
- Optimized for low FPN 12e$^-$
- Pixel matrix divided as 45 regions, to verify design options



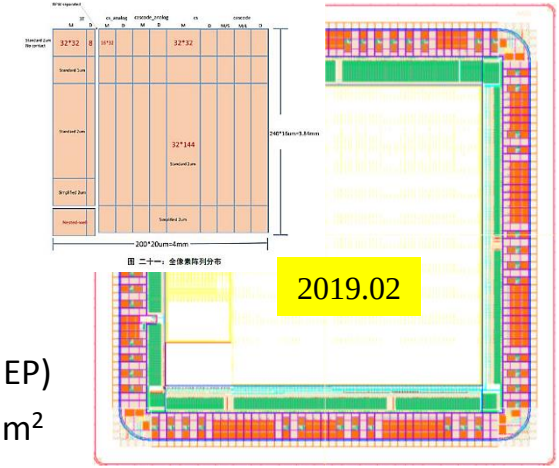
CPV1 (IHEP)

3 ×3 mm^2



CPV2 (IHEP) 3 × 3 mm^2

NIMA 924(2019) 409-416



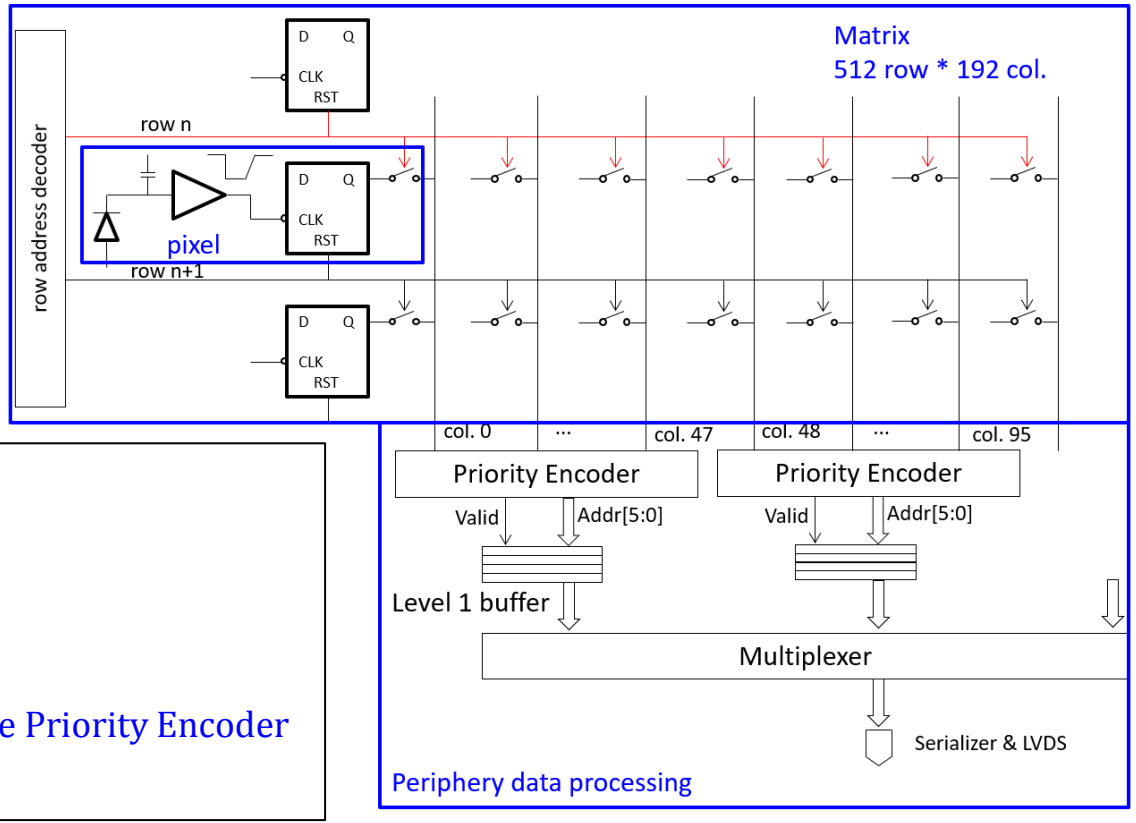
CPV3 (IHEP)

6 × 6 mm^2

JadePix3: fully functional prototype with small pixel design

Small pixel: Low power FE + Rolling shutter Readout

- **Specification:**
- Spatial resolution
  - ~ 3um
  - Initial pixel size 16um×20um
  - FPN < 20e-
- Power consumption
  - < 100mW/cm^2
  - Measureable



- **Rolling shutter readout**
  - 512 row * 192 col
  - One row selected at a time
  - 102 us to finish 512 rows
  - Every 48 columns fed into the Priority Encoder at the end of columns.

JadePix3: chip status

- Submitted in Oct. 2019
- Process finished in May 23rd 2020
- Diode, minimum size
  S_{diode}=4μm², $S_{footprint}$=36μm², C_{diode}~4-5fF
- Front-end, 2 versions
  - FE_V0, FE_V1 (20nA, 60nA)
- Pixel digital, 3 versions
  - DGT_V0, DGT_V1, DGT_V2
- Pixel area
  - 16×26 μm²
  - 16×23.11 μm²

Sector	Diode	Front-end	Pixel digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	**16×26 μm²**
1	2 + 2 μm	FE_V0	DGT_V1	**16× 26 μm²**
2	2 + 2 μm	FE_V0	DGT_V2	**16× 23.11 μm²**
3	2 + 2 μm	FE_V1	DGT_V0	**16×26 μm²**

Design team

IHEP: Yunpeng Lu, Ying Zhang, Yang Zhou, Zhigang Wu, Qun Ouyang
CCNU: Ping Yang, Weiping Ren, Le Xiao, Di Guo, Chenxing Meng, Anyang Xu, Xiangming Sun
Dalian Minzu Unv.: Zhan Shi
SDU: Liang Zhang

P Yang, CEPC workshop, Nov.2019
YP Lu, HSTD12, 14-18 Dec.2019, Hiroshima, Japan

Estimated: ~55mW/cm²:
- 9mW/cm² (pixel array)
- 30mW/cm² (zero suppression & data buffer)
- 6.25mW/cm² (Serializer)
- 5mW/cm² (PLL)
- 4mW/cm² (LVDS)

Details of design:
Full size sensor of the Silicon Vertex Detector, Wei WEI
https://indico.ihep.ac.cn/event/11068/

Plan of JadePix3 Test and JadePix4 design

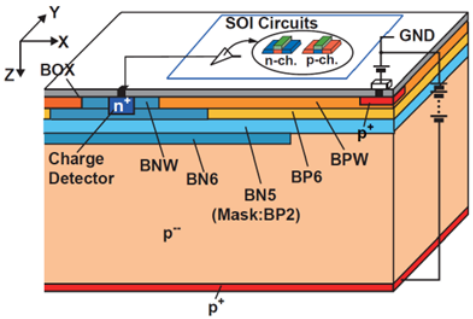
- May - Aug. 2020
  - Sub-board to mount the chip into readout system
  - Wire bonding and components loading
  - Readout system debugging
- Sep. 2020 - Feb. 2021
  - Characterization of individual parts on chip
  - Optimization of operation
  - ^{55}Fe 5.9 keV X-ray calibration
- Sometime in 2021
  - Beam test
  - JadePix4 design submission

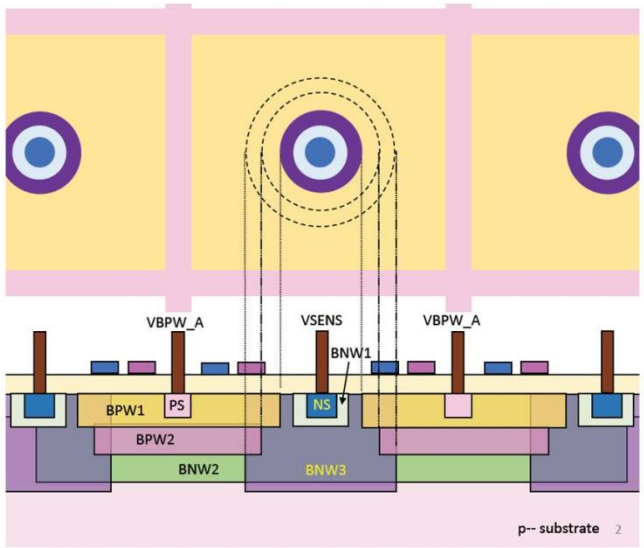
Yunpeng Lu, Wenhao Dong (USTC/IHEP)

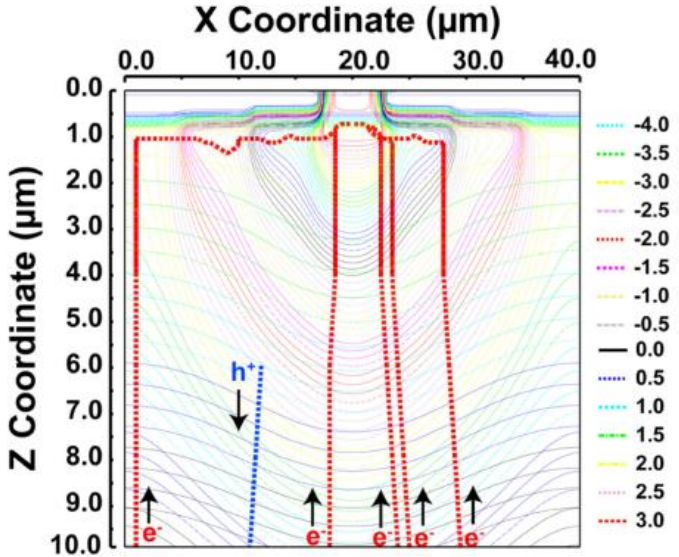
IHEP/CCNU/……

CPV3: an novel design with SOI-PDD process

- Proposed by Shoji Kawahito (Shizuoka U.)
  - Pinned Si surface layer → reduction of surface leakage by 2 orders
  - Depleted charge collection electrode → reduction of diode capacitance
  - Lateral electric field → improved charge collection efficiency



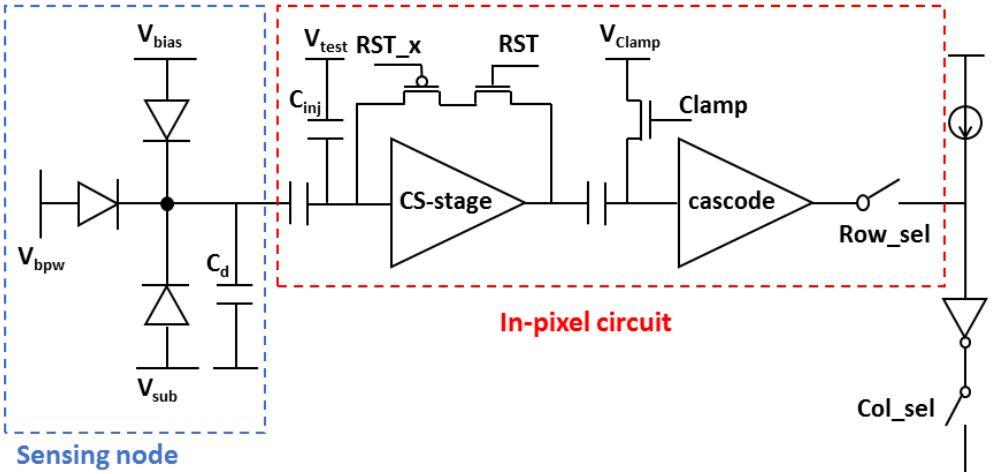


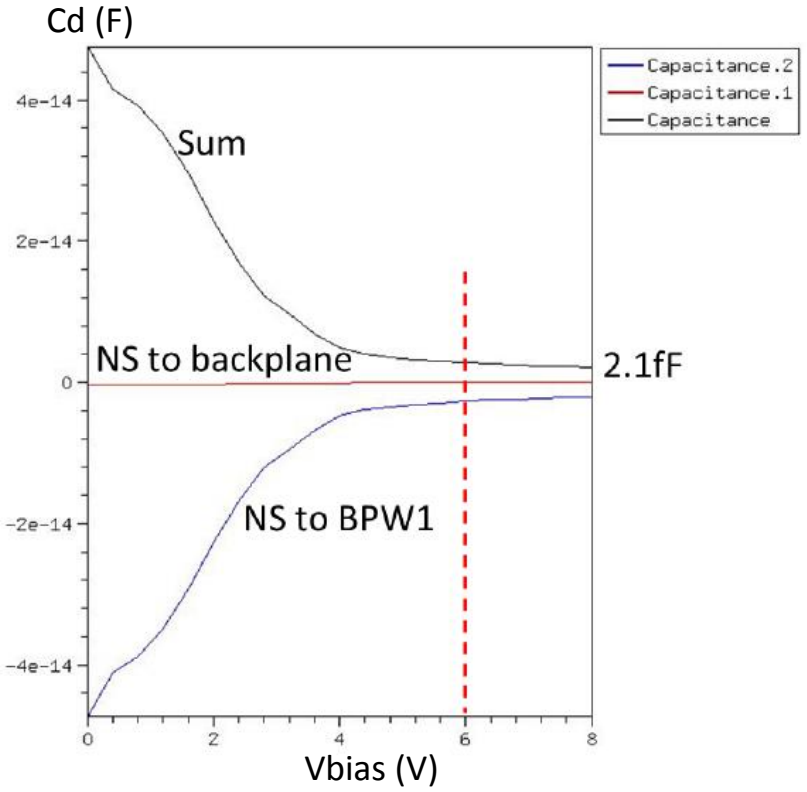


Ref: Sensors 2018, 18, 27; doi:10.3390/s18010027

Pixel design

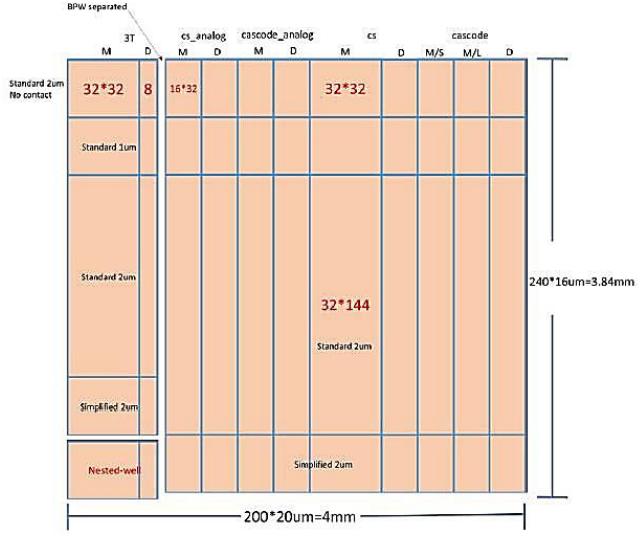
- **Sensing node AC-coupled to the amplifier to allow Vbias up to +10V**
  - Minimize the capacitance at pixel pitch 16 um * 20 um
- Common Source (CS) amplifier, 1st stage
- Cascode amplifier, 2nd stage
- Statistical simulation, FPN = 12 e- * CPV2: 114 e-

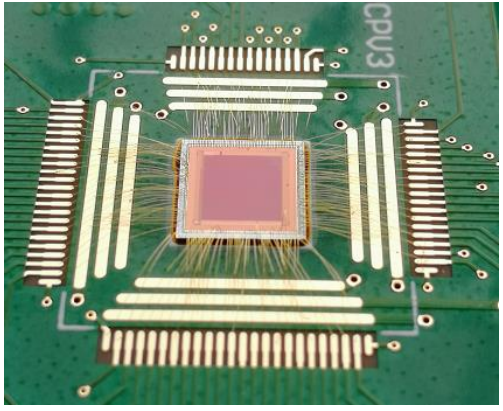




Status of CPV3

- Design team: Zhigang Wu, Yunpeng Lu
- Mask area: 6mm×6mm
  - Optimized for low FPN
  - Pixel matrix divided as 45 regions, to verify design options
  - Rolling shutter readout
- Summitted Feb, 2019
  - Delivered in Oct. 2019
  - Testing is ongoing





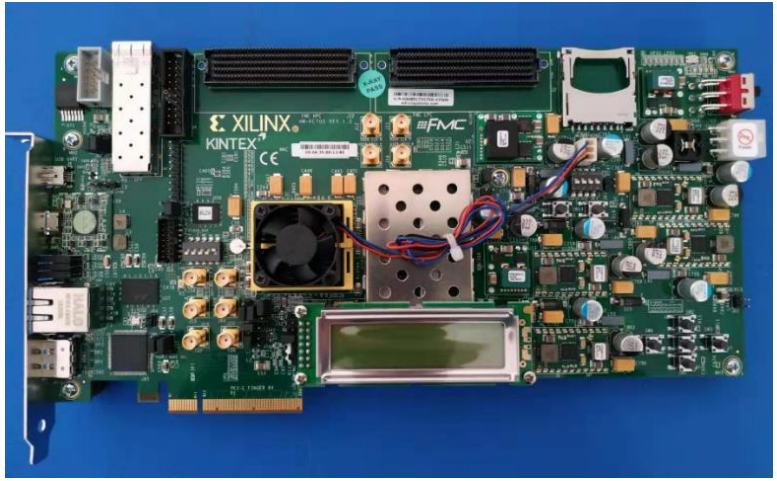
YP Lu, CEPC workshop, Nov.2019, Beijing
ZG Wu, HSTD12, 14-18 Dec.2019, Hiroshima, Japan

Readout System

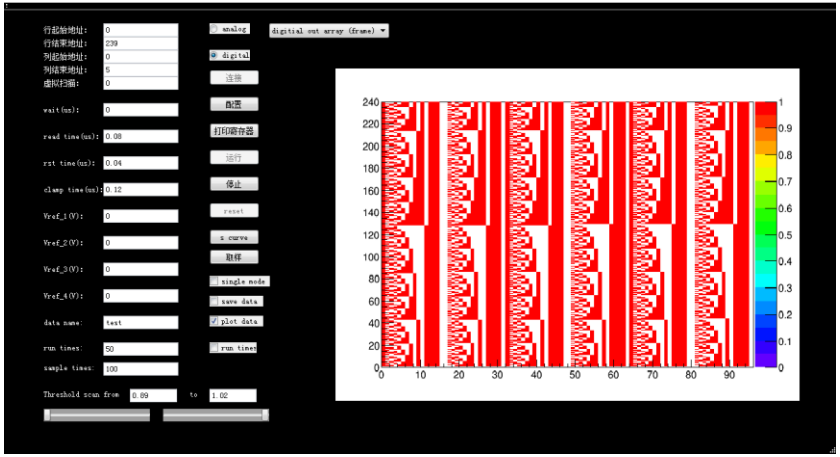
- FPGA board + Chip adaptor
  - Commercially available KC705
  - Gigabit Ethernet
  - DAQ code developed with Qt/C++
- Minor change to adapt to different chips

Chip Adaptor

FPGA Board

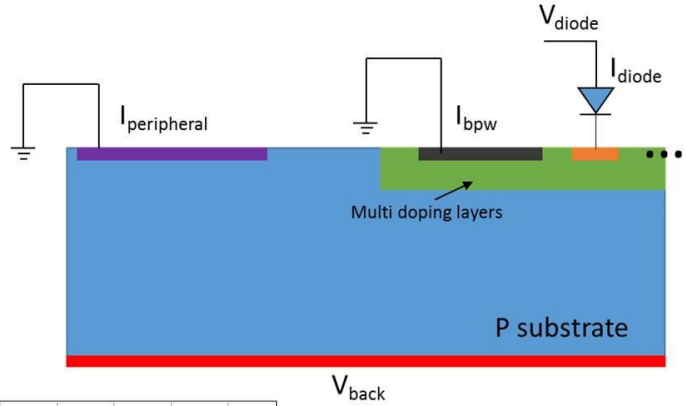


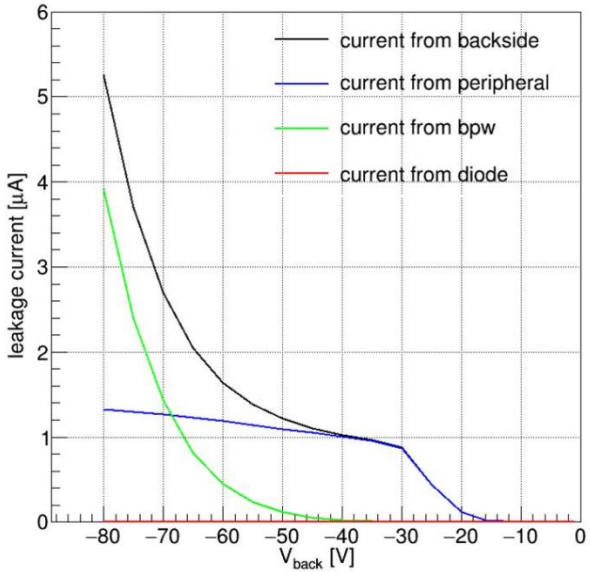
DAQ GUI

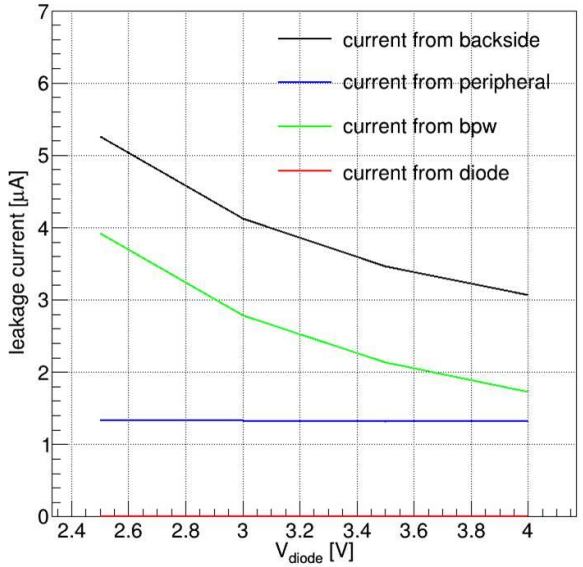


I-V test of sensor

- Leakage current components
  - Current from diode
  - Current from bpw
  - Current from peripheral
- Vdiode = +4V suppressed leakage on bpw and peripheral

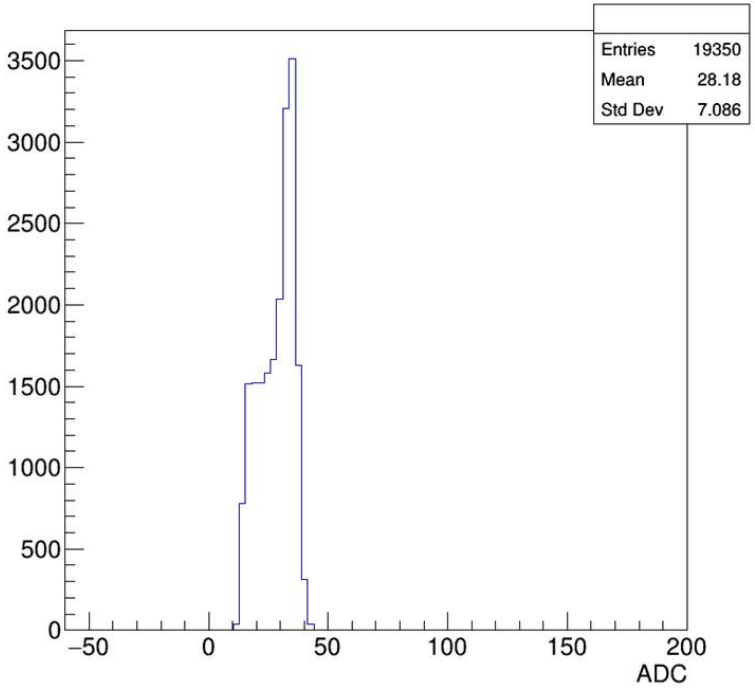


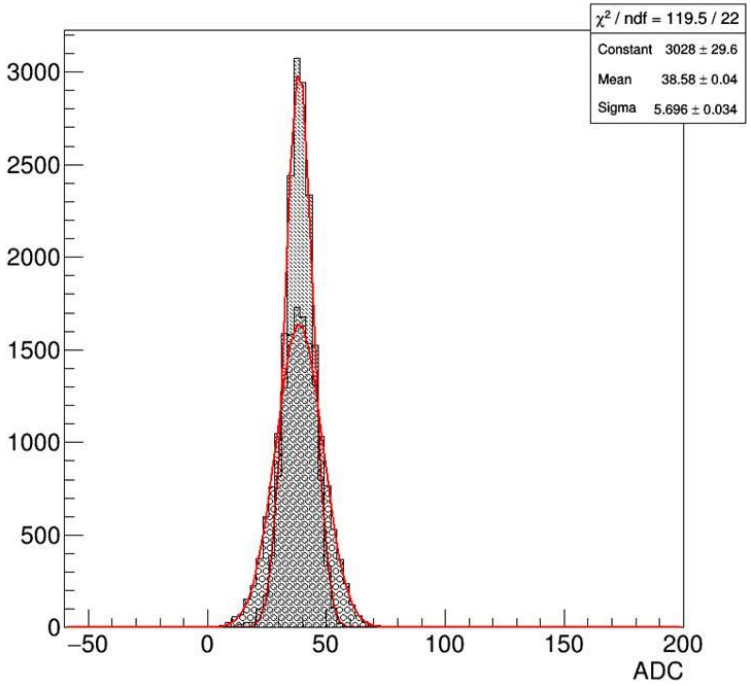




^{55}Fe X-ray Calibration

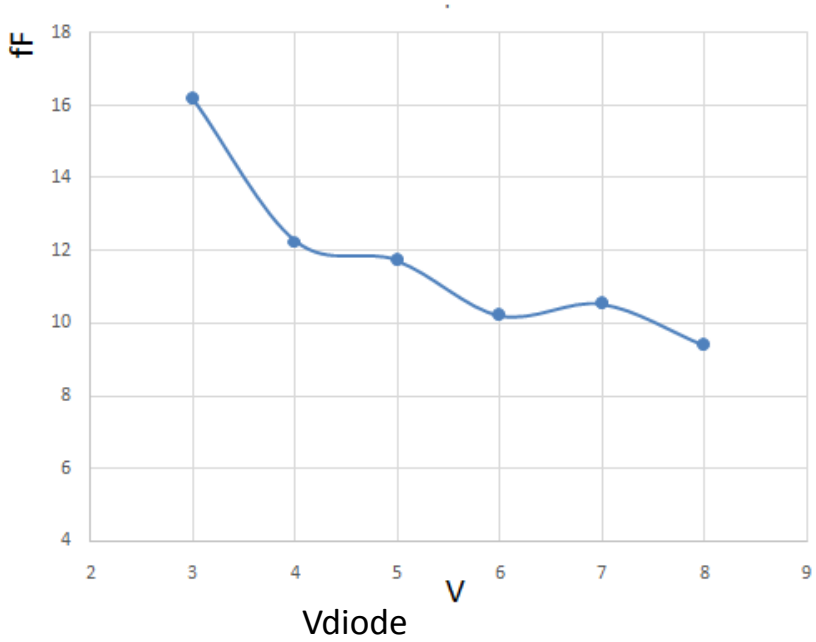
- Vdiode=+4V , Vbpw=0V , Vback=-60V
- Charge collected in a 3*3 cluster
- Wider peak spread of 5*5 cluster due to electrical noise
- Equivalent Cd = 12fF

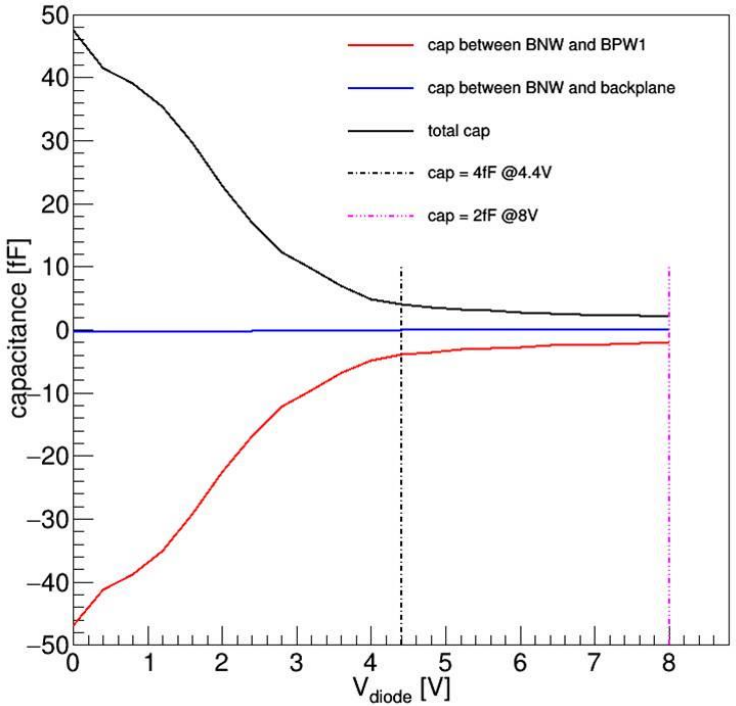




Reduction of Cd

- Vback=-60V，Vbpw=0V，increase Vdiode
  - Proof of PDD bias concept
- Expected to be 4fF@4.4V
  - Parasitic capacitance ?
  - To be confirmed by RC extraction (simulation)





More test to do

- To assemble more chips and adaptor cards
  - Compare different chips
- Optimize the operation of pixel circuit
  - Compare different structures
- Noise and threshold measurement

Try to be done by the end of year

Yunpeng Lu, Jing Dong

- Laser test or beam test, depending on
  - the outcome of full characterization
  - and possible scheme together with JadePix3

early of next year

Reminder

Vertex Detector Requirements

- Efficient tagging of heavy quarks (b/c) and τ leptons

  ⟶ impact parameter resolution

$$\sigma_{r\phi} = 5 \oplus \frac{10}{p(GeV)\,\sin^{3/2}\theta}\,(\mu m)$$

- Detector system requirements:
  - σ_{SP} near the interaction point: *<3 μm* ⟶ ~16μm pixel pitch
  - material budget: *≤ 0.15%X $_0$/layer* ⟶ power consumption < 50mW/cm^2 , if air cooling used
  - first layer located at a radius: *~1.6 cm*
  - pixel occupancy: *≤ 1 %* ⟶ ~ μs level readout

MOST1?

MOST2?

Target: fine pitch, low power, fast pixel sensor + light structure

Report of the Review of the Circular Electron Positron Collider Conceptual Design Report

Vertex Detector

Findings: there is active R&D and groups are making good progress, building on large effort by the international community. Compared to other efforts toward precise and transparent vertex detectors, CEPC (with its 100% duty cycle) should place stronger emphasis on power management. Advanced processes like 65 nm CMOS or 3D-integrated devices should be pursued actively and can have a big impact on the vertex detector performance.

R42: CEPC should develop an installation scheme for all detectors, where the Vertex Detector can be installed last and access to replace the vertex detector is possible.

R43: CEPC should keep a close eye on the power consumption an active cooling system impact of the cooling on the material budget needs to be understood, especially if air cooling is insufficient.

R44: Collaboration between the Vertex and MDI group is good, and should be further strengthened.

Vertex system revisited at the post-CDR stage

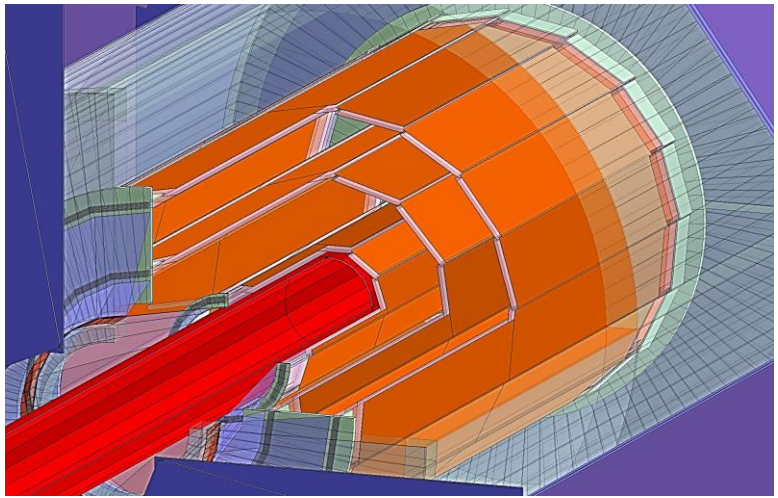


Table 1. Design parameters of the CEPC vertex system.

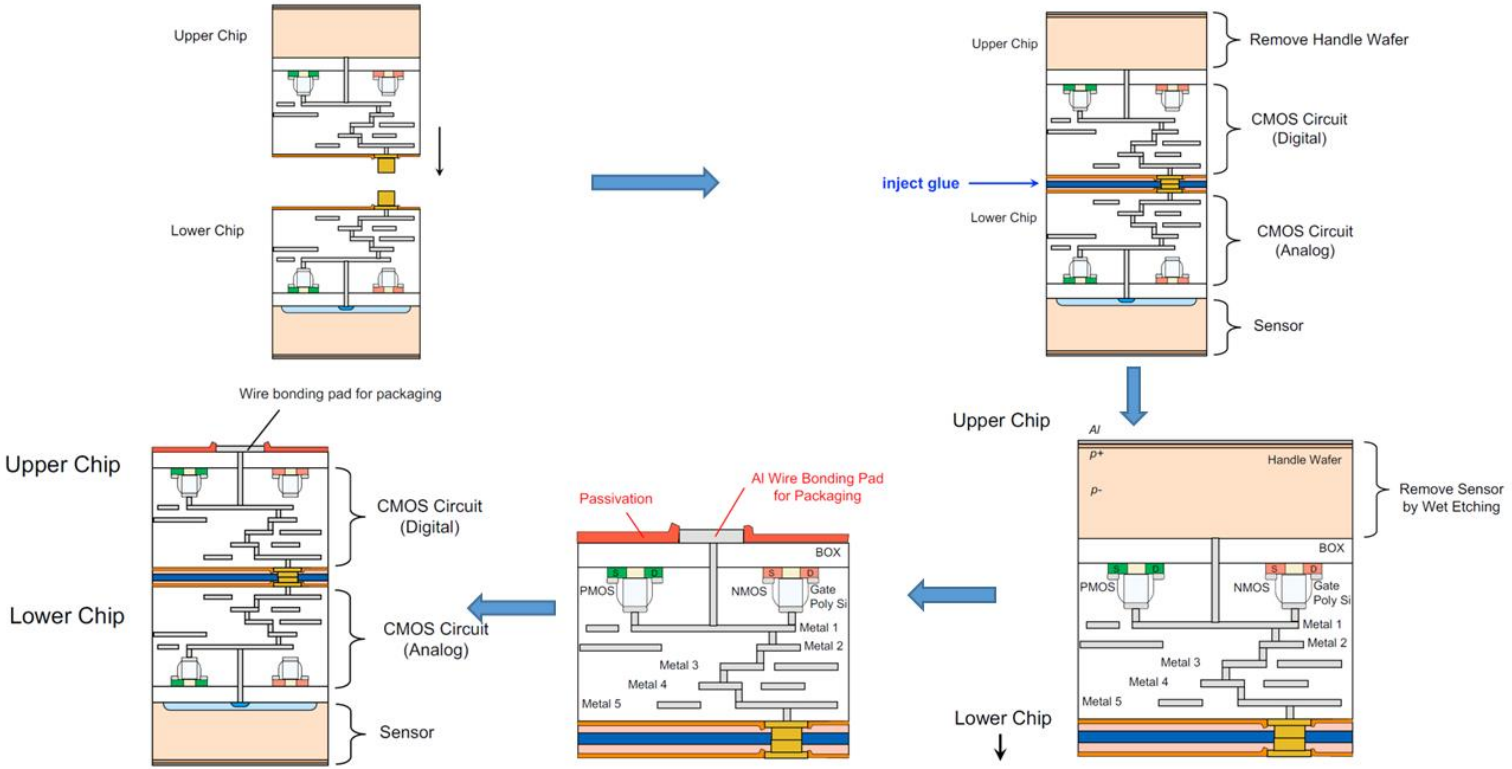
	R(mm)	| Z |(mm)	$\sigma(\mu m)$	material budget
Layer 1	16	62.5	2.8	0.15%/X_0
Layer 2	18	62.5	6	0.15%/X_0
Layer 3	37	125.0	4	0.15%/X_0
Layer 4	39	125.0	4	0.15%/X_0
Layer 5	58	125.0	4	0.15%/X_0
Layer 6	60	125.0	4	0.15%/X_0

- Optimization for system requirements: which could be loose, or already too loose?
  radiation level, dedicated Z-pole vertex?
- New concept of layout?
- New process helpful? time & resources needed
  - 110nm → LFoundry CiS explored by ARCADIA project, INFN
  - 65nm → TJ CiS explored by CERN
  - 3D → SOI-3D accessible via SOIPIX, but a lot still need to be verified
  - Ultra-light, self-supported pixel layer?

SOI based 3D integration

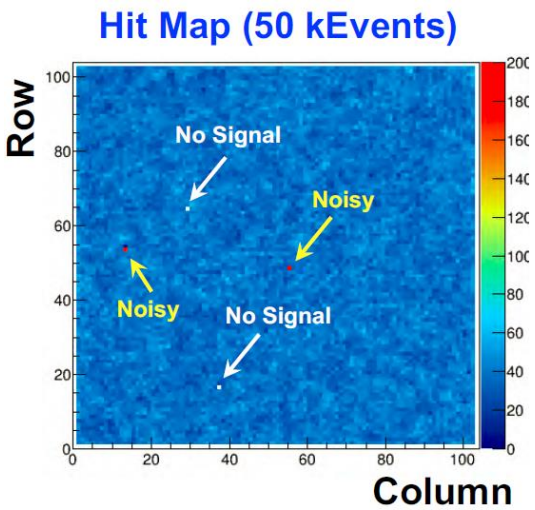
- The lower tier can be **either SOI or CMOS** pixel sensor
- 3D integration can be greatly simplified by using SOI as the upper tier
  - Etching of through via
  - Removal of handle wafer

T-Micro process



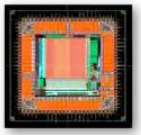
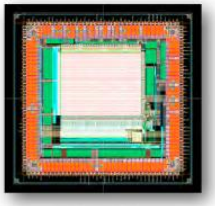
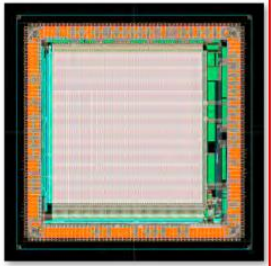
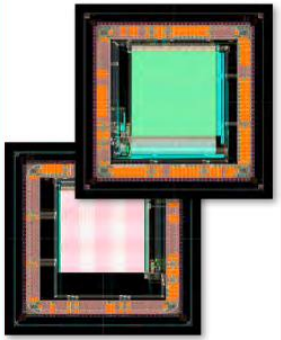
Demonstrated SOFIST 3D chip for ILC

Miho Yamada, 3D Integrated Pixel Sensor with Silicon-on-Insulator Technology for the International Linear Collider Experiment, IEEE 3DIC, Sendai, October 8th, 2019



Connection yield > 99.9%

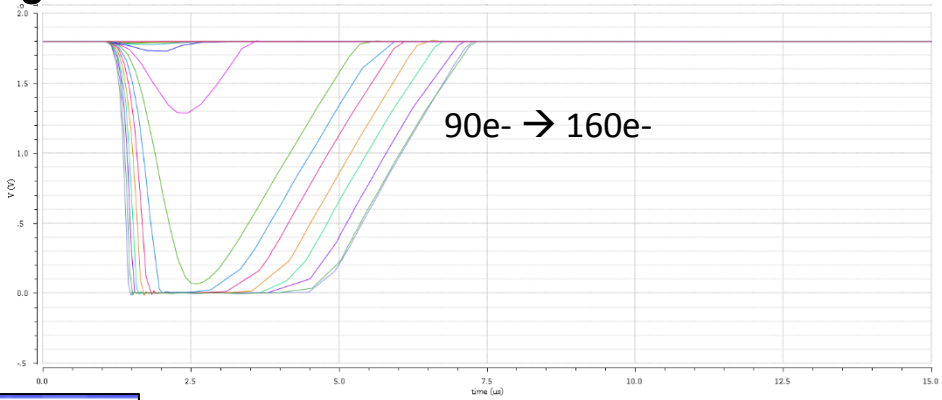
SOFIST

	SOFIST1	SOFIST2	SOFIST3	SOFIST4 (3D)
	Beam test at FNAL in Jan. 2017 Analog signal	Beam test at FNAL in Feb. 2018 Analog signal or Timestamp	Beam test at FNAL in Feb. 2019 Analog signal and Timestamp	3D integration by T-Micro
				
Chip Size (mm^2)	2.9 × 2.9	4.45 × 4.45	6 × 6	4.45 × 4.45
Pixel Size (μm^2)	20 × 20	25 × 25	30 × 30	20 × 20
Pixel Array	50 × 50 (Analog Signal)	64 × 64 (Time Stamp) 16 × 64 (Analog Signal)	128 × 128 (Analog signal and Time stamp)	104 × 104 (Analog signal and Time stamp)
Functions (Pixel)	Pre. Amplifier (CSA) Analog signal memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 2) Analog signal memory (2 hits) or Time stamp memory (2 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 3) Analog signal memory (3 hits) Time stamp memory (3 hits)	Pre. Amplifier (CSA) Comparator (Chopper inverter) Shift register (DFF × 3) Analog signal memory (3 hits) Time stamp memory (3 hits)
Functions (On Chip)	Column ADC (8 bit)	Column ADC (8 bit) Zero-suppression logic	Column ADC (8 bit)	Column ADC (8 bit)
Wafer	FZ *n*-type (Single SOI)	Cz *p*-type (Double SOI)	FZ *p*-type (Double SOI)	FZ *p*-type (Double SOI)
Wafer Resistivity (kΩ·cm)	2 ≤	1 ≤	3 - 10	3 - 10
Status	Delivered (Dec. 2015) Position resolution ~1.4 μm	Delivered (Jan. 2017) Time resolution ~1.55 μs	Delivered (May. 2018) Under evaluation	Delivered (Jan. 2019 ~)

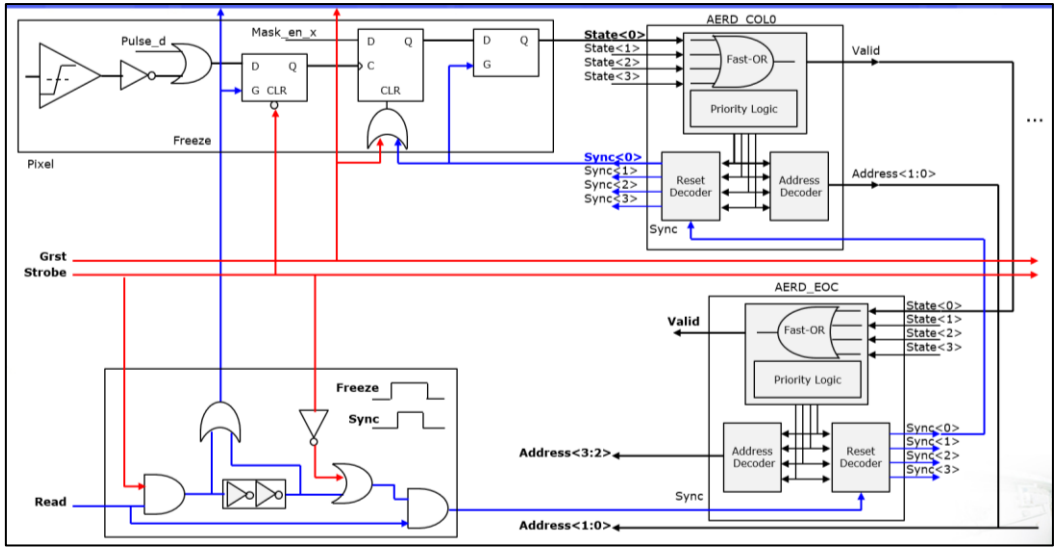
Development of SOI-3D chip for CEPC

— NSFC funding 2020.01-2024.12

- Faster and low power
  - Readout time ~ 1us, hit registered at the fast falling edge
  - Power consumption ~ 50mW/cm^2
  - Shrink the pixel size by SOI-3D
- Continuous readout mode (AERD)
  - Compatible with trigger mode



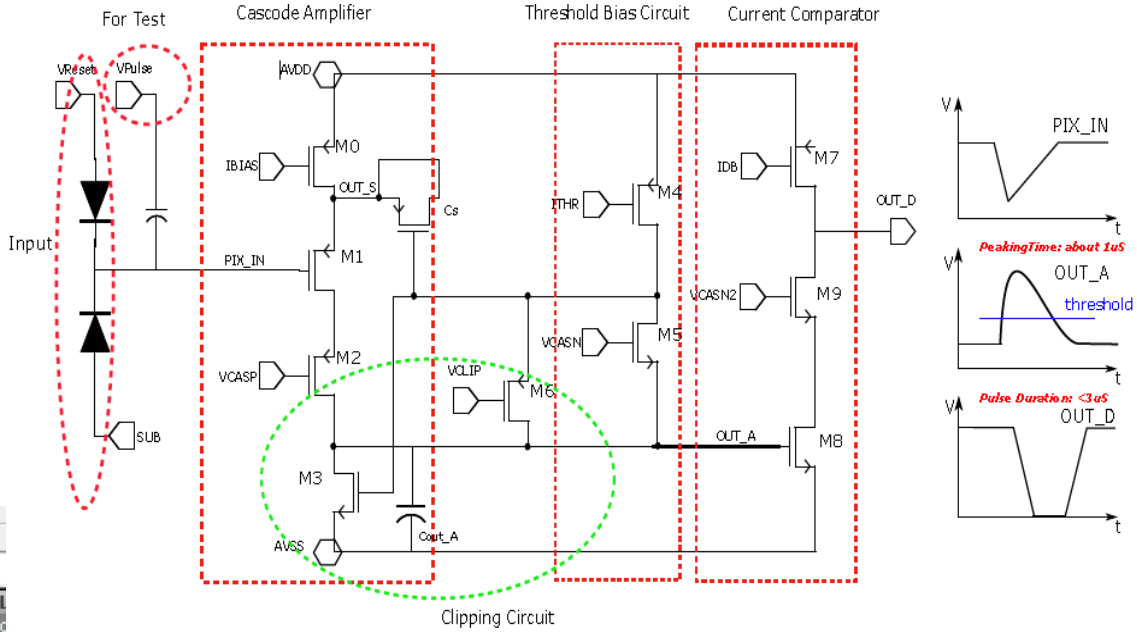
Output Waveform of Discriminator

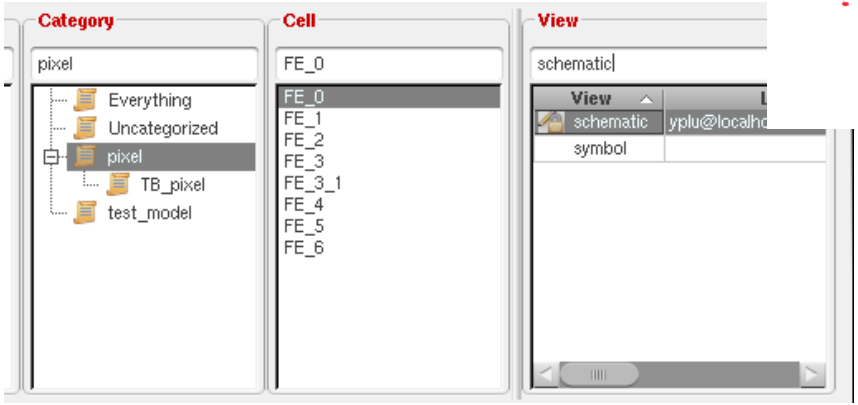


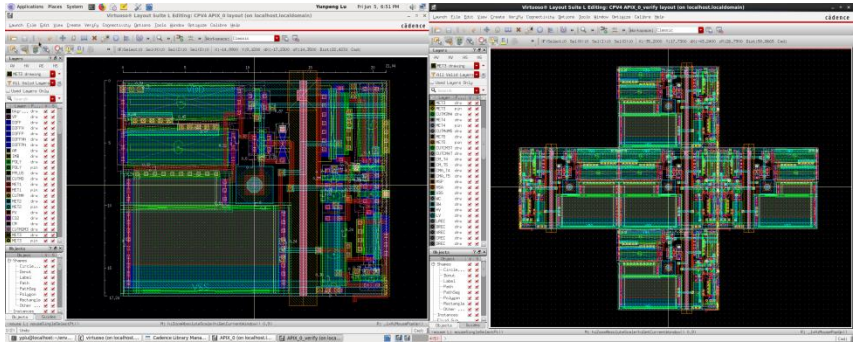
CPV4-3D design

Yunpeng Lu, Yang Zhou, Wenhao Dong (USTC/IHEP)

- Pixel design iteration
  - Minimum threshold 85 e^-
  - ENC ~ 1.3 e^- (pre-layout)
  - Compatible with SOI-PDD
- 90 work days allocated
  - Upper tier: digital
  - Lower tier: analog
- Exploring TID hardening
- Submission plan ~Oct. 2020

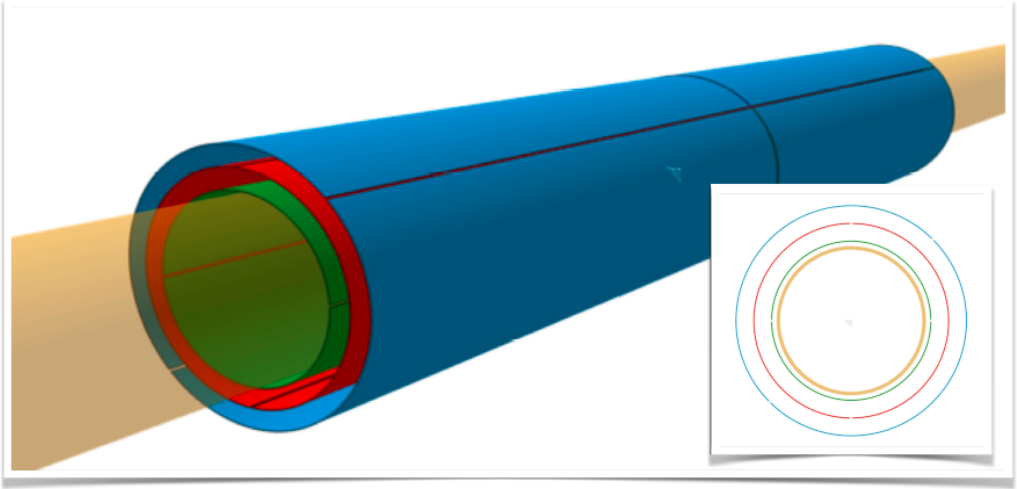






pixel layout (analog): 17 μm ×21 μm

ALICE ITS3 with stitching CMOS technology



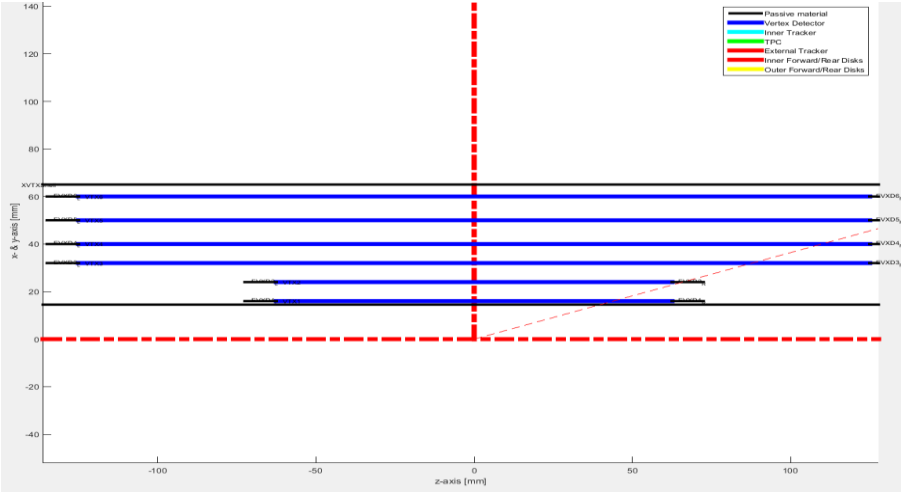
Beam pipe Inner/Outer Radius (mm)	16.0/16.5		
IB Layer Parameters	Layer 0	Layer 1	Layer 2
Radial position (mm)	18.0	24.0	30.0
Length (sensitive area) (mm)	300		
Pseudo-rapidity coverage	±2.5	±2.3	±2.0
Active area (cm^2)	610	816	1016
Pixel sensor dimensions (mm^2)	280 x 56.5	280 x 75.5	280 x 94
Number of sensors per layer	2		
Pixel size (μm^2)	O (10 x 10)		

- New beam pipe:
  - "old" radius/thickness: 18.2/0.8 mm
  - new radius/thickness: 16.0/0.5 mm
- Extremely low material budget:
  - Beam pipe thickness: 500 µm (0.14% X0)
  - Sensor thickness: 20-40 µm (0.02-0.04% X0)
- Material homogeneously distributed:
  - essentially zero systematic error from material distribution

Similar layout with CEPC layer 1-3

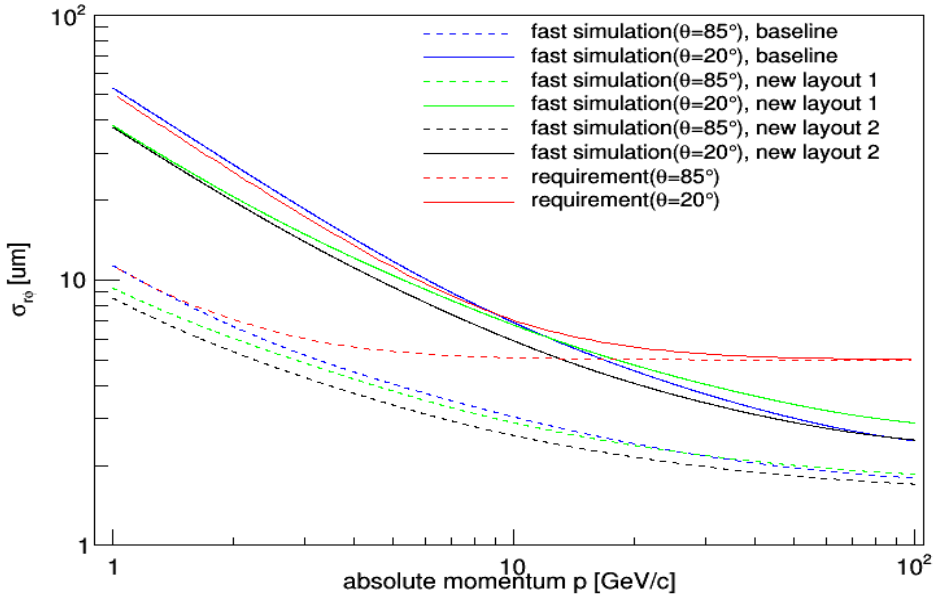
An ultra light structure vertex layout

	R(mm)	|Z|(mm)	σ(*μm*) (layout1/layout2)	material budget
Layer1	16	62.5	4/2.8	0.05%X_0
Layer2	24	62.5	4/4	0.05%X_0
Layer3	32	125	4/4	0.05%X_0
Layer4	40	125	4/4	0.05%X_0
Layer5	50	125	4/4	0.05%X_0
Layer6	60	125	4/4	0.05%X_0



- Technology to be explored
- Joint effort of CCNU (Xiangming Sun) and IHEP (Yunpeng Lu)

Zhigang Wu, Optimization on silicon detectors at CEPC, CEPC workshop, Nov.2019, Beijing

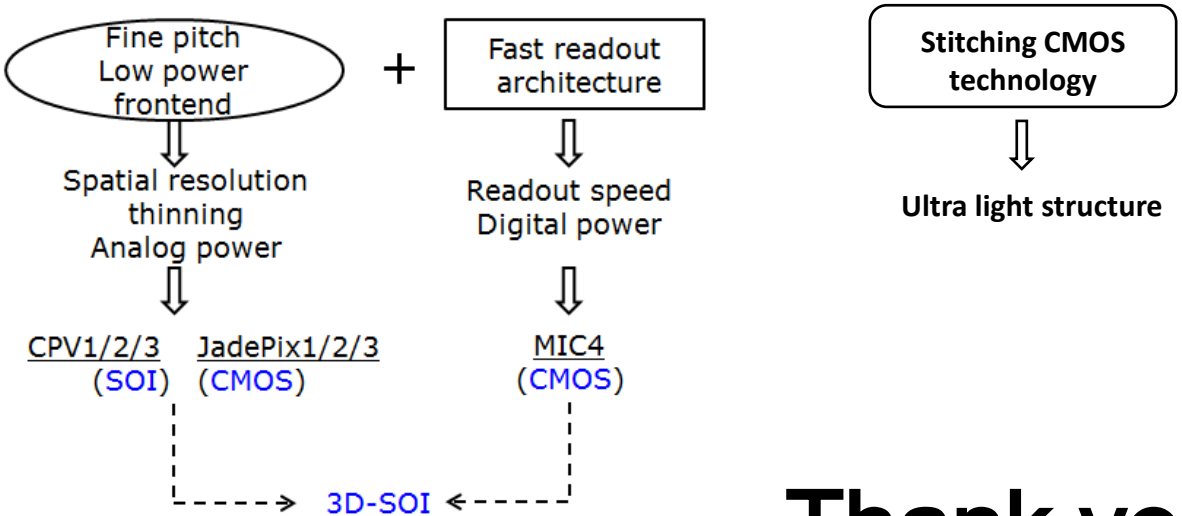


Comparing with baseline layout

- better performance (~20% improvement) for layout1 at low momentum, but poor performance at high momentum
- both within the requirement

Summary

- CMOS and SOI development in synergy
  - Following the same roadmap
  - Using the same readout system
- JadePix3 and CPV3 tests in parallel
- CPV4-3D design is ongoing, similar design scheme for JadePix4
- Stitching CMOS technology will be explored

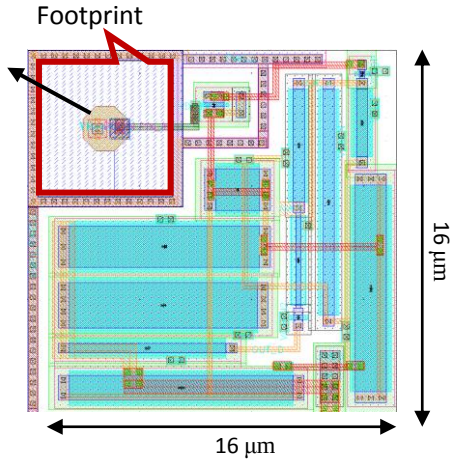


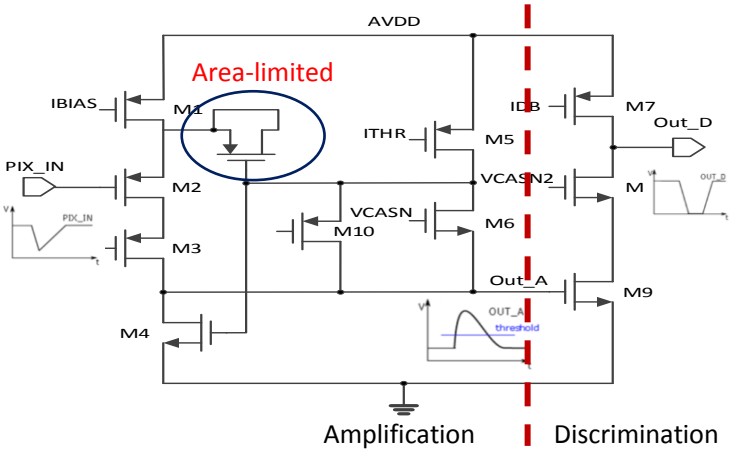
Thank you!

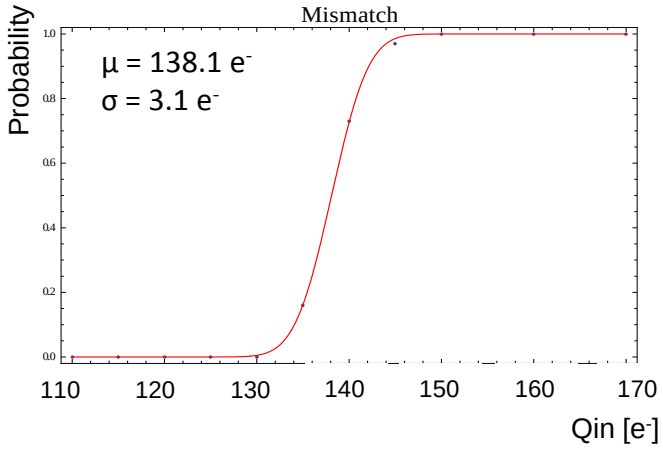
Backup

JadePix3: Diode & Front-end design

- Design goals: small pixel size and low power consumption
- Sensing diode: negatively biased for high Q/C
  - Electrode size 4 µm², with a small footprint 36 µm²
- Frontend: tradeoff between layout area and FPN
  - Reduction on the layout area, ~200 µm²
  - Improvement on the FPN = 3.1e⁻ (simulation)
  - A low power version (20nA), equivalent to 9 mW/cm²

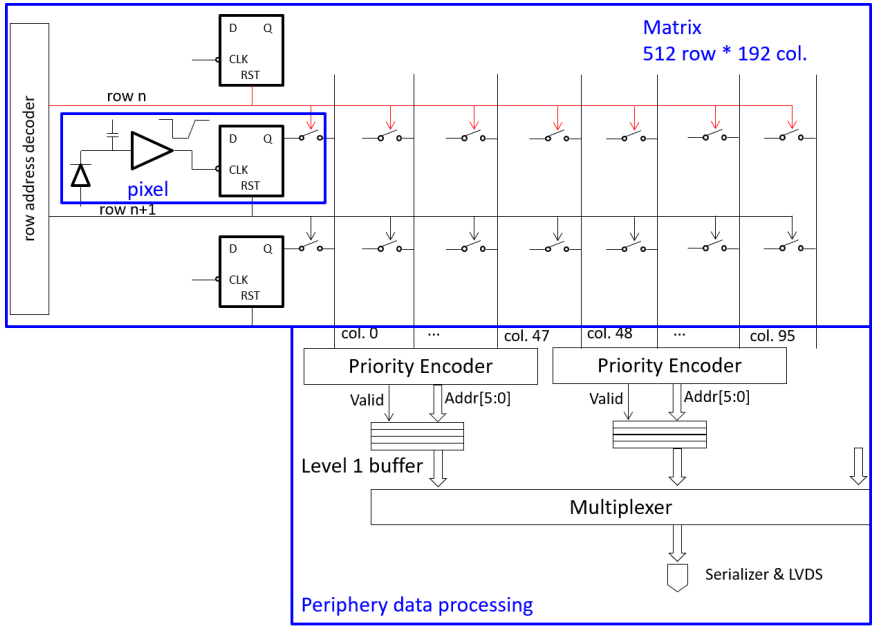




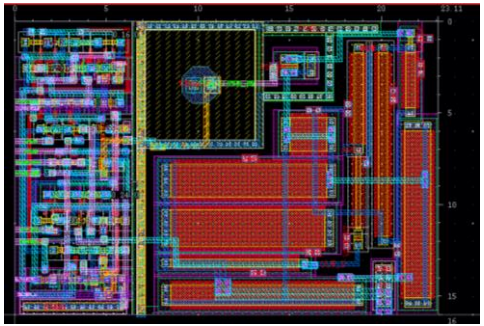


JadePix3: Rolling shutter readout of matrix

- In-pixel circuit
  - Low power binary front-end
  - Optimized DFF
- **Rolling shutter** readout
  - 512 row * 192 col.
  - One row selected at a time
  - 102 us to finish 512 rows
  - Every 48 columns fed into the Priority Enc at the end of columns.
- Minimum pixel size 16× 23.11 μm²
  - 4 variants to investigate possible optimiza



Sector	Diode	Front-end	Pixel digital	Pixel layout
0	2 + 2 μm	FE_V0	DGT_V0	16×26 μm²
1	2 + 2 μm	FE_V0	DGT_V1	16× 26 μm²
2	**2 + 2 μm**	**FE_V0**	**DGT_V2**	**16× 23.11 μm²**
3	2 + 2 μm	FE_V1	DGT_V0	16×26 μm²

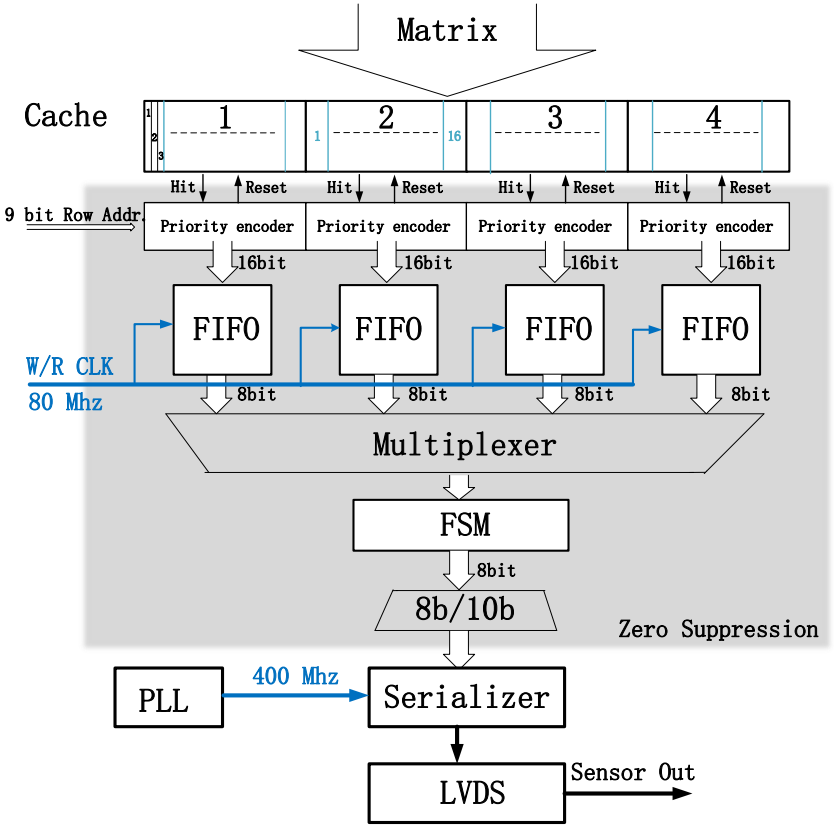


JadePix3: Periphery data processing

- Zero suppression at the end of column
  - Each 48 columns divided into 16 blocks
  - ‘Fired’ blocks identified sequentially by a 4-bit priority encoder
  - 12.5 ns * 16 blocks = 200 ns/row
- Only hit information fed into FIFO

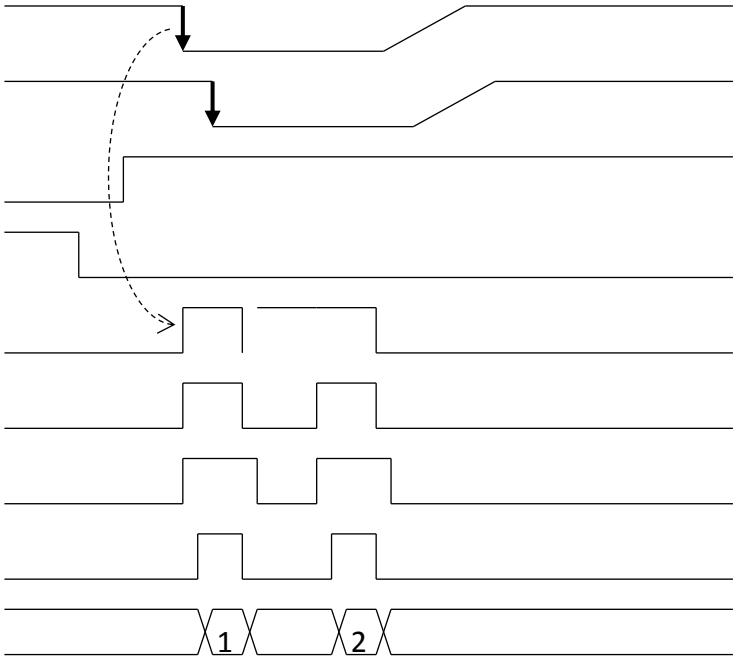
Row #	Block #	hits in block
9-bit	4-bit	3-bit

  - FIFO R/W clk: 80 MHz
  - FIFO depth: 48
- Data stream steered by a Finite State Machine
- Data after 8b/10b: 800 Mbit/s
- Estimated Power consumption 76mW
  - 15mW (Zero suppression), 25mW (Serializer), 20mW (PLL), 16mW (LVDS)

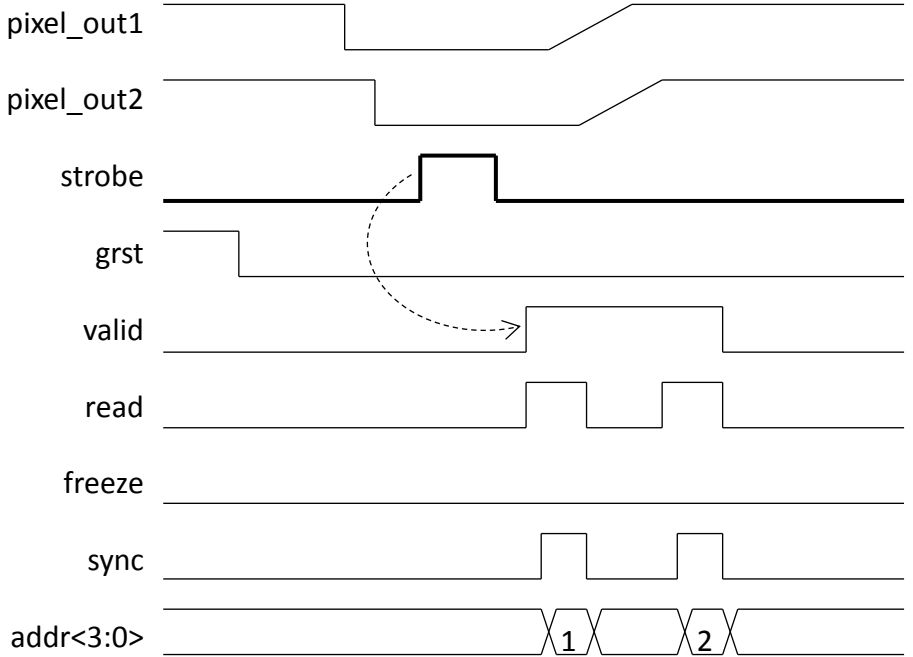


CPV4-3D: Readout mode

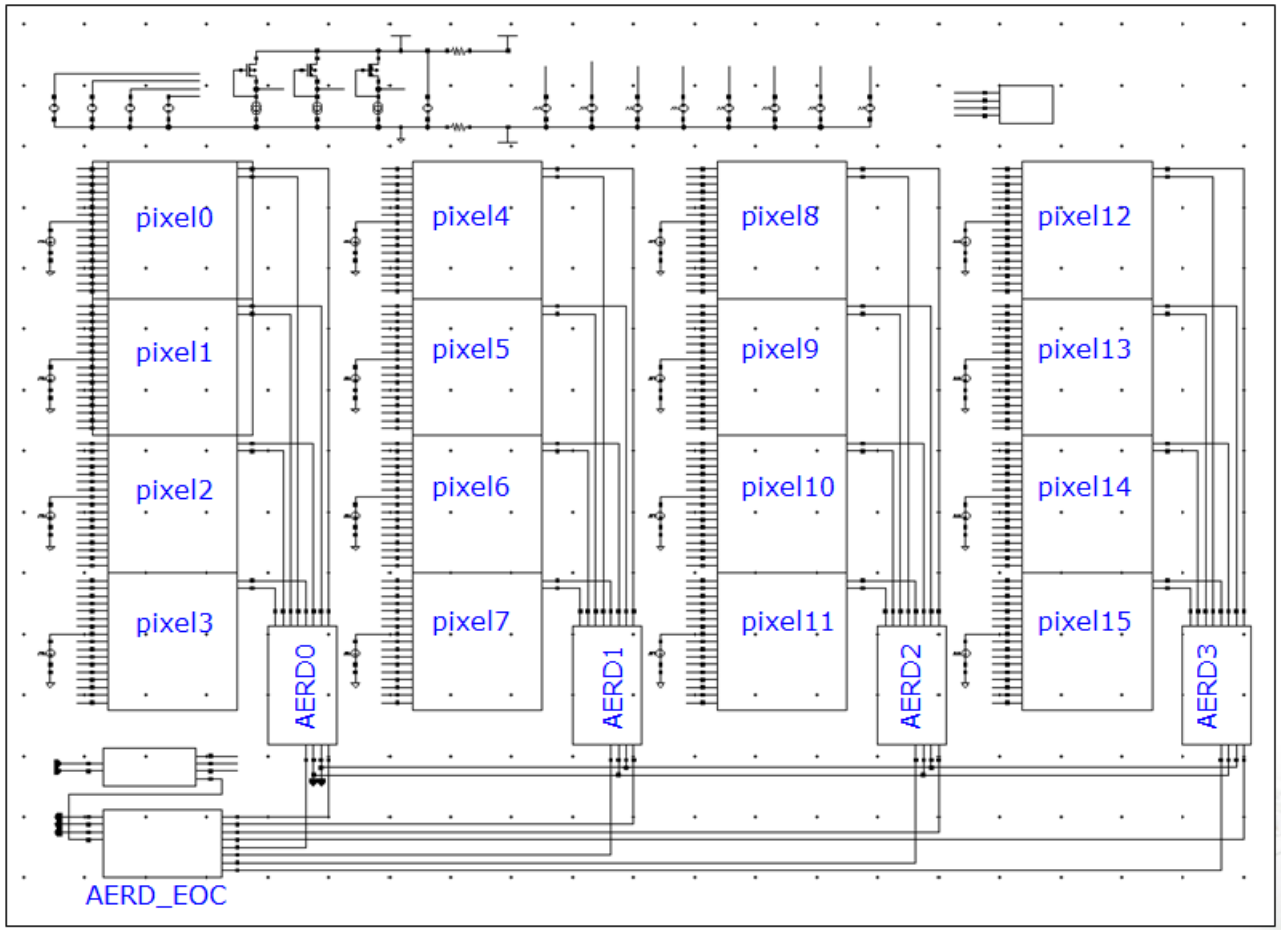
- Continuous readout
  - strobe == 1
  - Timing by falling edge ~1us



- Triggered readout
  - Strobe as gate signal
  - Timing by trigger ~5us



CPV4-3D: Verified on a Mini-Matrix design



Matrix identifying R&D priorities for different experiment areas

Technology Driver / Target Application	Pixel Size (Granularity)	Pixel Size (Resolution)	Radiation Hardness	Timing Resolution	Radiation Length	Collection Thinness	Cost per Area	Low Power
HL-LHC Vertex								
HL-LHC & LHCb Tracker upgrades								
LHCb Phase 3 Vertex								
Future hh Vertex								
Future hh Tracker								
Future hh HG ECAL								
Proton EDM								
Future e-h								
Nuclear Physics incl. HI & FAIR								
e^+e^- Vertex (ILC/circular)								
e^+e^- Vertex (CLIC)								
e+e- Tracker (ILC/circular)								
e^+e^- Tracker (CLIC)								
e^+e^- HG ECAL								
cLVF rare muon decays (Mu3e)								
Hadron Therapy								

Joost Vossebeld, **Silicon Detectors R&D future needs and opportunities for European collaboration,** 16/04/2018

Updated Parameters of Collider Ring since CDR

	Higgs		Z (2T)	
	CDR	Updated	CDR	Updated
Beam energy (GeV)	120	-	45.5	-
Synchrotron radiation loss/turn (GeV)	1.73	1.68	0.036	-
Piwinski angle	2.58	3.78	23.8	33
Number of particles/bunch N_e (10^{10})	15.0	17	8.0	15
Bunch number (bunch spacing)	242 (0.68μs)	218 (0.68μs)	12000	15000
Beam current (mA)	17.4	17.8	461.0	1081.4
Synchrotron radiation power /beam (MW)	30	-	16.5	38.6
Cell number/cavity	2	-	2	1
β function at IP β_x^* / β_y^* (m)	0.36/0.0015	0.33/0.001	0.2/0.001	-
Emittance $\varepsilon_x/\varepsilon_y$ (nm)	1.21/0.0031	0.89/0.0018	0.18/0.0016	-
Beam size at IP σ_x/σ_y (μm)	20.9/0.068	17.1/0.042	6.0/0.04	-
Bunch length σ_z (mm)	3.26	3.93	8.5	11.8
Lifetime (hour)	0.67	0.22	2.1	1.8
Luminosity/IP L (10^{34} cm^{-2}s^{-1})	2.93	5.2	32.1	101.6

Luminosity increase factor: × 1.8 × 3.2

Highlights and future perspective of the CEPC detector

November 2019
2019 International Workshop on the High Energy Circular Electron Positron Collider

Sarah Eno
University of Maryland

Important to do. While very stringent specs can inspire detector builders, when it comes time to build, too stringent specs can:

- can push one to immature technologies
- explode costs

Too loose specs can lead to missed physics opportunities
Nice session on Monday exploring this topic

Physics process	Measurands	Detector subsystem	Performance requirement
$ZH, Z \to e^+e^-, \mu^+\mu^-$ $H \to \mu^+\mu^-$	$m_H, \sigma(ZH)$ $\mathrm{BR}(H \to \mu^+\mu^-)$	Tracker	$\Delta(1/p_T) =$ $2 \times 10^{-5} \oplus \frac{0.001}{p(\mathrm{GeV})\sin^{3/2}\theta}$
$H \to b\bar{b}/c\bar{c}/gg$	$\mathrm{BR}(H \to b\bar{b}/c\bar{c}/gg)$	Vertex	$\sigma_{r\phi} =$ $5 \oplus \frac{10}{p(\mathrm{GeV})\times\sin^{3/2}\theta}(\mu\mathrm{m})$
$H \to q\bar{q}, WW^*, ZZ^*$	$\mathrm{BR}(H \to q\bar{q}, WW^*, ZZ^*)$	ECAL HCAL	$\sigma_E^{\mathrm{jet}}/E =$ $3 \sim 4\%$ at 100 GeV
$H \to \gamma\gamma$	$\mathrm{BR}(H \to \gamma\gamma)$	ECAL	$\frac{\Delta E}{E} =$ $\frac{0.20}{\sqrt{E(\mathrm{GeV})}} \oplus 0.01$

From CDR

Too tight?

Not enough?

Too tight?

Not enough?

Br(H->bb, cc) measurement

- Br (H -> cc) is extremely sensitive to the vertex design
- Br (H -> bb) is not really sensitive to the vertex design

Zhigang Wu, Optimization on silicon detectors at CEPC, CEPC workshop Nov.2019

	Scenario A (Aggressive)	Scenario B (Baseline)	Scenario C (Conservative)
Material per layer/X_0	0.075	0.15	0.3
Spatial resolution/μm	1.4 - 3	2.8 - 6	5 - 10.7
R_{in}/mm	8	16	23

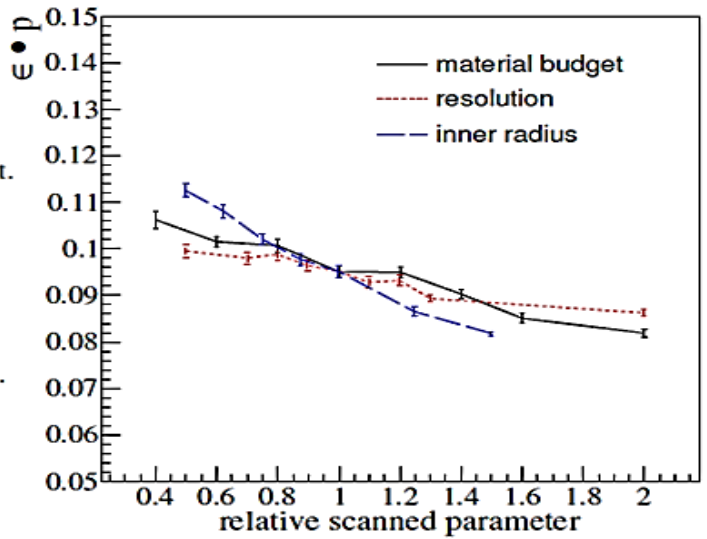
Table 3. Maximum $\epsilon \cdot p$ value comparison for the $Br(H \rightarrow c\bar{c})$ measurement.

σ_{SP}<2.8 μm very difficult

	Scenario A	Scenario B	Scenario C
$\epsilon \cdot p$	0.133 ± 0.002	0.095 ± 0.001	0.078 ± 0.001
	41%		-22%

Table 4. Maximum $\epsilon \cdot p$ value comparison for the $Br(H \rightarrow b\bar{b})$ measurement.

	Scenario A	Scenario B	Scenario C
$\epsilon \cdot p$	0.925 ± 0.001	0.914 ± 0.001	0.900 ± 0.001
	1%		-1.5%



$$\epsilon \cdot \mathrm{p} = 0.095(1 - 0.14\frac{\Delta x_{material}}{x_{material}})(1 - 0.09\frac{\Delta x_{resolution}}{x_{resolution}})(1 - 0.23\frac{\Delta x_{radius}}{x_{radius}})$$

Inner radius is the most sensitive parameter

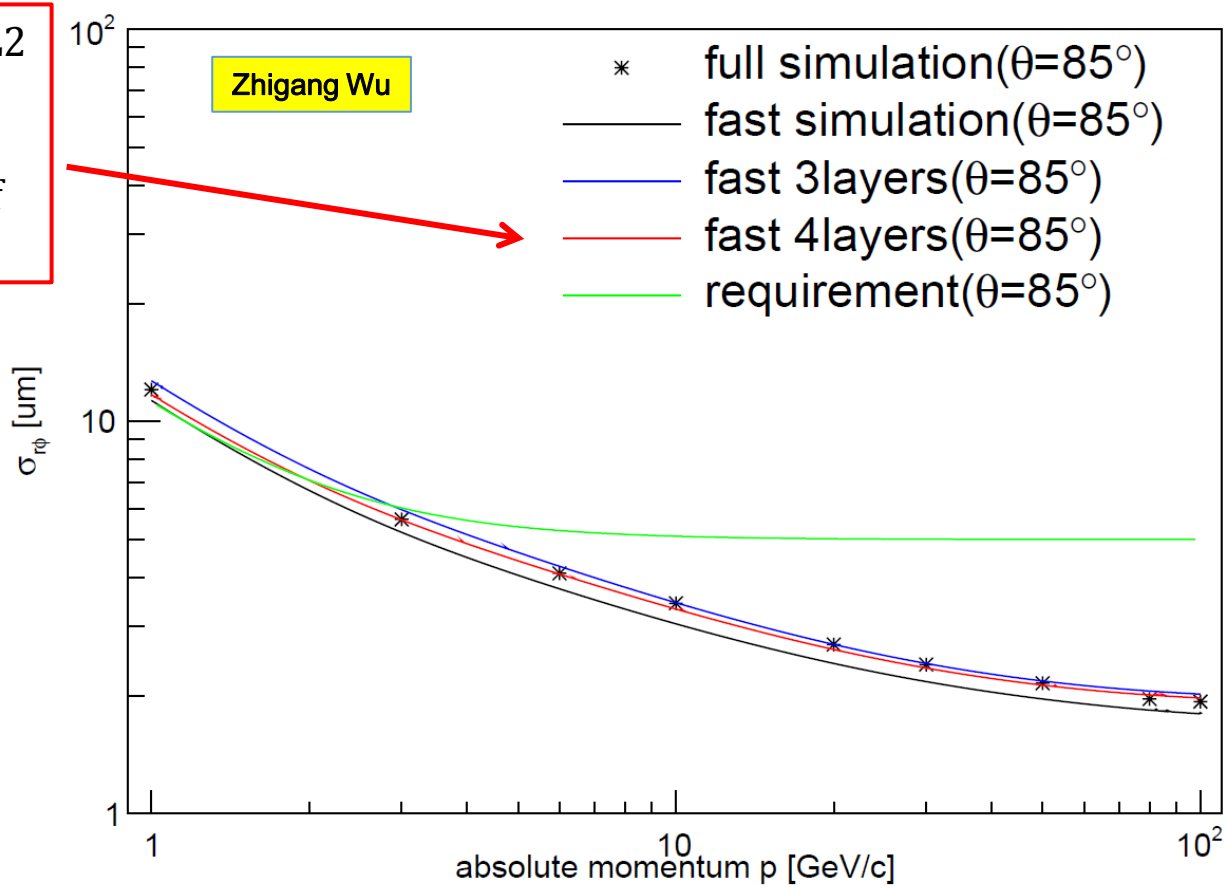
7

Z. Wu, et al., Study of vertex optimization at the CEPC, 2018 JINST 13 T09002

Same layout as in CDR

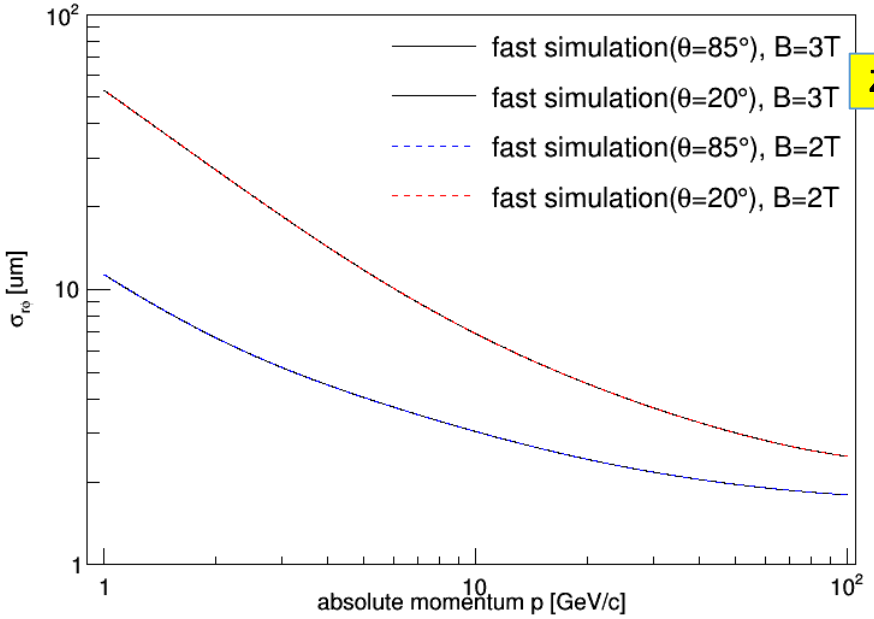
Q Ouyang, CEPC CDR review, Sept.2018

- σ_{sp}=4μm for L1 and L2
- σ_{sp}=3μm for combination of L3 and L4, and combination of L5 and L6

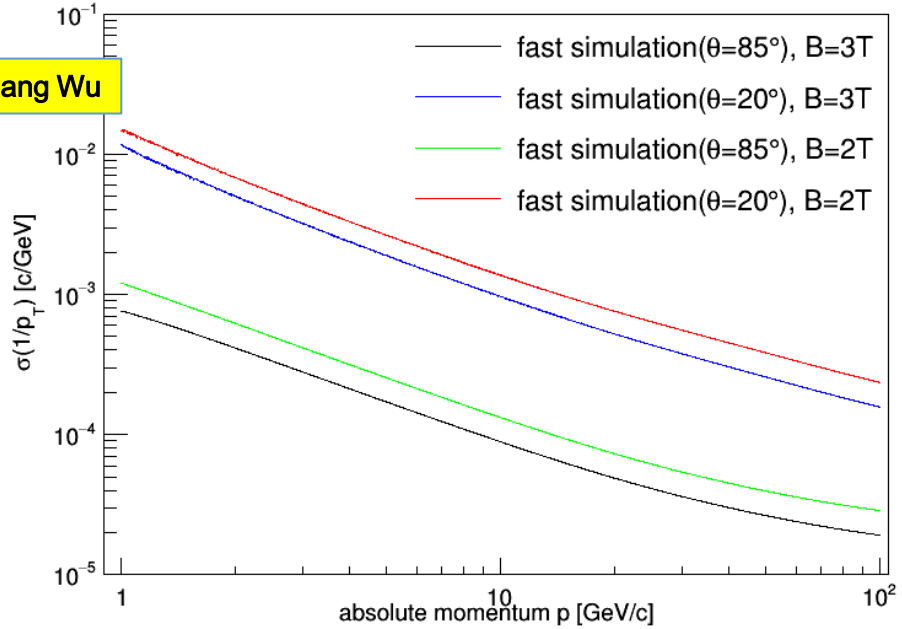


Impact of magnetic field

B=3T → 2T



Zhigang Wu



$\sigma_{r\varphi}$: almost the same

$\sigma(1/p_T)$: worsening ~50%