



Status of the TaichuPix chip for the high-rate CEPC Vertex Detector

Wei Wei

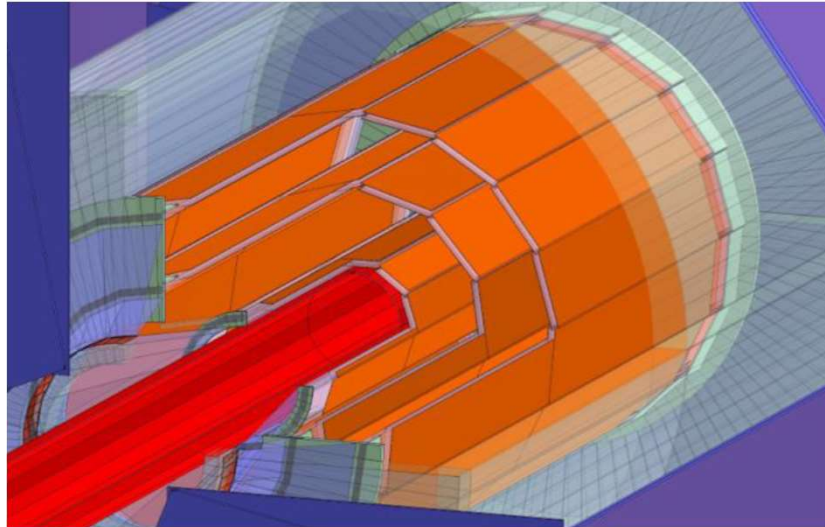
**On behalf of the CEPC MOST2 Vertex detector
design team**

2020-05-27

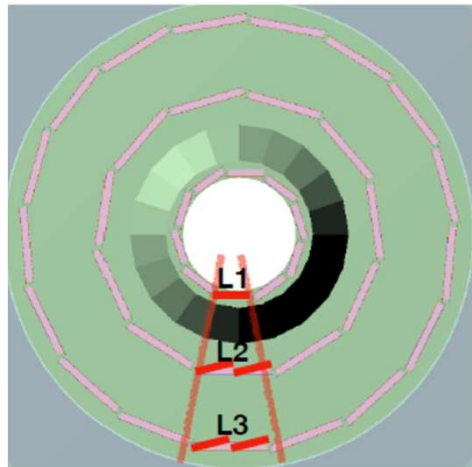
Outline

- **Status of the TaichuPix1 test**
- **Status of the TaichuPix2 submission (2nd MPW)**
- **Recent design status and plan**

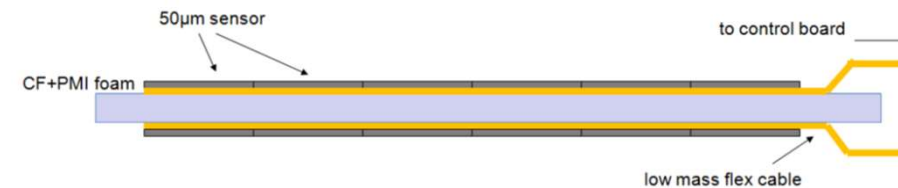
CEPC Vertex Detector Concept



3-layers of double-sided pixel sensors



	R(mm)	z (mm)	$\sigma(\mu\text{m})$
Ladder1 {	Layer1	16	2.8
	Layer2	18	6
Ladder2 {	Layer3	37	4
	Layer4	39	4
Ladder3 {	Layer5	58	4
	Layer6	60	4



A ladder module conceptual design

ATLAS/CMS upgrade
(15 μm)

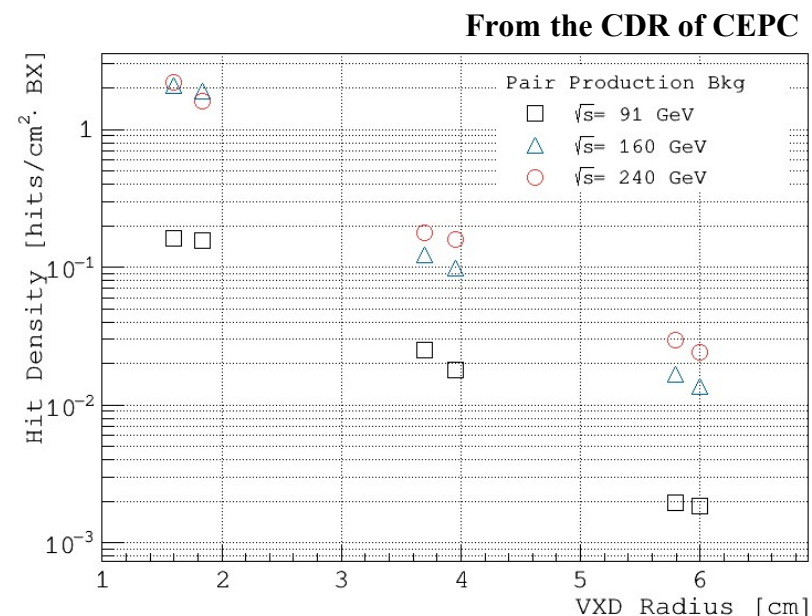
Alice upgrade
(8 ~ 10 μm)

CEPC vertex
(3 ~ 5 μm)



Main specs of the full size chip for high rate vertex detector

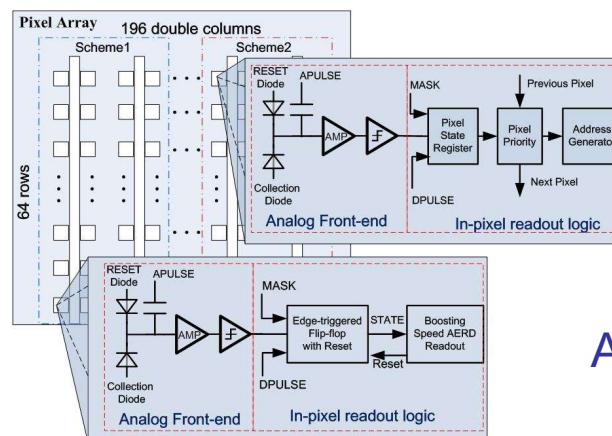
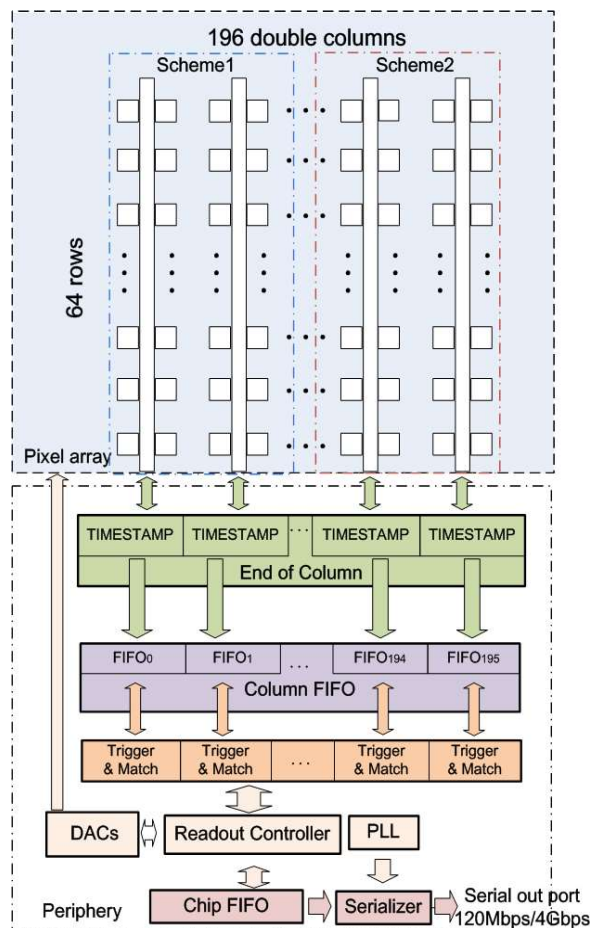
- **Bunch spacing**
 - Higgs: 680ns; W: 210ns; **Z: 25ns**
 - Meaning 40M/s bunches (same as the ATLAS Vertex)
- **Hit density**
 - 2.5hits/bunch/cm² for Higgs/W;
0.2hits/bunch/cm² for Z
- **Cluster size: 3pixels/hit**
 - Epi- layer thickness: ~18μm
 - Pixel size: 25μm × 25μm



For Vertex	Specs	For High rate Vertex	Specs	For Ladder Prototype	Specs
Pixel pitch	<25μm	Hit rate	120MHz/chip	Pixel array	512row × 1024col
TID	>1Mrad	Date rate	3.84Gbps --triggerless ~110Mbps --trigger	Power Density	< 200mW/cm ² (air cooling)
		Dead time	<500ns --for 98% efficiency	Chip size	~1.4cm × 2.56cm

New proposed architecture by TaichuPix1

From Tianya Wu in User Manual

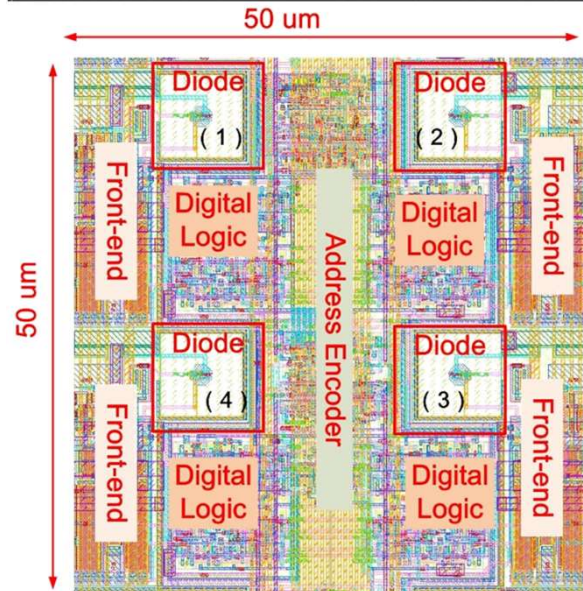
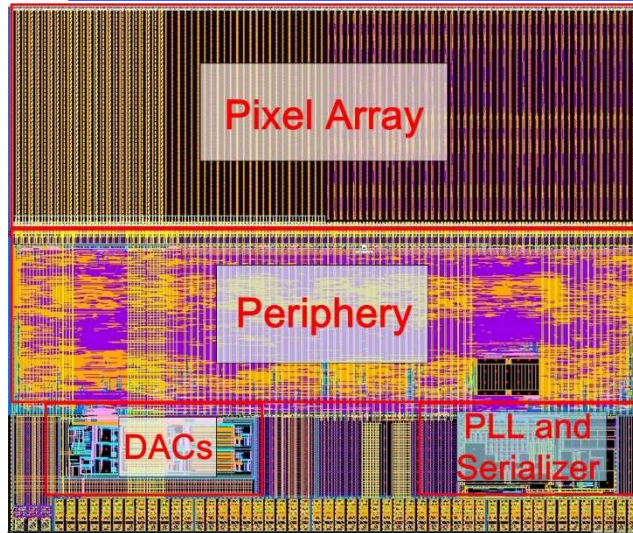


FE-I3-like Pixel

ALPIDE-like Pixel

- **Similar to the ATLAS ITK readout architecture: “column-drain” readout**
 - Priority based data driven readout
 - **Modification:** time stamp is added at EOC whenever a new fast-or busy signal is received
 - Dead time: 2 clk for each pixel (50ns @40MHz clk), negligible compared to the average hit rate
- **2-level FIFO architecture**
 - L1 FIFO: In column level, to de-randomize the injecting charge
 - L2 FIFO: Chip level, to match the in/out data rate between the core and interface
- **Trigger readout**
 - Make the data rate in a reasonable range
 - Data coincidence by time stamp, only matched event will be readout

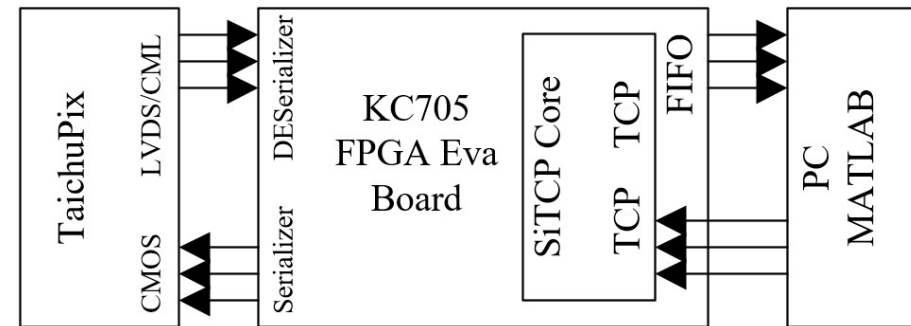
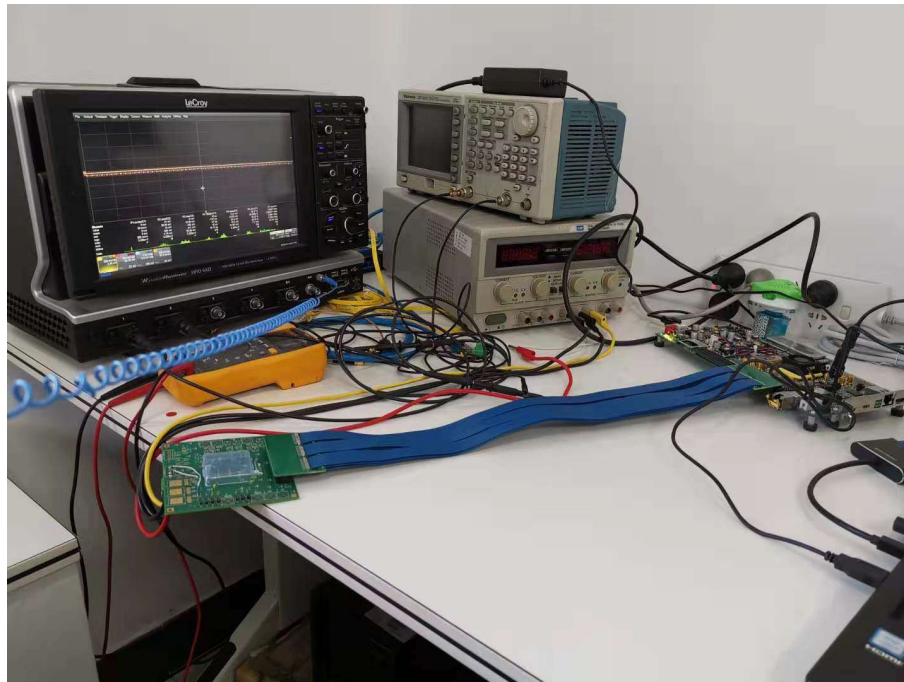
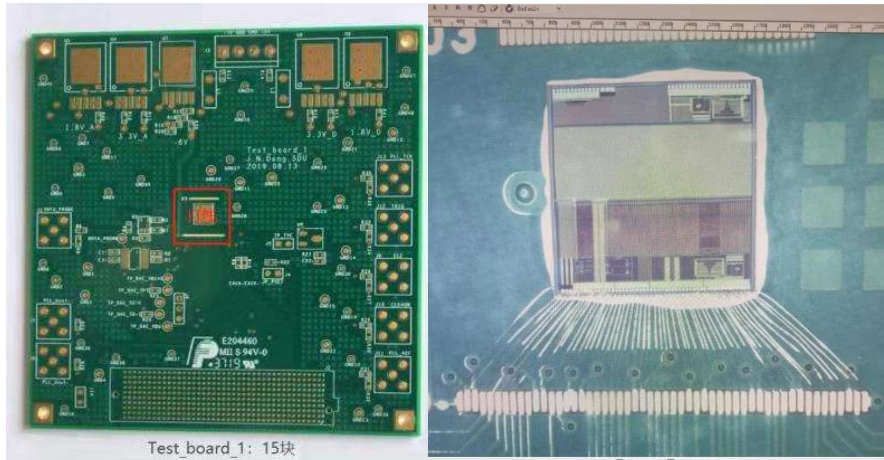
Chip Status of TaichuPix1



Chip size: $5\text{mm} \times 5\text{mm}$
Pixel size: $25\mu\text{m} \times 25\mu\text{m}$

- First MPW tapeout was submitted in June, 2019
 - Thanks IFAE for their tunnel for submission to TJ
- Chip received in Nov. 2019
 - With 60 chips, 40 chips delivered to China
- One block area of $5\text{mm} \times 5\text{mm}$ was fully occupied
 - **A full functional pixel array** (small scale)
 - 85% of the block area
 - A 64×192 Pixel array + Periphery + PLL + Serializer
 - Bias generation included
 - I/O arranged in one edge, as the final chip
 - other independent test blocks (less critical)
 - LDO + PLL
- We got the news that it is possible to use the modified TJ process

Test setup for chip evaluation

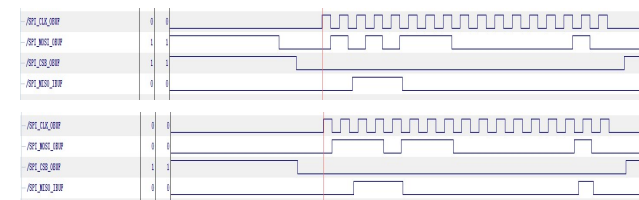
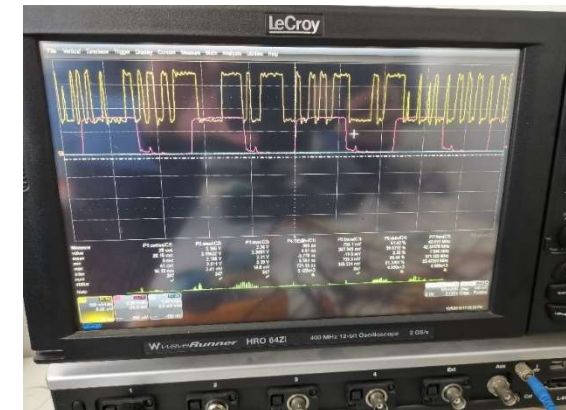


- **Test setup based on KC705 Xilinx FPGA Eva board**
- **General data stream**
 - Downstream from PC to chip: TCPIP@MATLAB → SPI package@FPGA → TaichuPix Periphery
 - Upstream from chip to PC: TaichuPix Serializer → FIFO@FPGA → TCPIP@MATLAB
- **Test Firmware developed in IHEP (China side) by Jun HU and Wei WEI**
 - Released version delivered to different collaborators, and functional worked

Test Status of TaichuPix1



- Initiated in November, in parallel with Tcpix2 design
- Due to the limited time and some detected bugs, most tests were functional test before Tcpix2's submission
- Blocks test
 - IO ring: **bugs found and located**
 - Weak short between VDD & VSS detected – due to the DNW soft conn
 - Test can still proceed with forcibly power supply
 - -6V power supply was found vulnerable to ESD
 - PLL: **Fully functional proved**
 - Lock frequency & lock range proved ✓
 - Typical freq@40MHz, 2.24GHz for Triggerless ✓
 - Serializer PRBS test functional proved ✓
 - LVDS@160MHz proved, Triggerless not testable
 - Periphery: (Almost) **Fully functional proved**
 - SPI configuration proved ✓
 - Communication with Serializer proved ✓
 - LDO:
 - Function good but with large output DC shift



Test Status of TaichuPix1

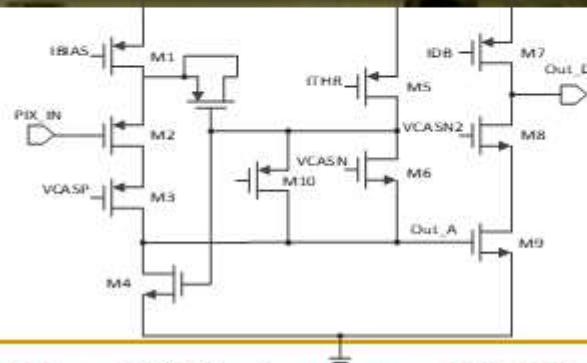
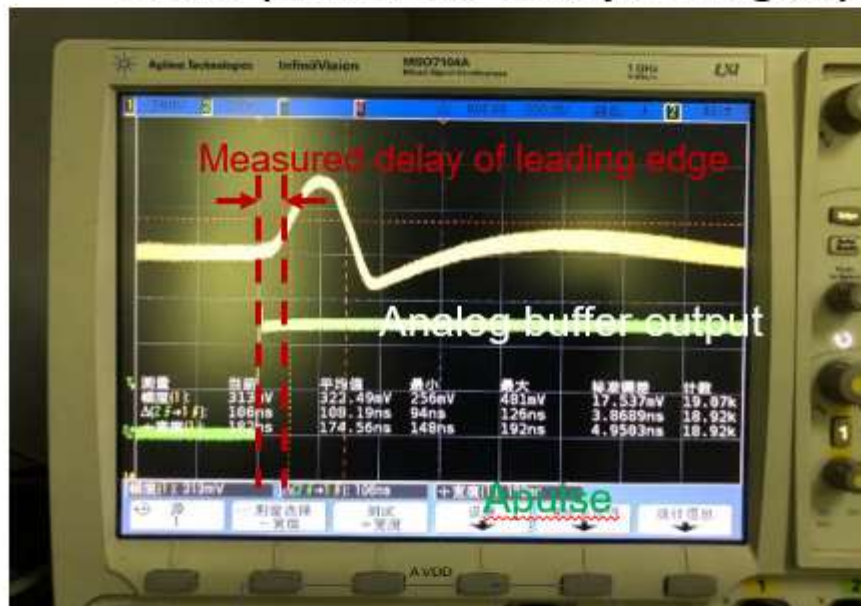


- **Blocks test**
 - **Bias generation: bugs found and located**
 - Output reference oscillates occasionally - lack of phase margin
 - Reference DC value with large shift – still not fully understood
 - Bypassed in the full test
 - **Pixel Analog - Fully functional proved**
 - Tested by a probing pixel with buffer
 - Response to the calibration pulse, and light
 - Pulse shape close to the saturation condition
 - Generally responses following the S-curve behavior
 - Bias needs careful tune due to the DAC shift
 - **Pixel Digital – problem found and almost located**
 - The ALPIDE-like columns (with the highest priority) cannot be reset, and will block other columns
 - Problem was because of the power supply issues of the pixel layout (needs further simulation)

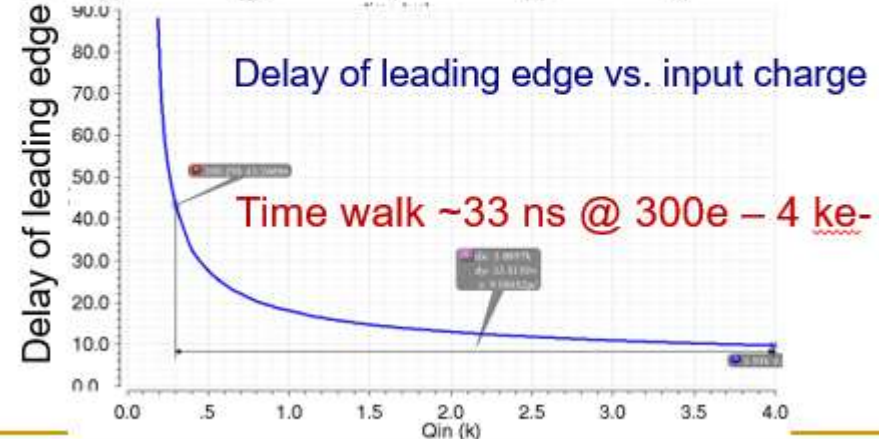
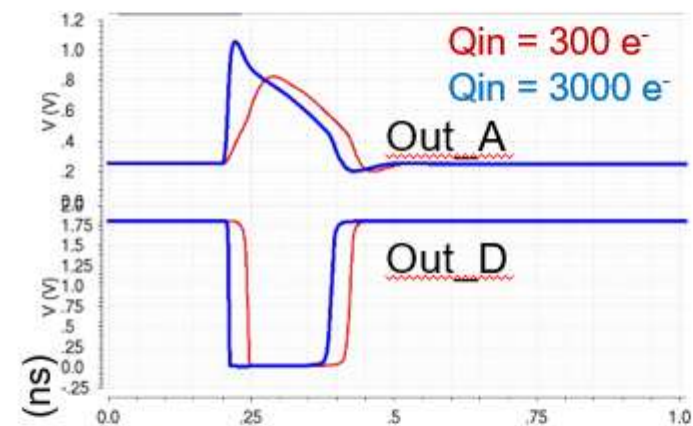


Timing performance

- Measured delay of leading edge → Time difference from 50% of leading edge of OUT_A to 50% of APULSE
- Simulated delay of leading edge → Time difference from 50% of leading edge of OUTD (connected to in-pixel digital) to 50% of PIX_IN

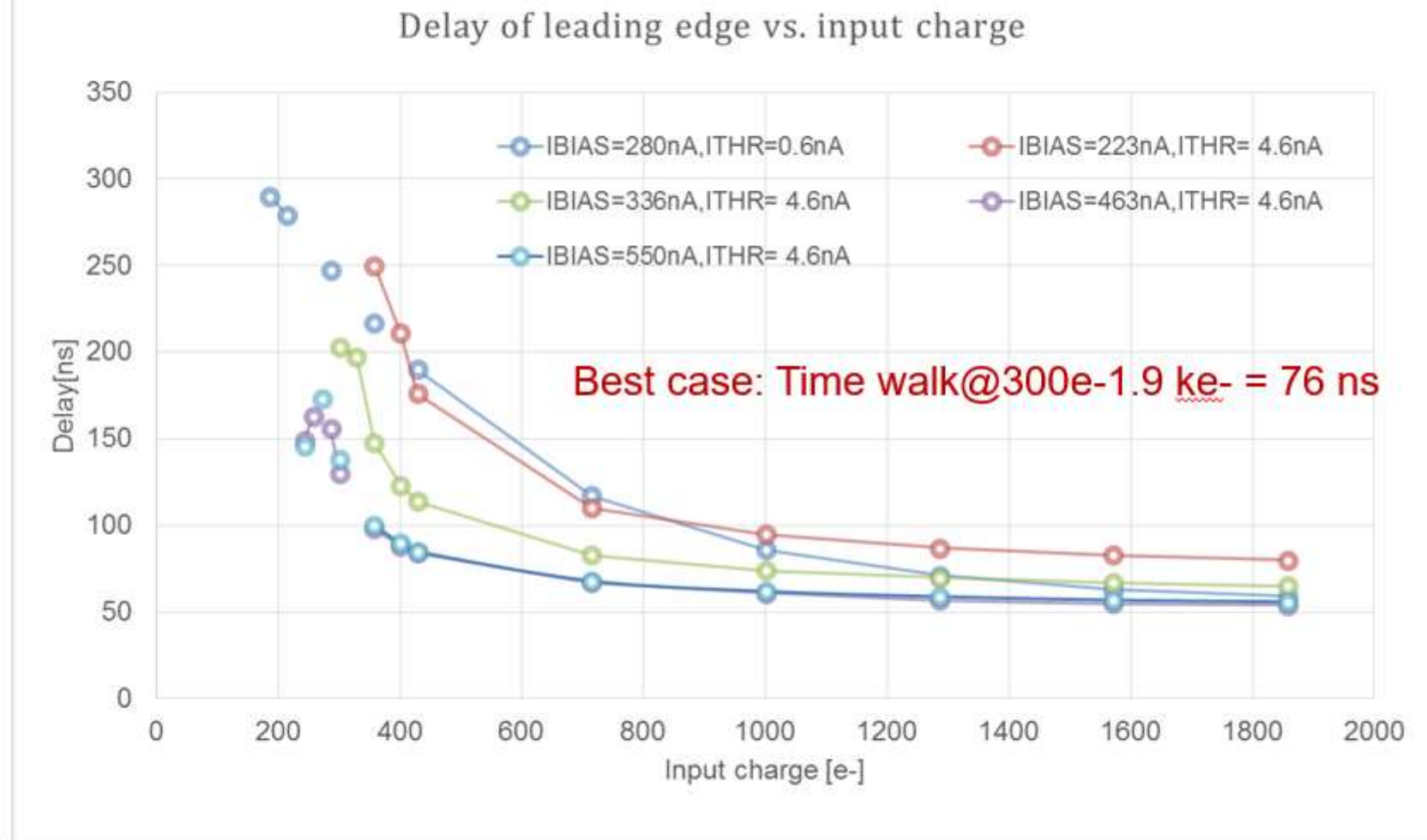


Simulated delay of leading edge



Timing performance

- VPWELL= 0 V, pulsing with VHIGH = 1.8 V, varying VLOW



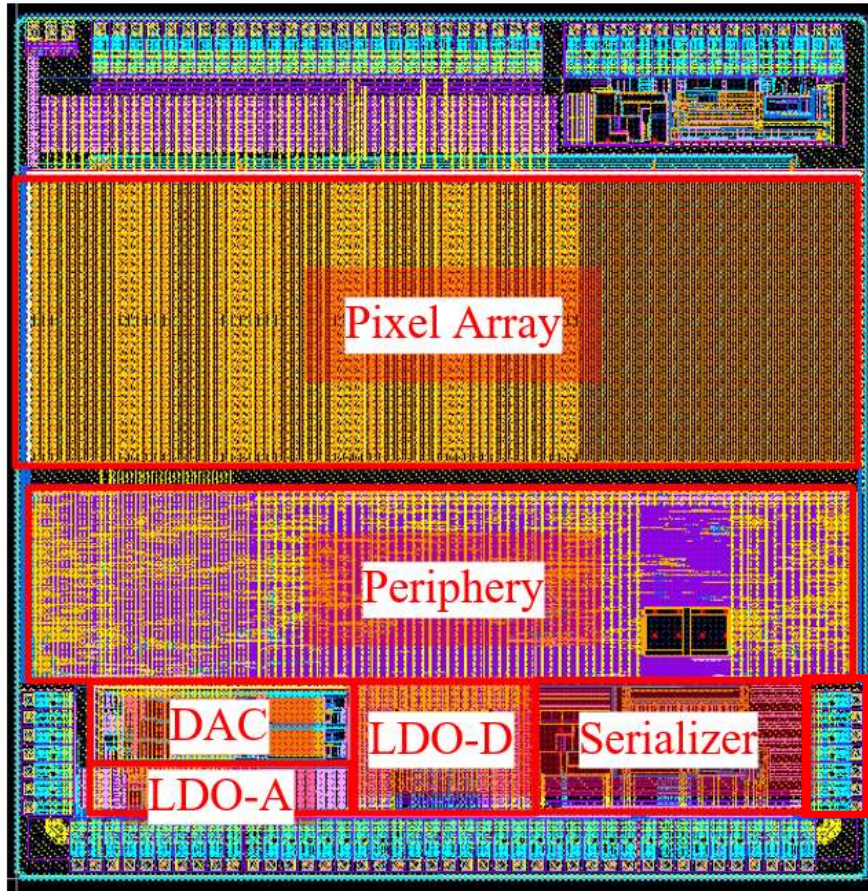
*IBIAS= 280 nA case measured with chip#4, the others measured with chip #5

Summary of the Preliminary performance test of Pixel Analog



- **Pixel Analog Functionally work**
- **Time walk performance was thoroughly tested**
 - Behavior similar to the simulation, however twice slower than simulation at the same biasing (power)
 - Maybe because of the incorrect bias generation of DAC, still needs to further understand
 - Not a serious problem though
- **Noise performance was roughly tested by S-curve method (in an analog way)**
 - 5e- of ENC was tested, by using the design value of injection capacitor, not energy calibrated
 - However, very rough result, the voltage tuning precision was very very poor

Design Status of TaichuPix2



- Submitted on Feb 18, 5*5mm
- All blocks fully integrated, as the final chip
- New features
 - A 64*192 pixel array with the same dimension as Tcpx1
 - 32 + 32 double column modified FE-I3 readout, 32 dblcol modified ALPIDE readout
 - 6 variations of pixel analog, each for 16 columns
 - Newly integrated blocks: Two LDOs for power supplies
 - 8b10b encoder added for Triggerless output and balanced datastream
 - X-chip buses added for multiple chip interconnections

Design Status of TaichuPix2



- **Major bugs (were tried to be) fixed**
 - New IO rings were used, without DNW soft connect issues
 - DAC stability improved with higher phase margin
- **Pixel readout optimized**
 - To make larger headroom for the timing
 - Data latching @ 1clk -> 1.5clk
 - Address encoder pull-up added to avoid high-Z state
- **Pixel analog new attempts**
 - Smaller pixel area
 - Possible to be 24um*25um
 - One branch with enclosed gate for better TID
- **X-chip interconnections attempts**
 - SPI buses, PLL clock reference, reset signal, are possible to be propagated by chip-chip wire bonding
 - Save some routing space for the flex cable design

Summary and Recent Schedule



- **Test of the Tcpx1 chip will continue, and to locate all the bugs**
 - **Test firmware were delivered to different sites, and parallel tests had been initiated**
 - **First crosscheck test agreed with those in IHEP**
 - **Performance test for the functional blocks**
 - **Pixel analog almost complete**
 - **Try to see if TID test is possible with Tcpx1**
- **The test setup design will be initiated for the Tcpx2 chip, based on previous setup**
 - **Tcpx2 is expected to be received in about Aug. ~ Oct.**
 - **Test board design for Tcpx2 is on-going**
- **Thinking about the following Tcpx3 MPW...**
 - **It is better to collect all the test results and bugs of Tcpx1 &2 before Tcpx3 submission**
 - **Expected to tapeout in the Spring of 2021**

Thank you !

Challenges and R&D activities on pixel sensors

- **Bunch spacing**
 - Higgs: 680ns; W: 210ns; **Z: 25ns**
 - Meaning 40M/s bunches (same as the ATLAS Vertex)
- **Hit density**
 - 2.5hits/bunch/cm² for Higgs/W;
0.2hits/bunch/cm² for Z
- **Cluster size: 3pixels/hit**
 - Epi- layer thickness: ~18μm
 - Pixel size: 25μm × 25μm
- **Hit rate: 120MHz/chip @W**
- **Two major constraints for the CMOS sensor**
 - Pixel size: < 25μm* 25μm (σ~5μm)
 - aiming for 16μm*16μm (σ~3μm)
 - Readout speed: bunch crossing @ 40MHz
- **None of the existing CMOS sensors can fully satisfy the requirement of high-rate CEPC Vertex Detector**
- **TID is also a constraint, 1~2.5Mrad/year is achievable**

	ALPIDE	ATLAS-MAPS (MONOPIX / MALTA)	MIMOSA
Pixel size	✓	X	✓
Readout Speed	X	✓	X
TID	X (?)	✓	✓

Team organization



- Slides from Y. Zhang, Satellite meeting of MOST2 in Oxford, 2019.4

- **Design team:**

- IHEP, SDU, NWPU, IFAE & CCNU
- Biweekly/weekly video design meeting on chip design (convened by IHEP)

Institutes	Tasks	Designers
IHEP	Full chip modeling & simulation Pixel Analog, TCAD simulation High speed interface: PLL + Serializer	Wei Wei, Ying Zhang Xiaoting Li, Weiguo Lu, Mei Zhao
CCNU/IFAE	Pixel Digital	Tianya Wu, Raimon Casanova
NWPU	Periphery Logic, LDO	Xiaomin Wei, Jia Wang
SDU	Bias generation	Liang Zhang

- **Chip characterization**

- Test system development: SDU & + other interested parties
- Electrical test: all designers supposed to be involved in the related module + other interested parties
- Irradiation test: X-ray irradiator + beam line