# Update on TPC R&D at IHEP

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IHEP and Tsinghua

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# Outline

- Status of TPC detector
- Status of ASIC R&D
- Status of the collaboration

✓ All of update progress will be reported: "Development of IBF suppression TPC integrated with low power ASIC and laser beams", ICHEP2020

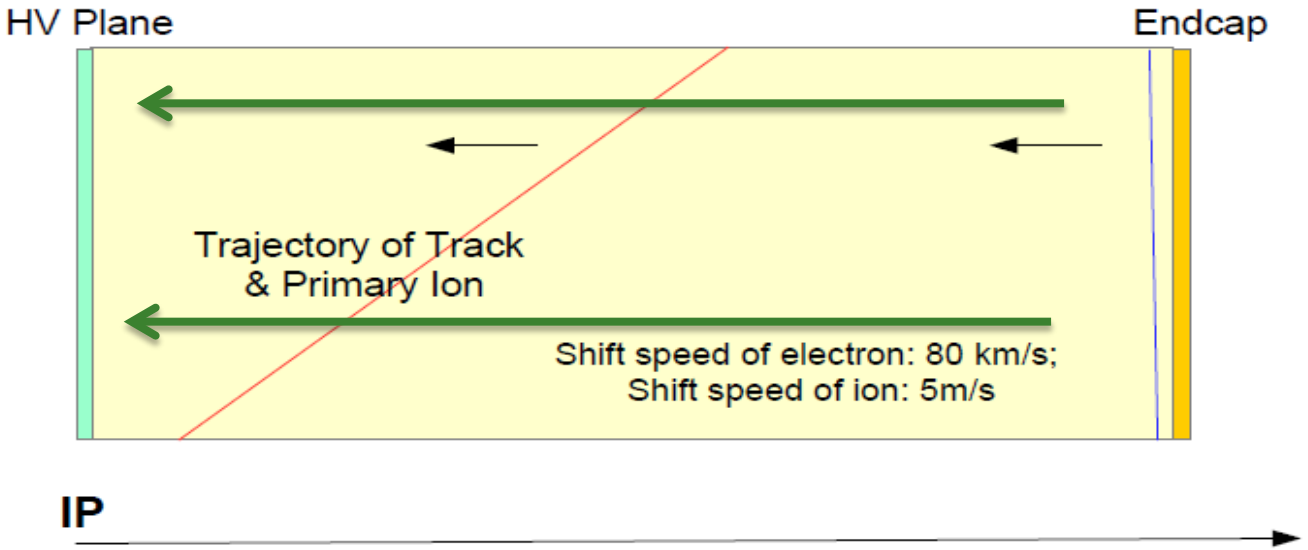
# Introduction

## TPC limitations for Z

- Ions back flow in chamber
- Calibration and alignment
- Low power consumption FEE ASIC chip

MOST1
NSFC
MOST1

| | International collaboration | Leading institutions |
|---|---|---|
| MOST1<br>2016.6-2021.6 | LCTPC, KEK, Saclay | IHEP, Tsinghua |
| NSFC<br>2016.1-2020.12 | LCTPC, KEK, Nikehf | IHEP, Tsinghua |




**Compare with ALICE TPC and CEPC TPC**

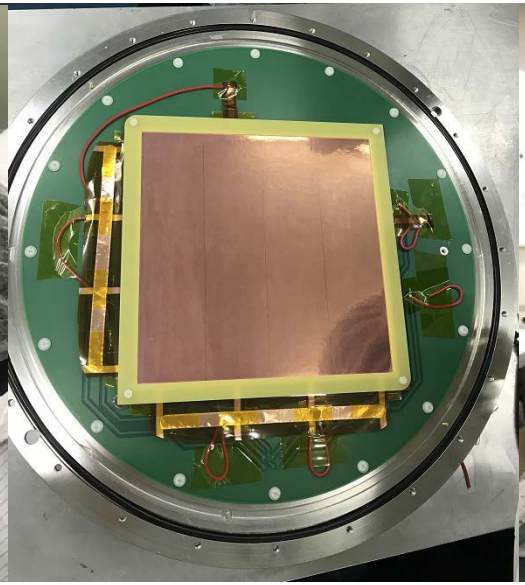
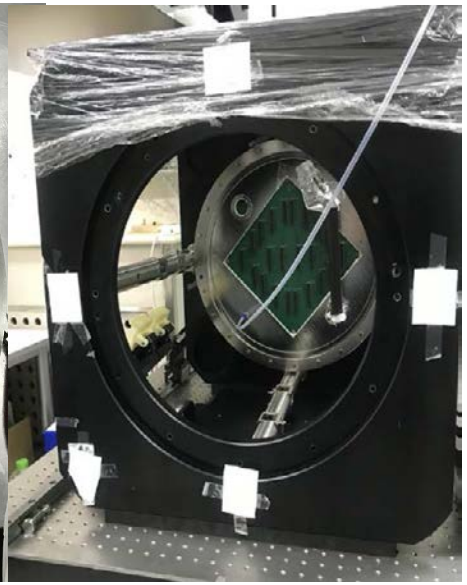
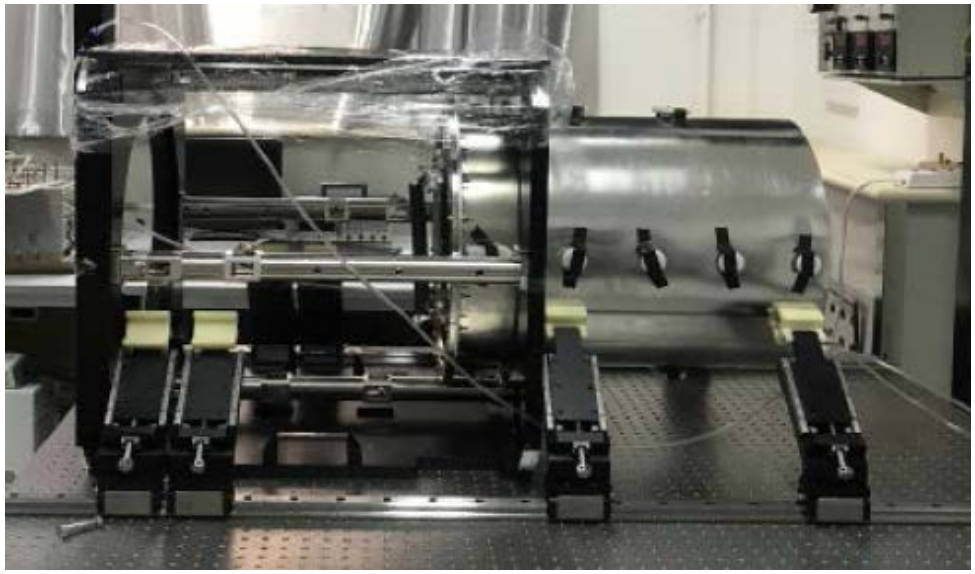
# Preliminary results

- Status of the prototype

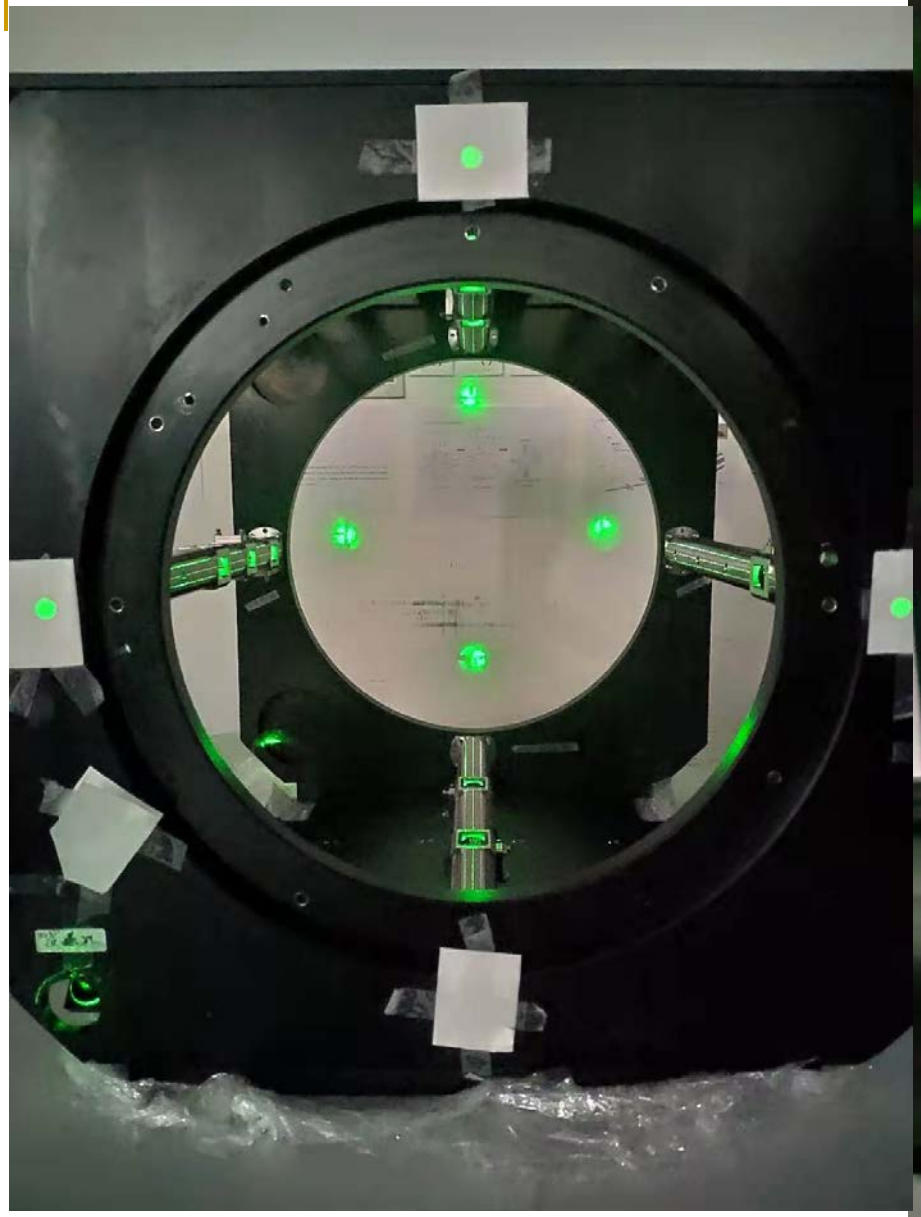
# Re-assembled TPC prototype in last three months

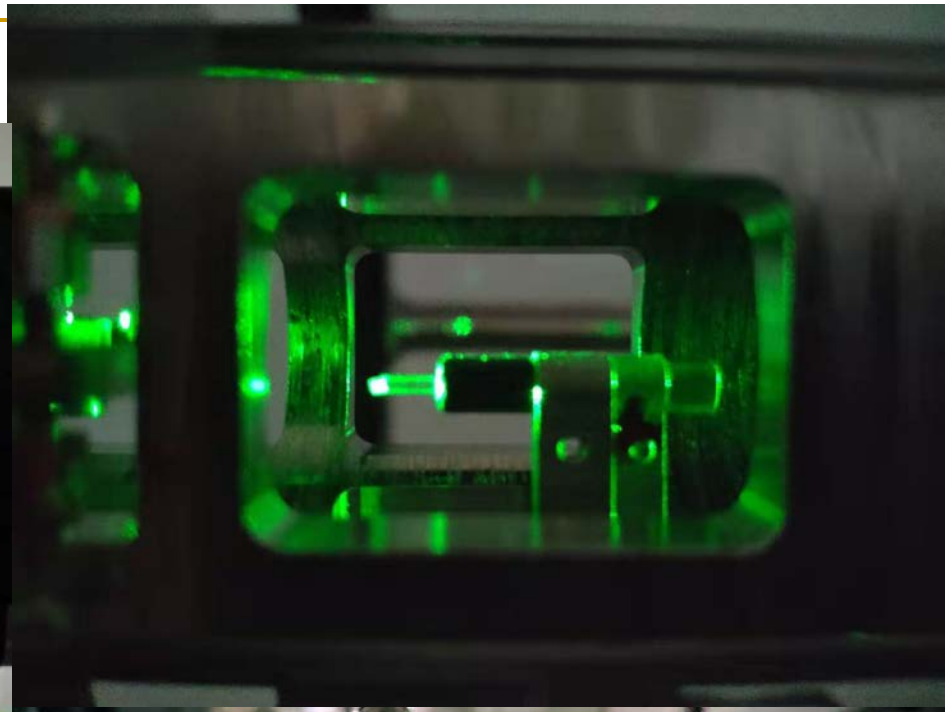
**Optimization of gas leak, O ring seal, detector HV connectors and UV beam devices.**

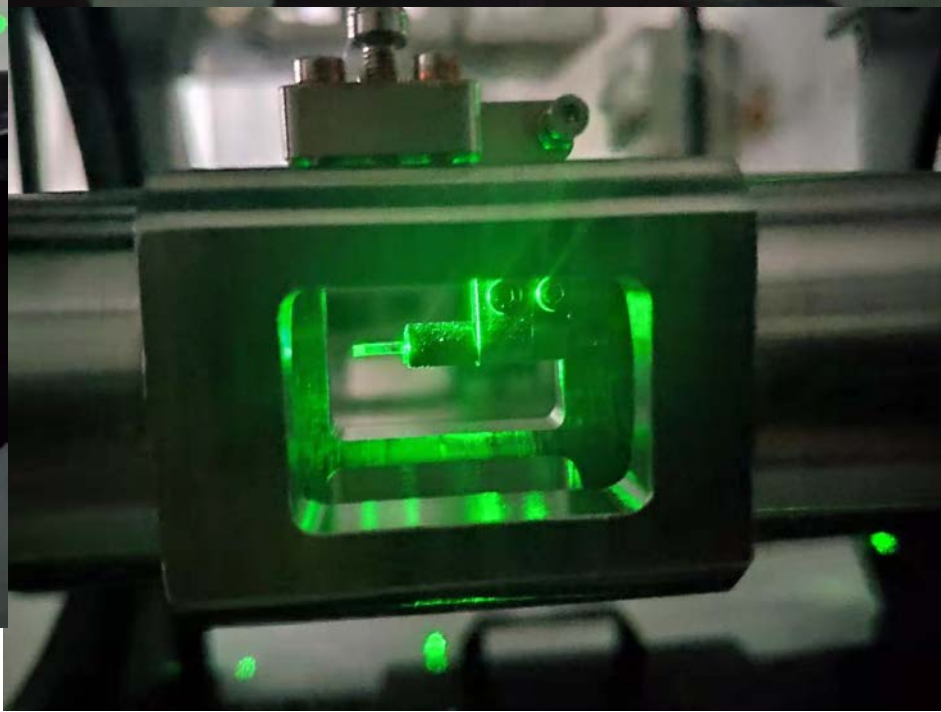


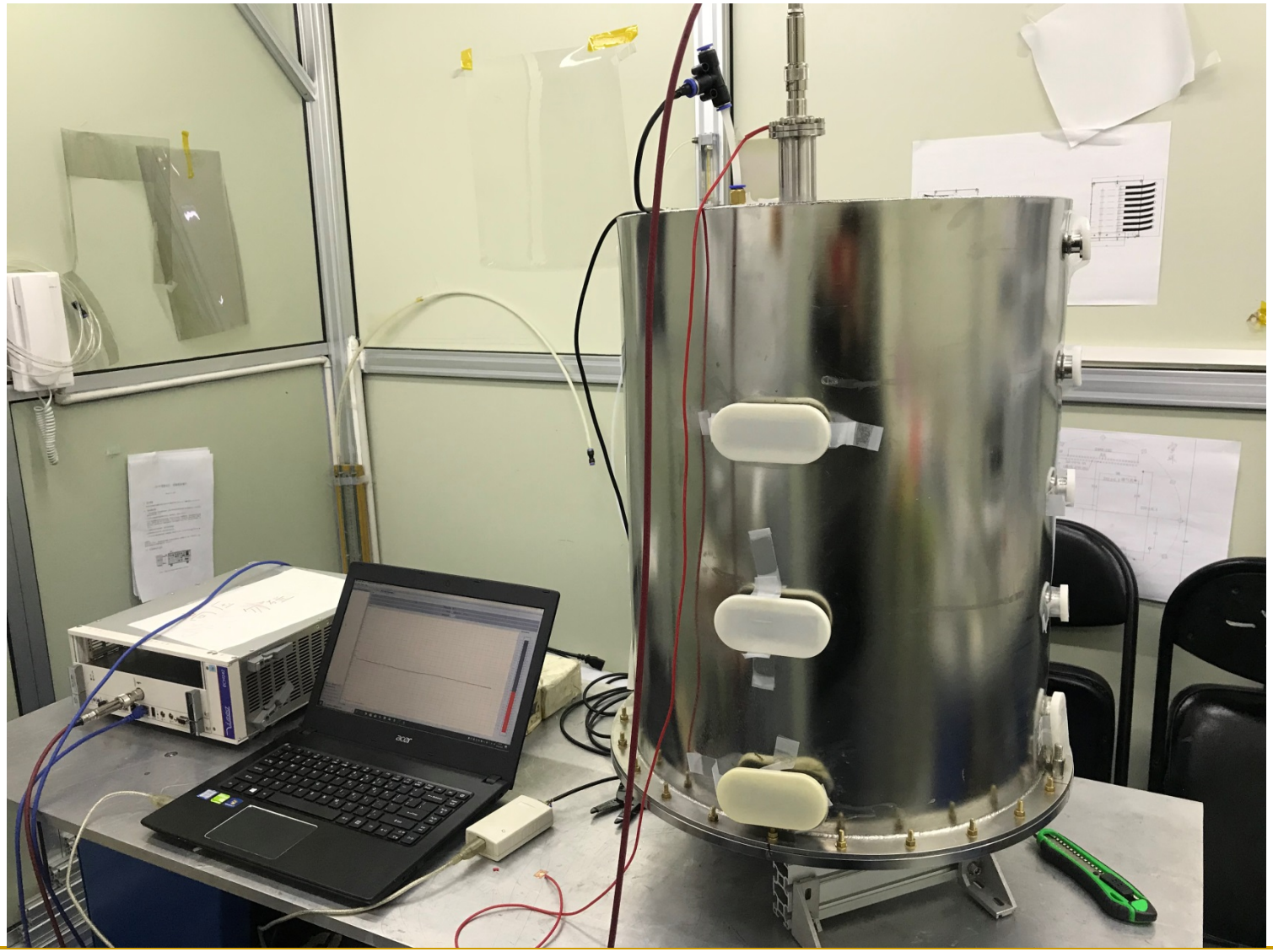
# Photos of the laser prototype



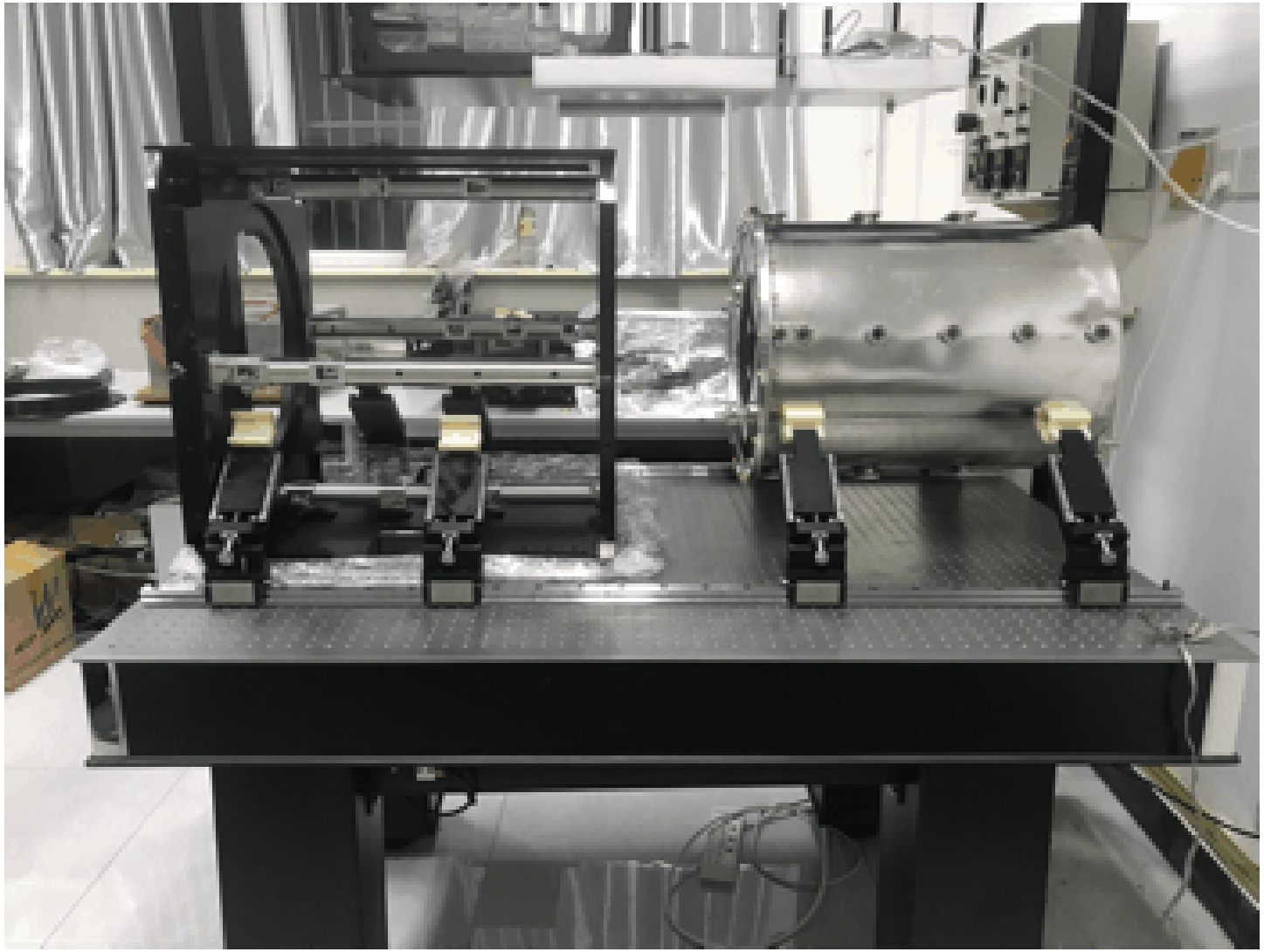




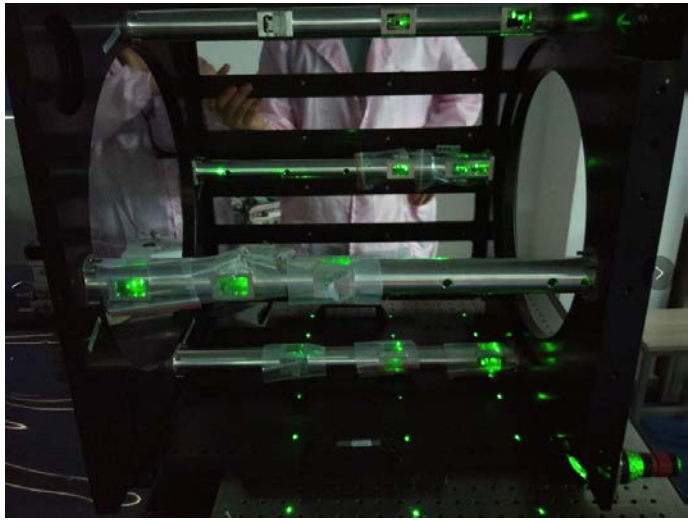
# >15000V high voltage training (Ready)



# Assembled and removed motion

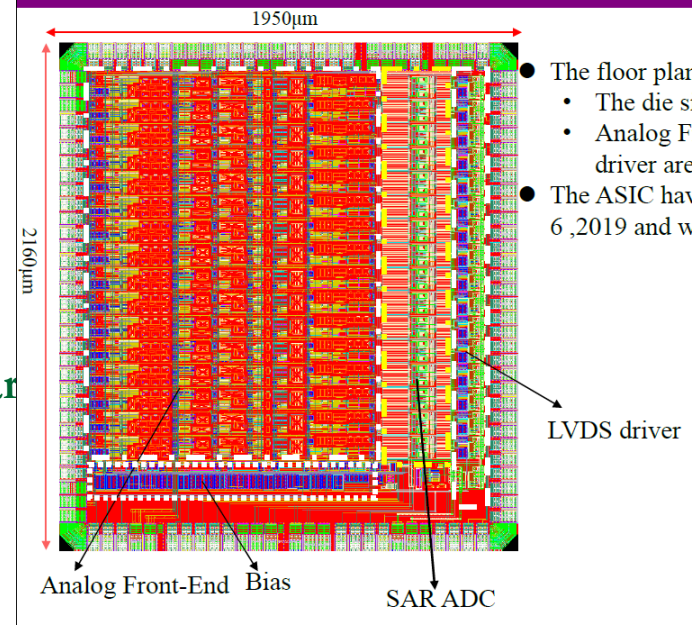


# TPC prototype and FEE R&D



- Main parameters
  - Drift length: ~510mm, Readout active area: 200mm×200mm
  - Integrated the laser calibration with 266nm
  - GEMs/Micromegas as the readout
  - Amplifier (Assembled)
    - CASAGEM chip
    - 16Chs/chip
    - Shape time: 20ns
  - DAQ (Assembled)
    - FPGA+ADC
    - 4 module/mother boar
    - 64Chs/module
    - Sample: 40MHz
    - 1280chs

Layout of 16-ch TPC Readout ASIC

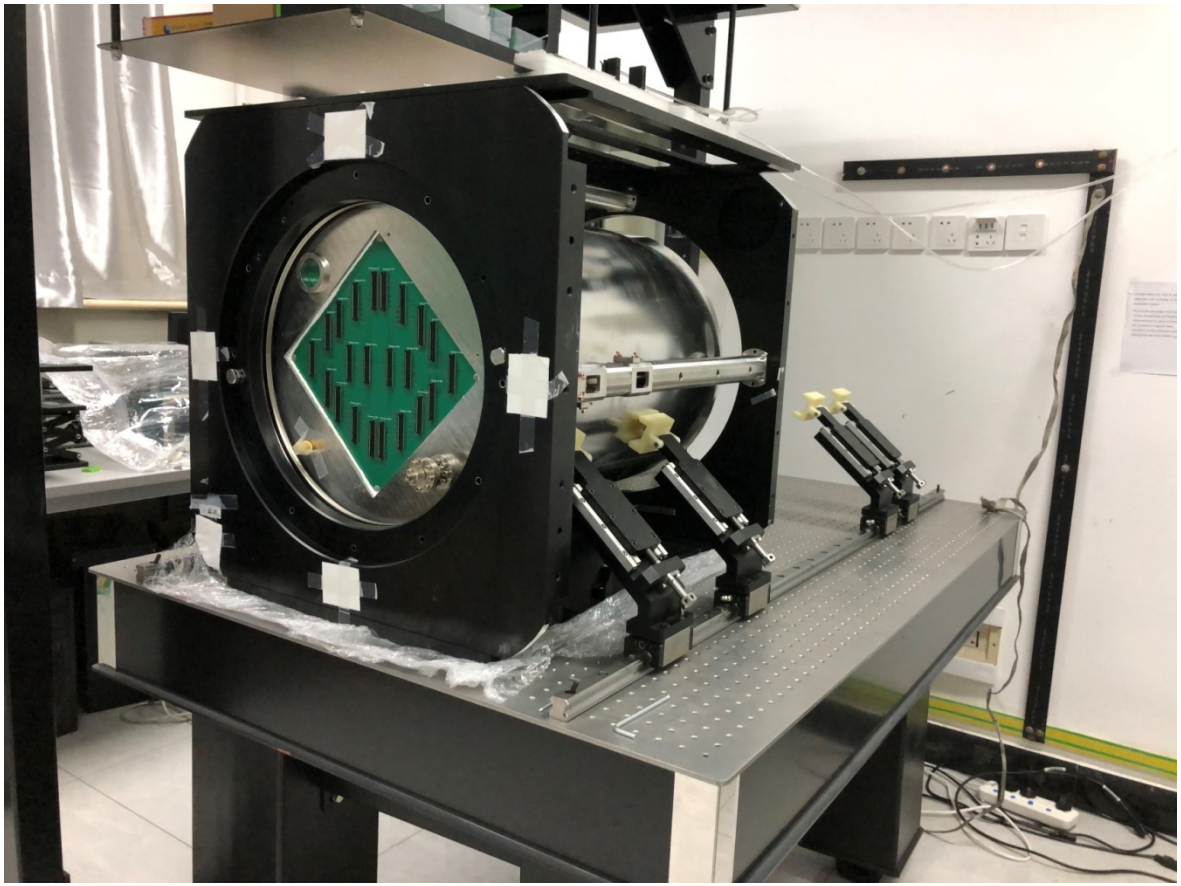



- The floor plan in layout：
  - The die size of 1950 μm x 2160 μm
  - Analog Front-End , SPI, SAR ADC, LVDS driver are supplied by separate power
- The ASIC have been taped out in November 6 ,2019 and will be evaluated in February,2020.

Diagram of the TPC prototype with the laser calibration system

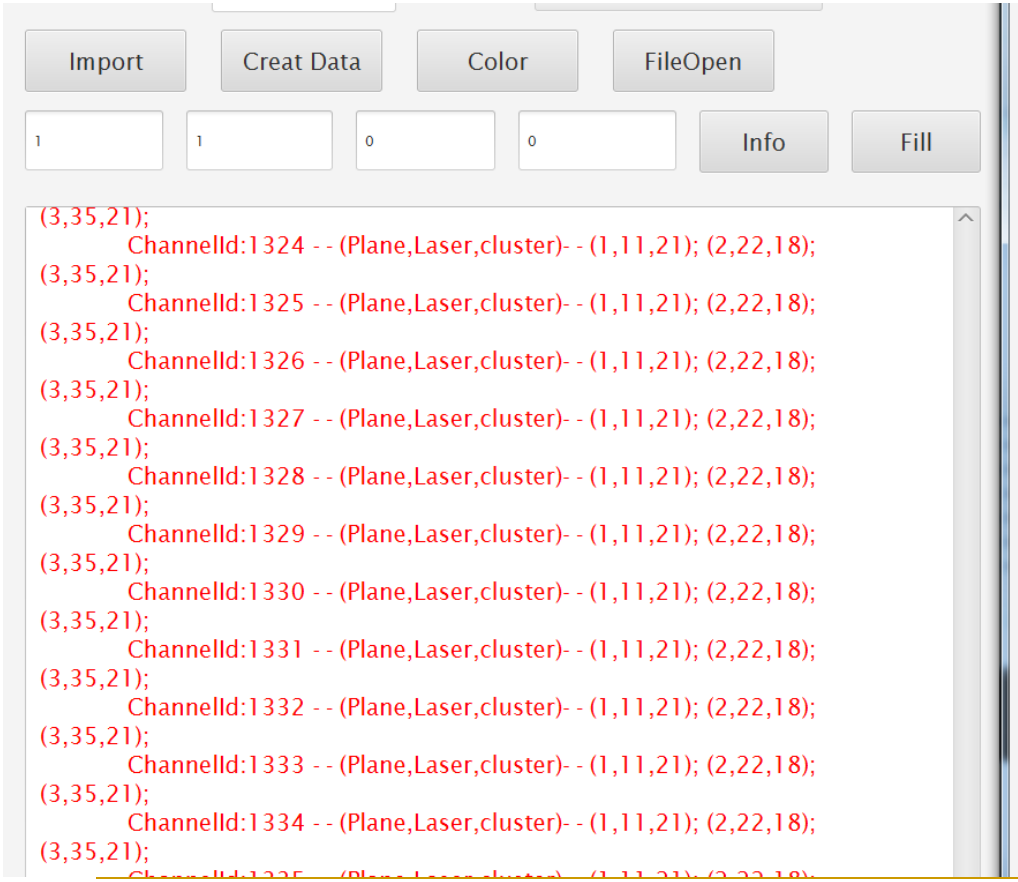
# All prototype in the lab (Ongoing Studies)

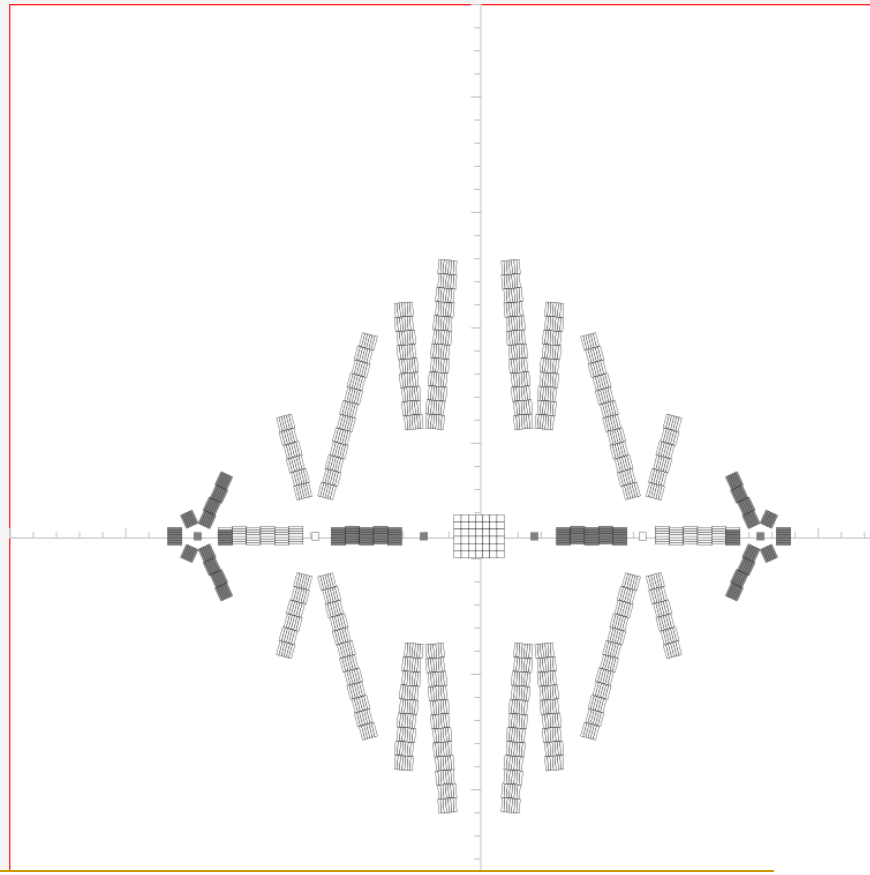
- Manpower
  - In last three months, Jian Zhang and Huirong
  - Our biweekly meeting has been maintained
  - Students will join in this month



# Event display interface @V1.7

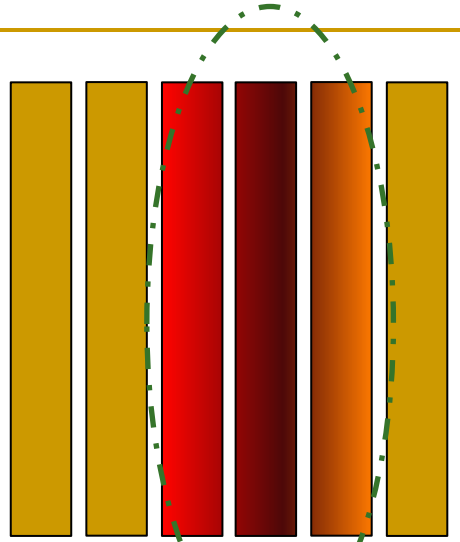
- Event display software
  - Integrated with DAQ software packages
  - Event and some information display interface developed

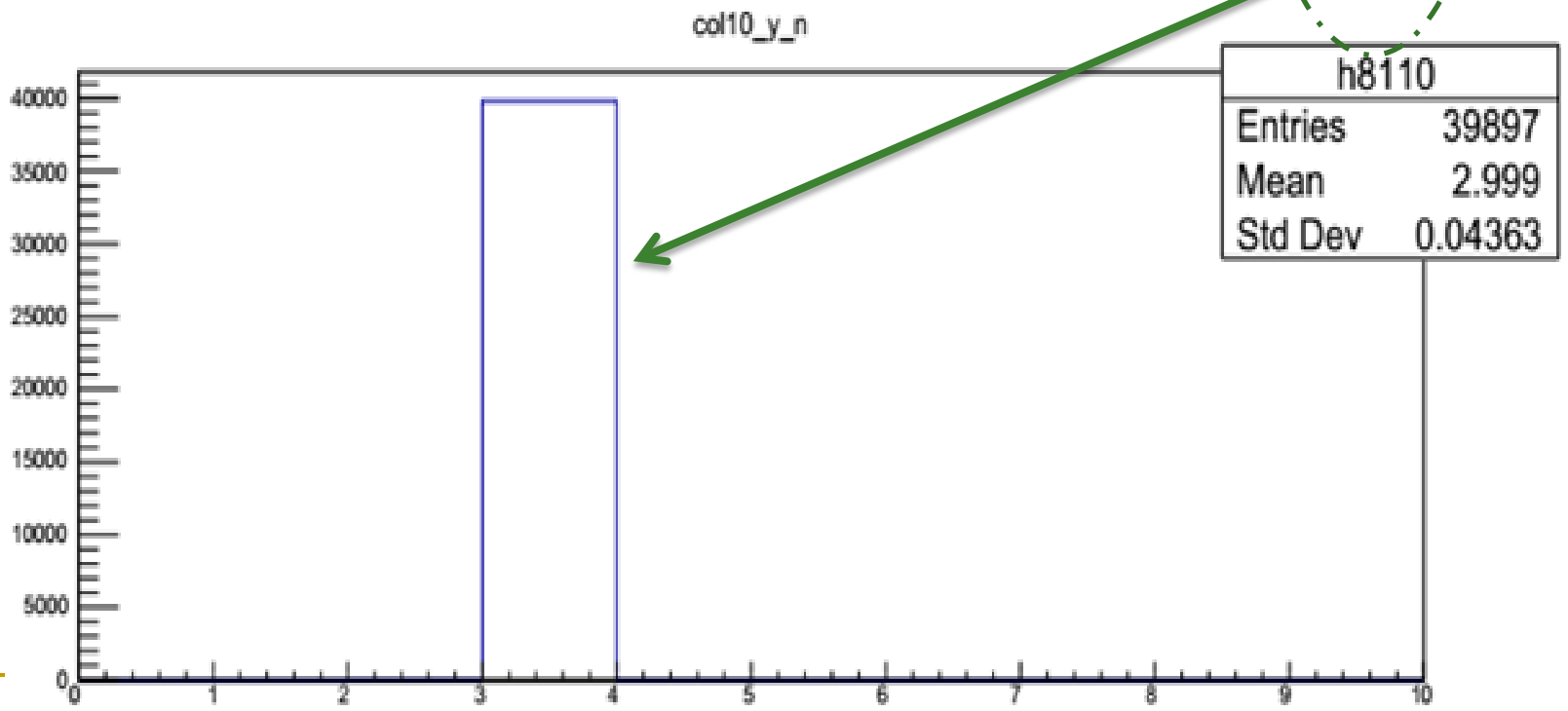


# Resolution

- Laser size: Φ0.75mm
- Gaussian laser profile
- Pad size: 0.95mm× 5.9mm
- Three adjacent pads : >92%





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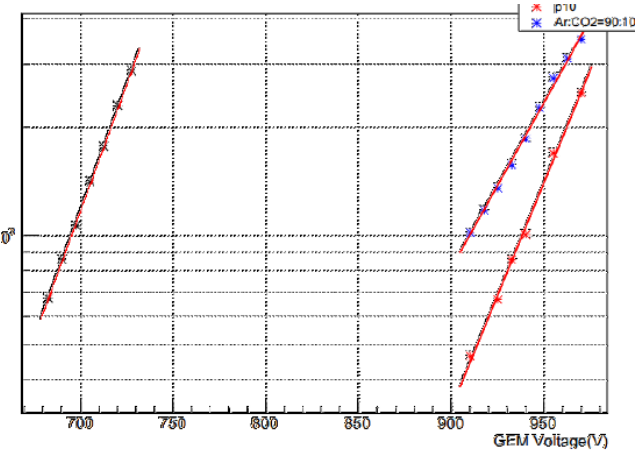
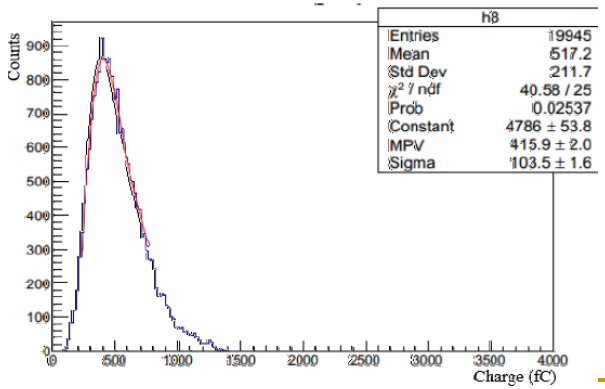
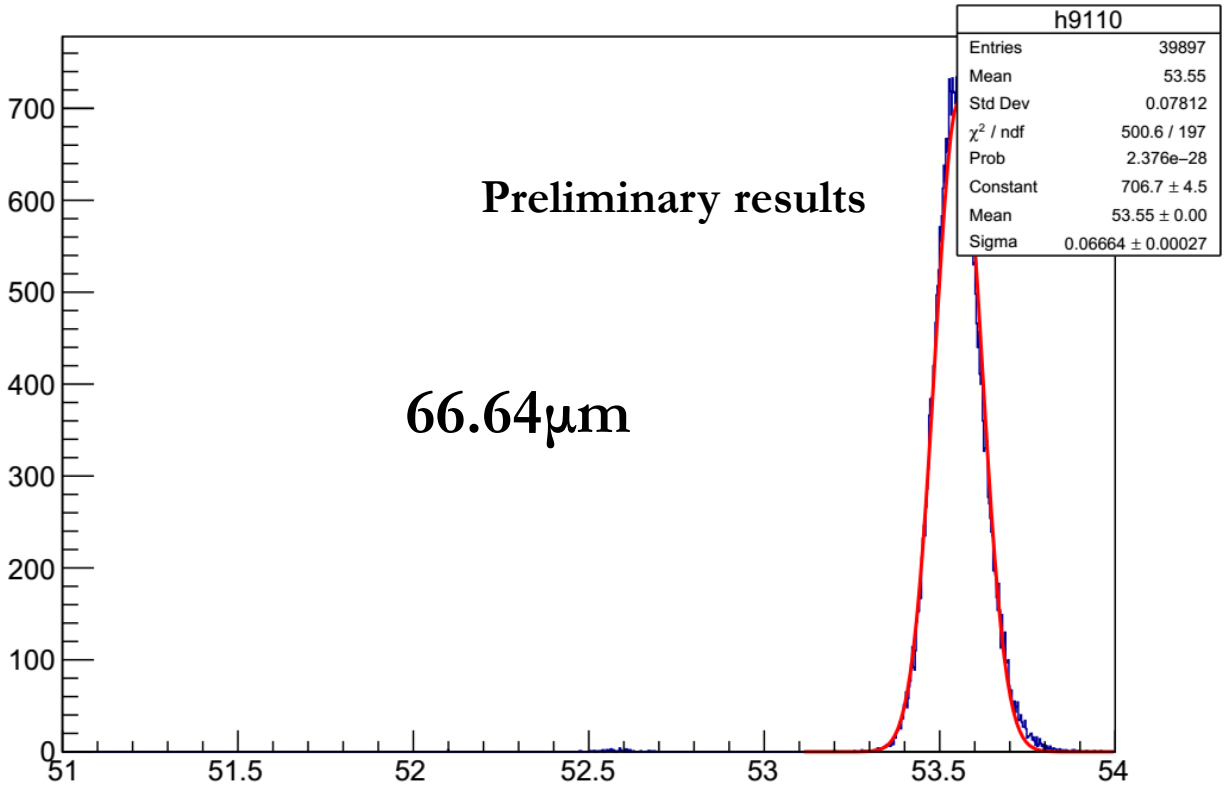


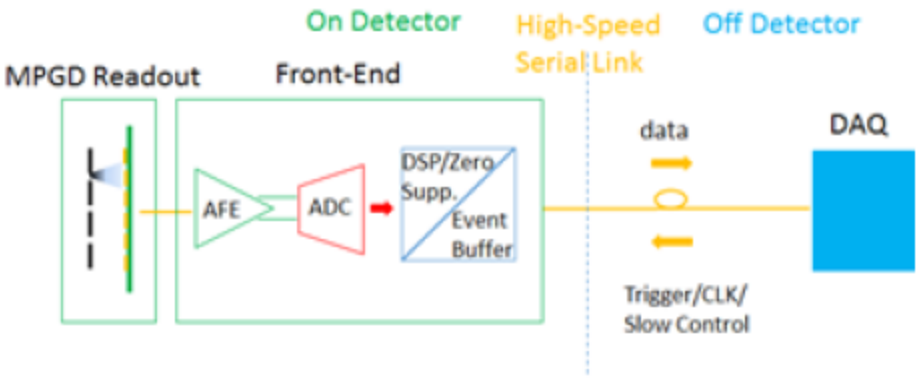




Gain and energy of 266nm laser

- Status of ASIC R&D

# ASIC in 65nm CMOS

## Architecture and Specification




The waveform sampling front end:

- a preamplifier and a shaper as the analog front-end (AFE)
- a waveform sampling ADC
- a dedicated digital signal processing (DSP) and data compression unit for each channel

The Key Specifications of the AFE and the ADC

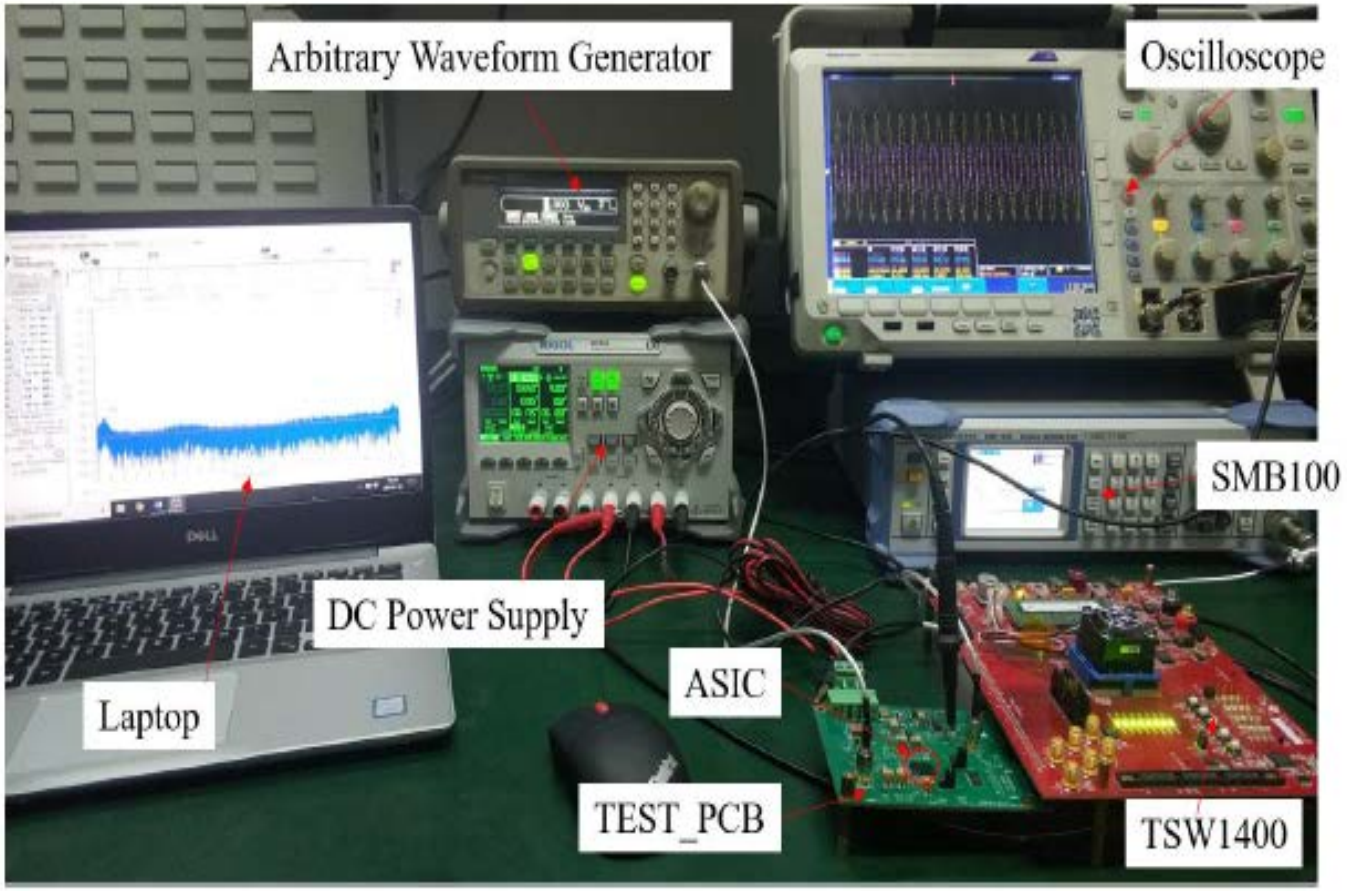
| | | | | |
|---|---|---|---|---|
| **AFE** | ENC | 500 e @ 10pF input cap. | Shaper | CR-RC |
| | Gain | ~10 mV/fC | Shaping time | ~160 ns |
| | Crosstalk | <1% | | |
| **ADC** | Sampling rate | ≥20 MSPS | Resolution | 10 bit |
| Process | | TSM C 65nm LP | Power consumption | ≤5 mW per channel |

# ASIC in 65nm CMOS

- **Current Progress**
  - **First MPW tape out in 2017, including three prototype chips**
    - **5-channels analog front end (preamplifier + CR-RC shaper)**
    - **Single channel SAR-ADC**
    - **Single channel full function ASIC (analog front and SAR-ADC)**
  - **5-channels analog front end, SAR-ADC and full function**
  - **Preliminary testing in Oct.,2019 and re-test in April, 2020**
  - **Second MPW tape out in Nov. 2019**
  - **Second MPW will be tested in Tsinghua University**
  - **Second MPW will used for TPC prototype's testing**

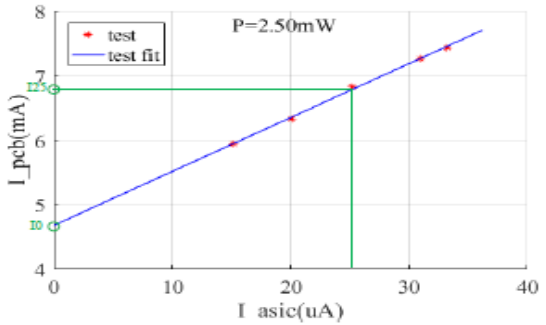
# First MPW ASIC tests

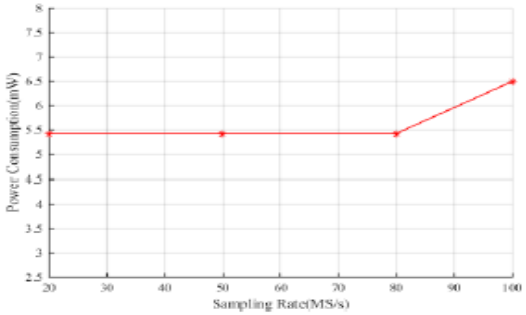
## Test Systems



# Results of power consumption and lineartity

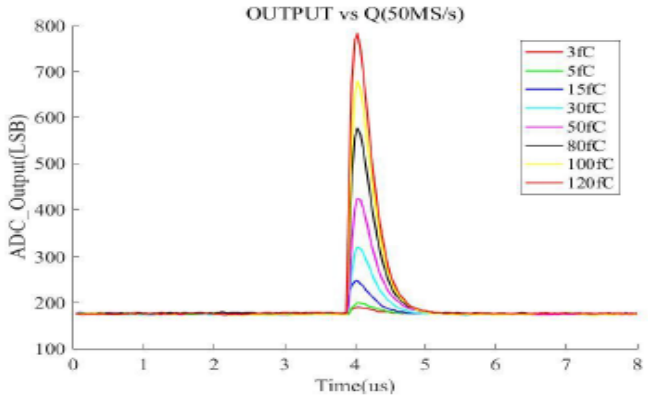
## Power Consumption

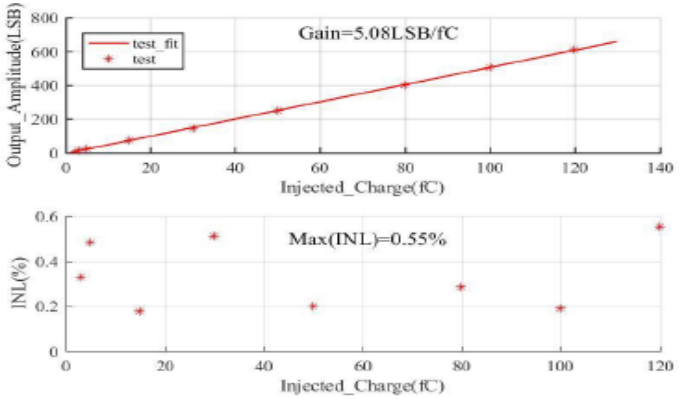



- Adjustable by an external resistor. At normal bias current of 25 μA, the power consumption of AFE part is **2.50 mW/ch**
- The power consumption of ADC part is **5.41 mW/ch** at 50MS/s. ADC core circuits consume 1/4 of the total ADC power (**1.35 mW/ch** )

## Non-Linearity

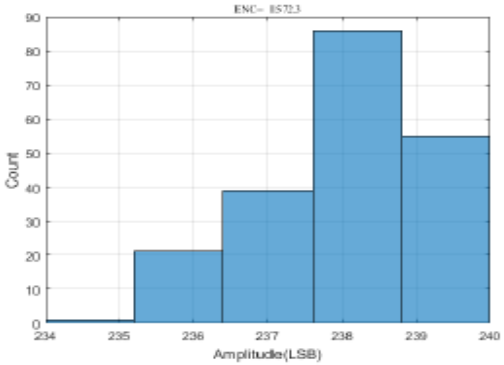


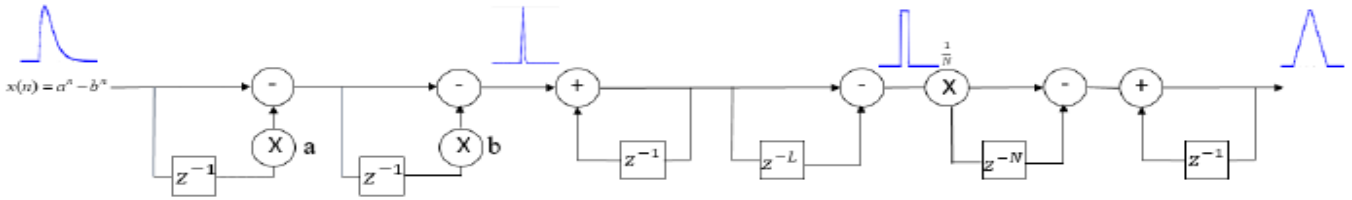

The maximum INL is 0.55% for the dynamic range up to 120fC (gain = 5.08 LSB/fC)

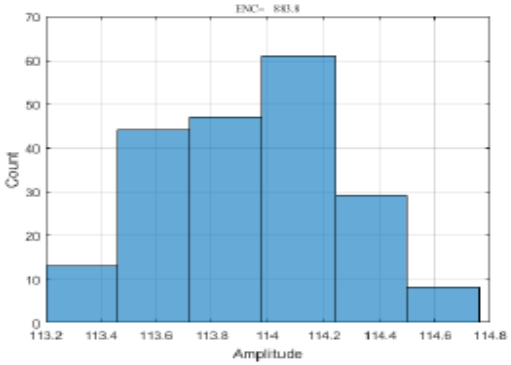
# Noise results

- Noise




Amplitude distribution of the direct ASIC outputs with 50 fC injected charge: ENC = 1572 e @ 4.3pF.




Amplitude distribution of the trapezoidal filter outputs implemented in Matlab: ENC = 883 e @ rising time = 1 μs and flat top time = 0.2 μs

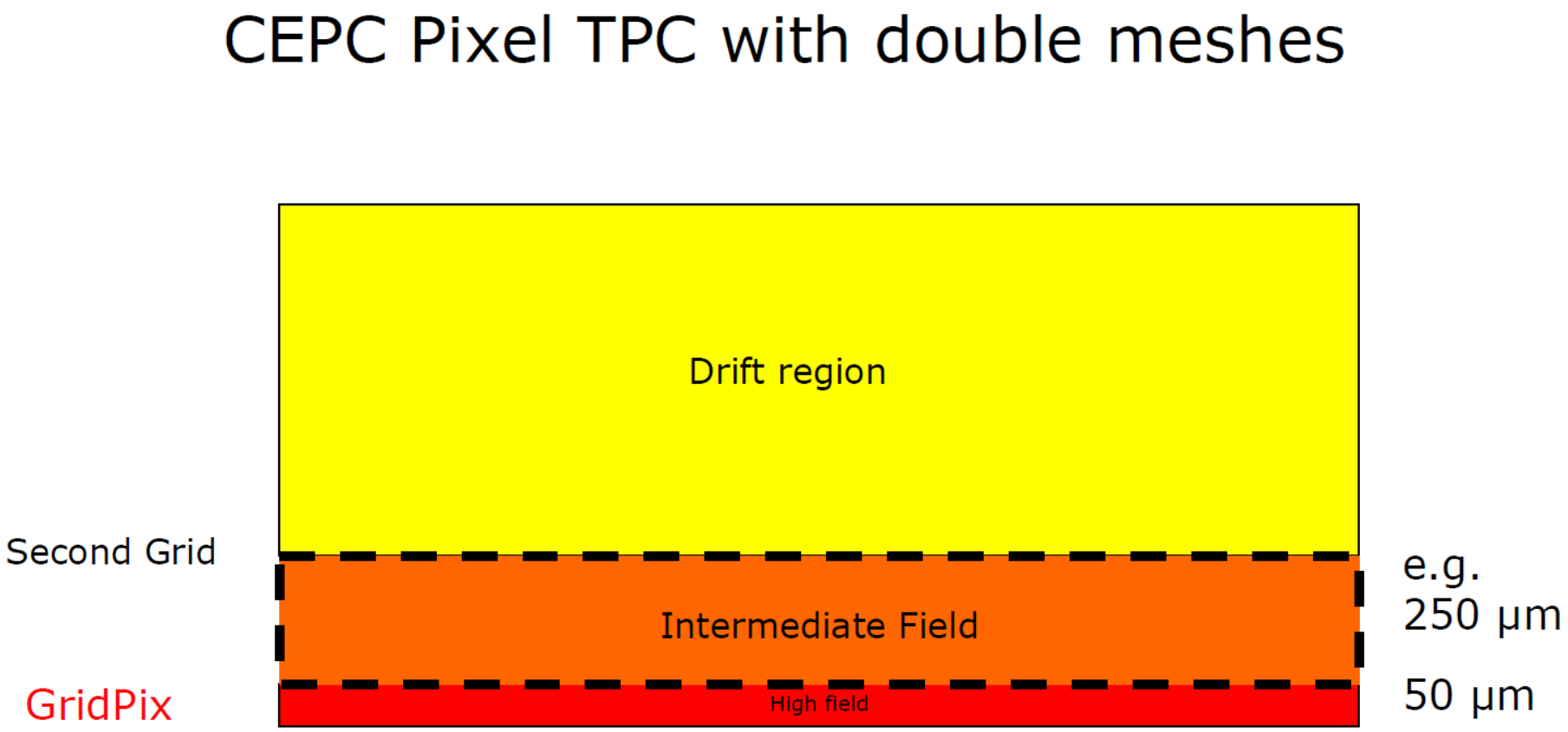
- Status of the collaboration

# New consideration for lowest IBF at low gain

## CEPC Pixel TPC with double meshes

- **Question**: can one reduce the Ion Back Flow of a GridPix detector?
- IHEP and Nikehf
  - Too design a GridPix detector using a double grid
  - The idea is that by creating two field regions, one with a medium field and one with a high field (Standard Grid Pix) one could reduce the ion backflow in two stages.
  - The high field avalanche region has a measured IBF of 1.3%
  - The aim is to reduce the IBF by another factor 100
  - The second Grid replaces the Gating device and is always operational

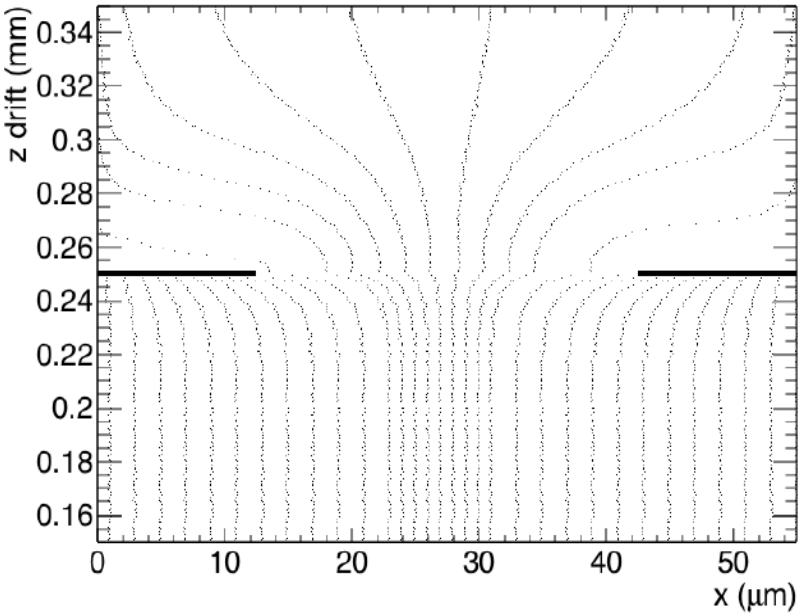
# Concept of the double meshes



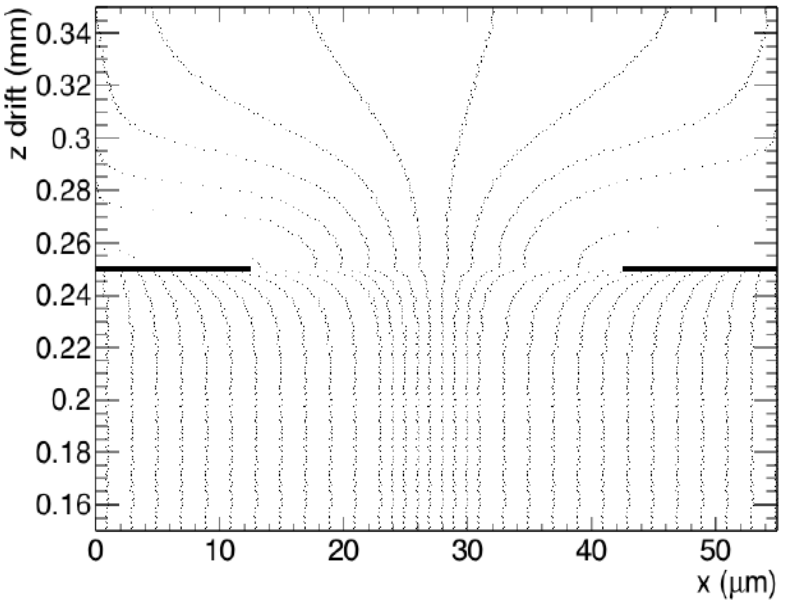
# Concept

## Simulation of backflow trajectories second Grid

Field ratio 40




Field ratio 240




Field ratio = E_2/E_1

# Ion backflow for a double grid

- Calculations for the IBF of the two meshes in case one has a total FR240 – normal GridPix operation. The lower Grid(Pix) was at FR16 too.

| Ion backflow | Hole 30 μm | Hole 25 μm | Hole 20 μm |
|---|---|---|---|
| Top grid | 2.2% | 1.2% | 0.7% |
| GridPix | 5.5% | 2.8% | 1.7% |
| Total (IBF) | $12\times10^{-4}$ | $3\times10^{-4}$ | $1\times10^{-4}$ |
| Electron transparency | 100% | 99.4% | 91.7% |

- In order to reach IBF×Gain (Gain $10^3$) below one has to choose a slightly
- Smaller hole size of 25 or 20 microns. (460LPI- 510LPI)
- The new meshes delivered to Nikehf and tests will be collaborated.

# Summary

- All of contents will be reported: “Development of IBF suppression TPC integrated with low power ASIC and laser beams”, ICHEP2020
- Some update progress of the TPC prototype R&D in last three months.
- Some update progress of the TPC ASIC chips R&D and the results of the power consumption and noise.
- Some update collaboration of the new concept R&D with Nikehf.

# Thanks!