Firmware Status

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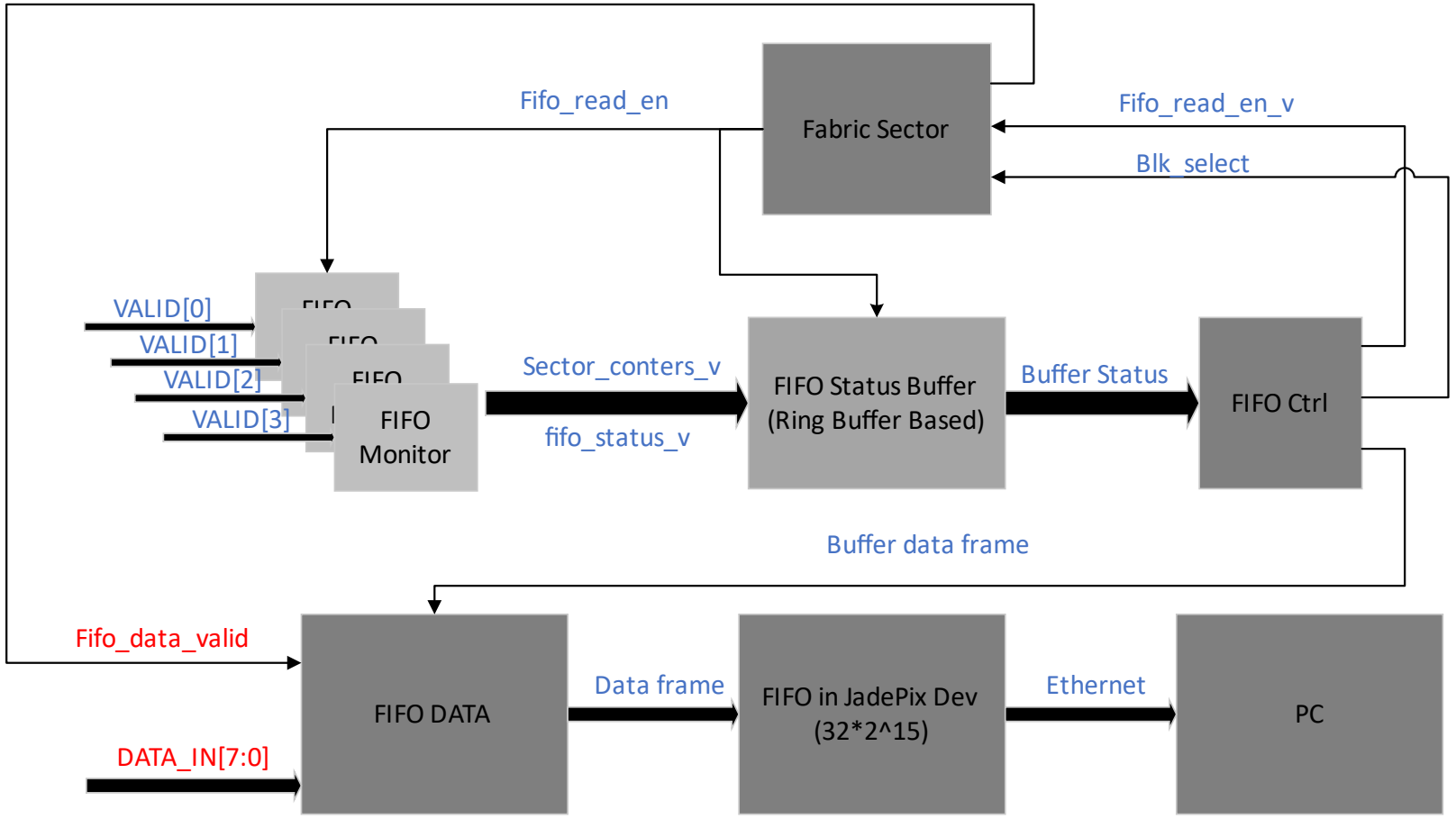
Jadepix Data Readout



FIFO type: Standard or First Word Fall Though?

fifo_data_valid: one clock period after signal fifo_read_en ?

There are WFIFO and RFIFO slaves in Jadepix device, so we can read DATA in RFIFO Periodically.
Need to test how fast the data should be read, and the number of data for one block read.

Simulation and ILA test

- The chip control logic, data readout logic can be simulated via Modelsim/Questasim.
- Testbench directory: {Firmware_root}/sim
- Next step: Software and ILA test
- How to archive data? .bin?